

# Analytic Models for Crosstalk Delay and Pulse Analysis Under Non-Ideal Inputs<sup>1</sup>

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## Abstract

In this paper we develop a general methodology to analyze crosstalk to obtain insight into effects that are likely to cause errors in deep submicron high speed circuits. We focus on crosstalk due to capacitive coupling between a pair of lines. We first consider the case where crosstalk noise manifests as a pulse and characterize the maximum amplitude, width, energy and timing of this pulse. Closed form equations quantifying the dependence of these pulse attributes on the values of circuit parameters and the rise time of the input transition are derived. We also consider how crosstalk causes slowdown (speedup), i.e. increases (decreases) the rise/fall times of signals on coupled lines, when their inputs have transitions in the opposite (same) directions. Expressions relating the slowdown (speedup) to circuit parameters, the rise/fall times of the input transitions, and the skew between the transitions are derived. We show that crosstalk effects can be significantly aggravated by variations in the fabrication process. New design corners are identified for validation of designs that have significant crosstalk effects. Finally, the results of our analysis provide conditions that must be satisfied by a sequence of vectors used for validation of designs as well as post-manufacturing testing of devices in the presence of significant crosstalk.

## I. Introduction

Continuous advancements in the field of VLSI has lead to a decrease in device geometries (deep sub-micron technology), high device densities, high clock rates and small signal transition times. Due to these changes, crosstalk noise between adjacent interconnects has become an important concern. If not carefully considered during design validation, crosstalk may cause extra signal delay, logic hazards, and even circuit malfunction. Accurate modeling and simulation of interconnect delay due to crosstalk thus becomes increasingly important in the design of high performance integrated circuits.

The modeling and analysis of crosstalk between interconnection lines have previously received considerable attention. Most crosstalk transient analysis techniques model interconnects as microstrip lines and utilize the well known multiconductor transmission line theory [1]. The analysis of coupled lossy transmission lines has been considered by several authors [2-6]. Numerical methods to solve a model of lossy transmission lines in the time domain have been proposed in [7,8]. Simulation models for interconnects and crosstalk were reported in [9,10]. Nonlinearity of the source and load networks, not addressed in these papers, were considered in [15-18]. Although the above techniques are very effective for specific cases, they provide little general insights into the coupling mechanism. In addition, these analysis methodologies are often not applicable to VLSI circuits because of the complexity of the circuit model used and high computation time. In [11,12], a simplified lumped RC model for crosstalk between a pair of coupled lines was proposed and the case is analyzed where the input to one line is held constant while the other has a step transition. In this case, the crosstalk effect manifests as a pulse on the line whose input is held constant. Further study of crosstalk speedup and slowdown, which occur when inputs to both lines have transitions, is necessary for the design of high performance systems because of small delay slacks of critical paths.

The purpose of this paper is to develop a general methodology to analyze and obtain greater insight into the crosstalk phenomenon. A methodology is presented and used to characterize cases where inputs to one or both coupled lines have transitions with arbitrary transition times and directions. Our analysis starts with a model in the frequency domain ( $s$  domain) to obtain a closed form voltage transfer function. This is then transformed to obtain expressions in the time domain. These expressions are used to characterize the amplitude, width, energy, and timing of the pulse, as well as the speedup or slowdown of transitions due to crosstalk.

The paper is organized as follows. In section II the proposed methodology to analyze crosstalk is presented, followed by the derivation of closed form expressions for the frequency domain transfer functions

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and time domain signal waveforms. In section III we discuss the analytic results. In section IV we discuss design and test issues for various crosstalk situations. Finally, in section V we present our conclusions.

## II. Crosstalk Analysis

### 2.1 Crosstalk Effects

In VLSI circuits it is very common to have wires running adjacent to one another. In submicron designs, due to greater proximity of adjacent wires on the same layout layer, increase in the heights of wires (relative to their widths), and increase in the switching speeds of signals, the parasitic coupling effects are significant. Coupling effects produce interference between signals, referred to as crosstalk noise, and may increase or decrease signal delays and decrease signal integrity.

Parasitic coupling includes inductive and capacitive effects. There is a low inductance value that becomes significant at very high frequency in certain lines, such as VDD and GND global buses, which are very long and wide and may conduct large switching current. For signal interconnects it is still feasible to accurately model crosstalk without considering inductance because of the voltage controlled nature of MOS devices. Fig. 1 shows a simple circuit with mutual capacitance  $C_m$  between two signal lines A and V.

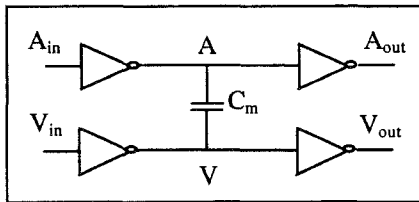


Figure 1 Simple circuit showing source of crosstalk due to capacitive coupling

Crosstalk noise may cause undesirable effects including excessive overshoot, undershoot, glitches, addition signal delay and even a reduction in signal delay. These effects can lead to possible circuit malfunction (permanent errors) and increased power dissipation. Fig. 2 shows the effects of crosstalk obtained by SPICE simulation on the signal V in Fig. 1. In the simulation, we assume that wire resistance and coupling capacitance can be modeled as a lumped resistance,  $R_{ine}$ , and a lumped capacitance,  $C_m$ , (lumped RC model), respectively, and the size of the transistors in the inverters and lengths of the metal wires are chosen to obtain a nominal driver output response with a rise time of about 130ps, which is realistic assuming a clock period of 4 ns. For reliable operation, some aspect of the worst case crosstalk pulse, such as energy or maximum amplitude, should be bounded and the input patterns that maximize these

aspects of crosstalk should be used during design validation. In Fig. 2 (a) we see that a pulse is generated on line V, which should ideally have a constant zero, due to a rising transition on line A. Fig. 2 (b) shows that when A and V have transitions in the same (or different) directions, the results is a decrease (or increase) in the signal transition time (speedup/slowdown) of signal V.

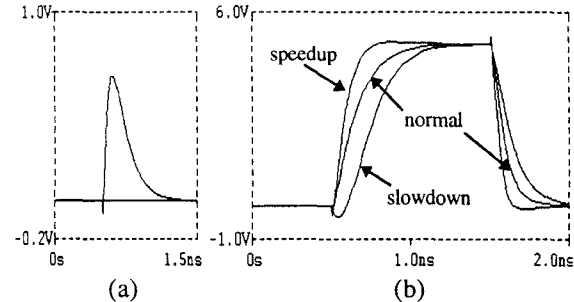


Figure 2 Crosstalk waveforms of signals in Figure 1 (a) Crosstalk pulse; (b) Crosstalk decreases/increases signal transition times (speedup/slowdown)

### 2.2 Crosstalk Model and Analysis

To obtain insight into the detailed nature of crosstalk and its dependence on the circuit parameters associated with the coupled lines, consider the lumped model of capacitive coupling shown in Fig. 3.

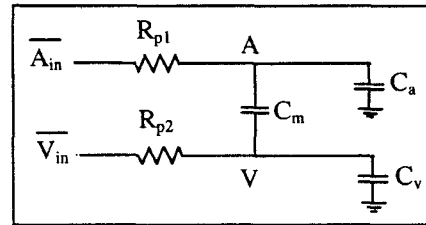


Figure 3 Capacitive coupling model

In this model, each pulling resistance,  $R_{p1}$  or  $R_{p2}$ , is composed of the line resistance and the on-channel resistance associated with the line driver, where we assume the complementary device is off immediately after the inputs are applied. In [13,14] it is shown that the impact of neglecting the short circuit current is small provided that the transition time is short. The load capacitances,  $C_a$  and  $C_v$ , consist of the line capacitance and the gate capacitance of the load driven by the line. Thus the line driver is equivalent to a pulling resistance, and the coupling network can be viewed as a network of capacitors ( $C_m$ ,  $C_a$ ,  $C_v$ ). Compared with the simplified model in [11], which assumed a linear rise/fall time on the node A, our expanded model allows for a more general model of the signals  $A_{in}$  and  $V_{in}$ , not only in terms of their switching rates but also their relative skew.

#### 2.2.1 Analysis Procedure

We de-couple the system shown in Fig. 3 into an input waveform stage, a driver characterization stage and a coupling network stage. By doing this, we can employ more complex models to obtain more accurate results, take into account input waveforms other than ideal step functions, and thus analyze crosstalk induced speedup and slowdown (delay).

By using Laplace transformations, we can accomplish the following:

- 1) for the input waveform stage, obtain the Laplace transfer expressions for fairly complex inputs,
- 2) for the driver characterization stage, obtain the transfer function of the line driver model at a desired degree of accuracy,
- 3) for the cross-coupling network, obtain the transfer function from V to A.

By cascading these three stages we can obtain an expression for crosstalk in the s-domain, which we can transform back to the time domain. The analytic response we derive is based on the first order model of MOS device behavior, commonly referred as the LEVEL 1 model, assuming that the channel modulation is negligible. This model was selected because more sophisticated models that take into account higher order effects are intractable for analytic manipulation. The insights gained from the results obtained using this simple model are sufficiently useful.

### 2.2.2 Analysis of Crosstalk Pulse

To illustrate the analysis procedure, consider the case of a positive crosstalk pulse induced on node V (victim line) due to a rising transition at node A (affecting line). The input  $A_{in}$  to the inverter driving the affecting line in Fig. 1 is a falling transition, and the input  $V_{in}$  to the inverter driving the victim line is kept high so that the victim line should remain at a constant low.

After the input to  $A_{in}$  is applied, the pulling device (PMOS) of the inverter driven by  $A_{in}$  can be modeled by its on channel resistance,  $R_{on}$ , connecting A to VDD; the corresponding NMOS device is off. The inverter driven by  $V_{in}$  can be modeled by the channel resistance of its NMOS device connecting V to GND. For computational convenience, we normalize VDD to be 1 and GND to be 0. Fig. 4(a) shows the circuit model for the situation just described. Fig. 4(b) shows the equivalent circuit of Fig. 4(a).

Some notation used throughout the rest of this paper is described next:

A - node or signal at A,

$A(t)$  - voltage at A in time domain,

$A(s)$  - voltage at A in frequency domain,

$A_{exp}(t)$  - voltage at A when  $A_{in}(t)$  is an exponential signal and  $V_{in}(t)$  is stable,

$A_{step}(t)$  - voltage at A when  $A_{in}(t)$  is a step function and  $V_{in}(t)$  is stable,

$A_{su}(t)$  - voltage at A when  $A_{in}$  and  $V_{in}$  are exponential inputs with identical directions of transition,

$A_{sd}(t)$  - voltage at A when  $A_{in}$  and  $V_{in}$  are exponential inputs with opposite directions of transition.

(In the above, A and V can be interchanged to derive another set of notation.)

Let "H" indicate a transfer function and its subscript indicate the node name or conventional output-to-input notation.

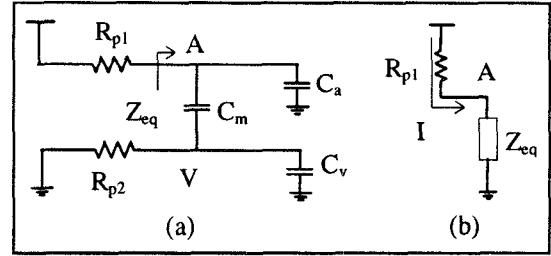


Figure 4 Circuit model for crosstalk pulse analysis. (a): Circuit model for a positive pulse induced on V due to a rising transition on A; (b) an equivalent circuit

From Fig. 4(a), solving for the impedance at node A, we have

$$Z_{eq} = (C_m + C_a) - C_m \cdot \frac{V(s)}{A(s)}$$

The transfer function from V to A is

$$\frac{V(s)}{A(s)} = \frac{sC_m}{\frac{1}{R_{p2}} + s(C_m + C_v)}$$

Therefore,  $Z_{eq}$  can be expressed as

$$Z_{eq} = \frac{(C_m + C_a) + sR_{p2}C_t}{1 + sR_{p2}(C_m + C_v)}$$

where  $C_t = C_m C_v + C_m C_a + C_a C_v$ .

Now,  $A(s) = H_A = H_{A/A_n} H_{A_n}$ , where  $H_{A/A_n}$  is the characteristic transfer function of the low pass circuit composed of the pulling resistance  $R_{p1}$  and the equivalent reactance  $Z_{eq}$ , namely  $H_{A/A_n} = \frac{\tau}{s + \tau}$ , where  $\tau = 1/R_{p1} Z_{eq}$ . If the input is a unit step function then  $H_{A_n} = 1/s$  and

$$A(s) = H_A = \left(\frac{\tau}{s + \tau}\right) \frac{1}{s}$$

One can think of this transfer function as the product of the driver characteristic transfer function stage and an input waveform transformation stage. Thus, the transfer function of node V to the input is

$$V(s) = H_V = H_{V/A} \cdot H_{A/A_n} \cdot H_{A_n}$$

where  $H_{V/A}$  is the coupling network transfer function,  $H_{A/A_n}$  is the transfer function of the driver that contains

$R_{p1}$  and  $Z_{eq}$ , and  $H_{A_{in}}$  is the Laplace expression of the input seen by the driver characterization stage.

Carrying out the algebra

$$V(s) = H_V = \frac{C_m}{R_{p1}C_t} \left( \frac{1}{w-u} \right) \left( \frac{1}{s-w} - \frac{1}{s-u} \right), \text{ and}$$

$$A(s) = H_A = \frac{1}{s} - \frac{1}{w-u} \left( \frac{1}{s-w} - \frac{1}{s-u} \right) \left( s + \frac{C_m + C_a}{R_{p2}C_t} \right),$$

where  $w, u$  are solutions to the quadratic equation,

$$s^2 + s \left( \frac{R_{p1}(C_m + C_a) + R_{p2}(C_m + C_v)}{R_{p1}R_{p2}C_t} \right) + \frac{1}{R_{p1}R_{p2}C_t} = 0,$$

and both  $w$  and  $u$  are negative.

The time domain voltage waveform  $V(t)$  is obtained by taking the inverse Laplace transformation of its corresponding  $s$ -domain expression, resulting in

$$V(t) = \left( \frac{C_m}{R_{p1}C_t} \right) \left( \frac{1}{w-u} \right) (e^{wt} - e^{ut}).$$

For arbitrary input waveforms instead of step functions, we can modify the above input waveform transformation stage. Inputs such as step functions, ramps, exponentials or combinations of the above are commonly seen in electrical models and are easy to use in transformation analysis. For example, assume the input to the driver stage is an exponential rising waveform  $(1 - e^{-t/x})$ , where  $x$  is the time constant. The  $s$ -domain expression of this waveform is  $[(1/s) - (1/(s+1/x))]$ . The transfer function at  $A$ , namely  $H_{A_{exp}}$ , under this exponential input is

$$\begin{aligned} H_{A_{exp}} &= H_{A/A_{in}} \cdot H_{A_{in}} = \frac{\tau}{s+\tau} \left( \frac{1}{s} - \frac{1}{s+1/x} \right) \\ &= \left( \frac{1}{s} - \frac{1}{s+\tau} \right) \frac{1}{s+1/x} = H_{A_{step}} \cdot \frac{1/x}{s+1/x}, \end{aligned}$$

where  $H_{A_{step}}$  is the transfer function  $H_A$  discussed previously (the voltage seen by the driver stage is a step function), and the subscripts are used to indicate the type of input waveform.

Hence, an exponential input results in a modulation term  $1/x(s+1/x)$ . Using this technique, the corresponding victim line time domain response is

$$\begin{aligned} V(t) &= \frac{C_m}{R_{p1}C_t} \left( \frac{1/x}{(w+1/x)(w-u)} e^{wt} \right. \\ &\quad \left. + \frac{1/x}{(u+1/x)(u-w)} e^{ut} + \frac{1/x}{(w+1/x)(u+1/x)} e^{-t/x} \right). \end{aligned}$$

Fig. 5 shows the crosstalk pulse on line  $V$  due to a unit step transition and an exponential transition on line  $A_{in}$ , where for the latter case the rise time is 130ps, i.e. a rise time of  $x=55.56$ . It can be seen that the pulse due to a

step transition on  $A_{in}$  has higher amplitude than when an exponential transition occurs at  $A_{in}$ .

### 2.2.3 Analysis of Crosstalk Delay

By using the techniques described above, we can analyze effects such as when both signals  $A$  and  $V$  change simultaneously and in the same direction to cause signal speedup, or change in the opposite direction to cause extra delay, change with a relative timing skew so that the interference between signal pairs causes distortion on the signal waveforms.

Consider the case where the affecting line  $A$  has a falling transition and line  $V$  has a rising transition. The equivalent circuit model is shown in Fig. 6. Here we assume that exponential waveforms of time constants  $x$  and  $y$  are applied to  $A_{in}$  and  $V_{in}$ , respectively, and the  $A_{in}$  signal has a time skew of  $z$  units with respect to signal  $V_{in}$ , where  $z$  can be positive or negative.

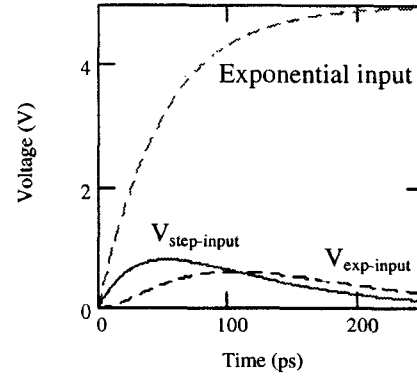


Figure 5 Crosstalk pulse at  $V$  due to exponential and step inputs at  $A_{in}$

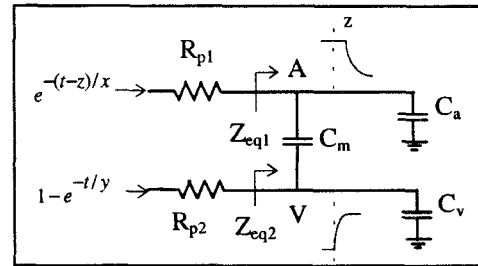


Figure 6 Equivalent circuit for crosstalk delay analysis

By using the techniques described in section 2.2.2, the Laplace transformation for shifting the time-axis, and proper initial conditions, we have the following results.

$$A_{sd}(s) = \left[ \left( \frac{1}{s + \frac{1}{R_{p1}Z_{eq1}}} \right) \left( \frac{1/x}{s+1/x} \right) + \frac{1}{s+1/x} \right] e^{-sz} - \frac{e^{-sz}}{s} + \frac{1}{s}, \text{ and}$$

$$V_{sd}(s) = \left(\frac{1}{s}\right) \left(\frac{R_{p2} Z_{eq2}}{s + \frac{1}{R_{p2} Z_{eq2}}}\right) \left(\frac{1/y}{s+1/y}\right),$$

where

$$Z_{eq1} = \left[ \frac{1}{sA_{sd}(s) - 1} (sA_{sd}(s)(C_m + C_a) - sC_m V_{sd}(s) - C_a - C_m) \right],$$

and

$$Z_{eq2} = C_m + C_a - C_m \frac{A_{sd}(s)}{V_{sd}(s)} + \frac{C_m}{V_{sd}(s)}.$$

By solving the above system of equations, we obtain

$$A_{sd}(s) = \left[ A_{step}(s) \left( \frac{1/x}{s+1/x} \right) + \frac{1}{s+1/x} \right] e^{-sz} + \left( \frac{C_m}{R_{p2} C_i} \frac{1}{(s-w)(s-u)} \right) \left( \frac{1/y}{s+1/y} \right) + \left[ \frac{1}{s} + \frac{e^{-sz}}{s} \right],$$

and

$$V_{sd}(s) = V_{step}(s) \left( \frac{1/y}{s+1/y} \right) - \left( \frac{C_m}{R_{p1} C_i} \frac{1}{(s-w)(s-u)} \right) \left( \frac{1/x}{s+1/x} \right) e^{-sz},$$

where

$$A_{step}(s) = \frac{1}{(s-w)(s-u)} \left( s + \frac{C_m + C_a}{R_{p2} C_i} \right),$$

and

$$V_{step}(s) = \frac{1}{s} - \frac{1}{(s-w)(s-u)} \left( s + \frac{C_m + C_v}{R_{p1} C_i} \right).$$

We can interpret these equations in the following way.

**“Total response on line V = (signal due to step input at V<sub>in</sub>)\*(modulation on line V) + (coupling from line A)\*(modulation on line A)\*(skew on line A)”**

where  $\left(\frac{1/y}{s+1/y}\right)$  represents the modulation on line V due

to the finite signal transition time,  $\left(\frac{1/x}{s+1/x}\right)$  represents the modulation on line A, and  $e^{-sz}$  represents the time skew of line A with respect to the signal on line V.

$A_{sd}(s)$  can be interpreted in a similar manner except that there are also terms resulting from initial conditions.

The waveforms of A and V are given by the expressions

$$A_{sd}(t) = A_{exp}(t) + \frac{1}{y} \left[ \frac{c}{(w+1/y)(w-u)} e^{wt} + \frac{c}{(u+1/y)(u-w)} e^{ut} + \frac{c}{(w+1/y)(u+1/y)} e^{-t/y} \right],$$

$$V_{sd}(t) = V_{exp}(t) - \left[ \frac{1}{x} \left[ \frac{b}{(w+1/x)(w-u)} e^{w(t-z)} + \frac{b}{(u+1/x)(u-w)} e^{u(t-z)} + \frac{b}{(w+1/x)(u+1/x)} e^{\frac{-(t-z)}{x}} \right] U(t-z) \right],$$

where

$$A_{exp}(t) = \left( \frac{1}{x} \left[ \frac{w+a}{(w+1/x)(w-u)} e^{w(t-z)} + \frac{u+a}{(u+1/x)(u-w)} e^{u(t-z)} + \frac{a-1/x}{(w+1/x)(u+1/x)} e^{\frac{-(t-z)}{x}} \right] + e^{\frac{-(t-z)}{x}} \right) U(t-z) + U(t) - U(t-z),$$

$$V_{exp}(t) = 1 - e^{-t/y} - \frac{1}{y} \left[ \frac{w+f}{(w+1/y)(w-u)} e^{wt} + \frac{u+f}{(u+1/y)(u-w)} e^{ut} + \frac{f-1/y}{(w+1/y)(u+1/y)} e^{-t/y} \right],$$

$$a = \frac{C_m + C_a}{R_{p2} C_i}, \quad c = \frac{C_m}{R_{p2} C_i}, \quad b = \frac{C_m}{R_{p1} C_i}, \quad f = \frac{C_m + C_v}{R_{p1} C_i},$$

$$C_i = C_m C_v + C_m C_a + C_a C_v,$$

and U(t) is a unit step function.

The terms in  $A_{sd}(t)$ , except for  $A_{exp}(t)$ , contribute to the slowdown effect caused by the mutual capacitance. The terms in  $V_{sd}(t)$  contribute in a similar way.

Similar equations have been derived for speedup [23].

Fig. 7 shows the degree of speedup or slowdown due to coupling effects, assuming that the input signals switch simultaneously, i.e.  $z = 0$ . The circuit configuration is shown in Fig. 8. The circuit consists of two unbalanced drivers with a 4000 $\mu$ m long and 4 $\mu$ m wide metal2 affecting line A driven by the larger driver (64 $\mu$ /0.8 $\mu$  PMOS and 32 $\mu$ /0.8 $\mu$  NMOS), and a 1000 $\mu$ m long and 2 $\mu$ m wide metal1 victim line V driven by the smaller driver (16 $\mu$ /0.8 $\mu$  PMOS and 8 $\mu$ /0.8 $\mu$  NMOS). Fig. 8 also shows the dimensions of the components. R, C and gain values used for analysis and simulations have been extracted from a layout, where  $R_{m1}$ ,  $R_{m2}$  are metal1 and metal2 line resistances,  $C_{m1g}$ ,  $C_{m2g}$  are metal1 and metal2 line-to-substrate capacitances, and  $C_m$  is the mutual capacitance.

Consider the case where V has a rising transition and A remains constant. Then from Fig. 7(a) we see that V reaches  $0.5 \times 5 = 2.5$  volts at about  $t = 99$ ps. Now if A simultaneously has a rising transition, then V reaches 2.5 volts at  $t = 80$ ps, i.e. 19ps earlier. This illustrates the concept of crosstalk speedup.

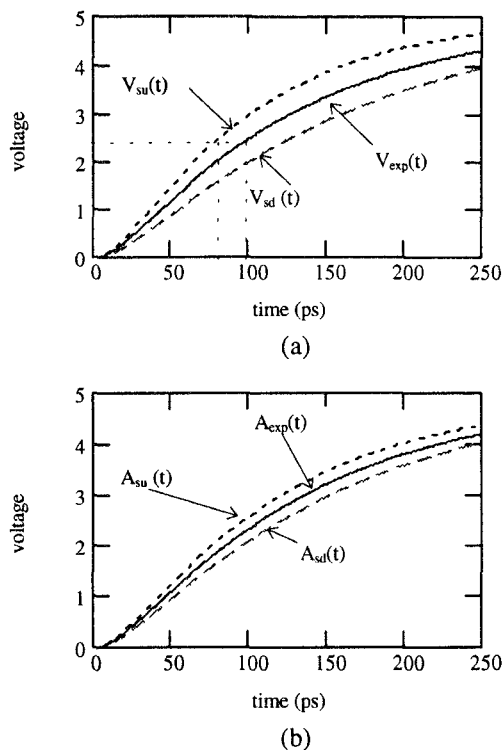


Figure 7 Crosstalk speedup and slowdown effects assuming simultaneously switching inputs where both inputs have a transition time of 200ps. (a) effects on victim line; (b) effects on affecting line

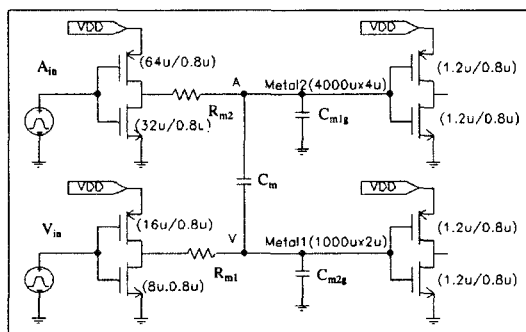


Figure 8 Circuit used to study influence of input signal properties and circuit parameters on crosstalk

By using the sensitivity analysis on the equations described previously, we can observe that the severity of crosstalk is directly proportional to the mutual capacitance, line V resistance, and inversely proportional to the line A resistance and the load capacitance on each line.

### III. Input Waveforms, Process Variations, and Crosstalk

In this section we investigate in more detail the dependence of crosstalk on input waveform and skew. We

will also see how coupling effects can be further aggravated by variations in the manufacturing process.

#### 3.1 Dependence of Crosstalk Effects on Input Waveform and Timing

##### 3.1.1 Crosstalk Delay

Let the delay time of a falling transition on a line be  $t_d$  when the other line is static,  $t_{d-su}$  when both lines have transitions in the same direction, and  $t_{d-sd}$  when both lines have transitions in opposite directions. The speedup-time due to the coupling effect is  $(t_d - t_{d-su})$ , and the slowdown-time is  $(t_{d-sd} - t_d)$ . Fig. 9 shows the effects of speedup with respect to input waveform switching rates, i.e. the time constants,  $x$  and  $y$ , of the exponential inputs. For simplicity, we assume both signals switch simultaneously, i.e.  $z = 0$ . As  $x$  decreases, the exponential waveforms  $e^{-t/x}$  and  $(1 - e^{-t/x})$  approach ideal step functions. In modern CMOS technologies the signal rise/fall times range from 100ps to 300ps, thus  $x$  ranges from 44 to 130. The curve with  $y = 44$  corresponds to the case when the victim line input  $V_{in}$  has a rise time of 100ps; the one with  $y = .01$  corresponds to a step function.

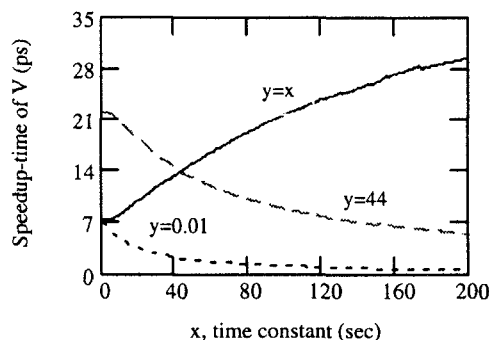


Figure 9 The victim line speedup-time vs. input switching rates

From Fig. 9 we can see that when the input signal to the victim line is kept at a fixed switching rate, then the faster the affecting line changes the larger the speedup of the victim line. Also for the case  $x=y$ , we see that the absolute amount of speedup increases as  $x$  increases. For example, an exponential signal with a rise/fall time of 100ps ( $x = 43.48$ ,  $t_d = 64$ ps) has a speedup-time of 14ps and one with a rise/fall time of 200ps ( $x = 83.33$ ,  $t_d = 108$ ps) has a speedup-time of 21ps. However, the percentage change in delay decreases as both  $x$  and  $y$  increase. The speedup-time in the former case (100ps) represents a 22% decrease in delay, while that in the later case represents a 19% decrease in delay. This implies that slow transition signals have less effect than fast transition signals.

Similar result have been obtained for the case of slowdown [23].

We now consider the amount of speedup and/or slowdown as a function of  $z$ , the time skew between the two signal transitions when  $A_{in}$  and  $V_{in}$  have rise/fall time of 100ps. Fig. 10 shows the voltage waveforms on both lines, assuming the transition on the affecting line occurs first. In the time interval  $0 < t < z$ , A either pre-charges or discharges V. Eventually, when  $V_{in}$  changes, A and V affect each other and lead to a speedup or slowdown. From Fig. 10 we can see that the coupling effect between these two lines are different due to the difference in line driver strengths and loads.

Fig. 11 shows the influence of the input signal time skew  $z$  on the amount of speedup and slowdown where  $A_{in}$  and  $V_{in}$  have rise/fall times of 100ps.

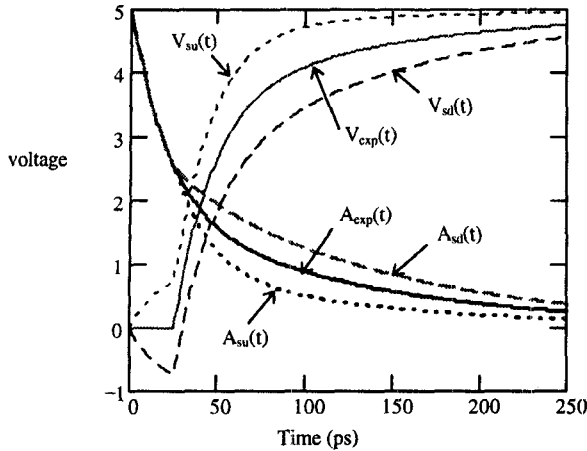


Figure 10 Voltage waveforms on affecting and victim lines for  $z = 25$  ps

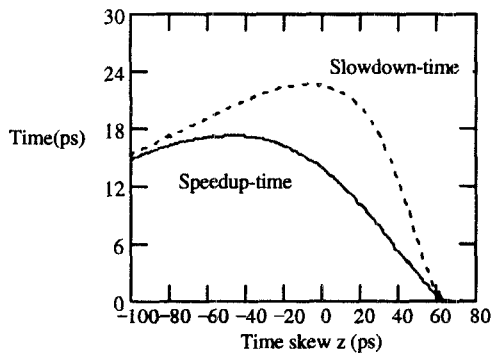


Figure 11 Victim line speedup-time and slowdown-time vs. skew  $z$

From Fig. 11 we observe that as  $z$  increases the amount of speedup and slowdown on V both first increase and then decrease. For the speedup situation, if A switches earlier than V, then A helps charge/discharge V before V changes, increasing the speedup. The amount of speedup reaches its maximum value when the coupling effect from

A is maximum (i.e. where the pulse at V due to A is maximum). After that, the remaining effect of A on V starts to dissipate and hence the speedup decreases. Also from Fig. 11, we can observe that the slowdown is maximum when signals switch simultaneously. This can be explained by considering the fact that a rapid change in the voltage at A transfers charge to node V via the coupling capacitance  $C_m$ . If the transition at V occurs concurrently with the transition at A, then the entire charge transferred is discharged via the pull down of the inverter driving line V, increasing its fall time. On the other hand, if A switches earlier than V, then some of the transferred charge is discharged via the pull up of the inverter driving the line V prior to its switching. Hence only a part of the charge transferred from A is discharged when V begins to fall, decreasing the slowdown. If A switches later than V, then for a time  $z$ , V transits toward its target value before A affects it, hence the slowdown is decreased. For  $z$  greater than some fixed amount  $z_0$ , A cannot impact V since V has already reached 50% of VDD, which defines the delay time  $t_d$ .

### 3.1.2 Crosstalk Pulse

Consider once again the results of the crosstalk pulse analysis presented in section 2.2.2. The crosstalk pulse waveform is given by

$$V(t) = \frac{C_m}{R_{p1}C_i} \left[ \frac{1/x}{(w+1/x)(w-u)} e^{wt} + \frac{1/x}{(u+1/x)(u-w)} e^{ut} + \frac{1/x}{(w+1/x)(u+1/x)} e^{-t/x} \right].$$

To determine the effects of the input waveform shape on the crosstalk pulse, including its amplitude, the time the pulse reaches its maximum amplitude, and the energy of the pulse, we can differentiate or integrate the above voltage waveform expression. After some mathematical manipulations, we obtained the following results, which have also been verified by detailed SPICE simulations.

- 1) The time  $t_0$  at which the pulse reaches its maximum value is proportional to  $x$ , more precisely, it is proportional to  $\frac{1}{p+1/x} \ln \left[ \frac{q}{x(r+1/x)} \right]$ , where  $p, q, r$  are constants. That is, the faster the input transition the smaller the value of  $t_0$ .
- 2) The maximum amplitude of the pulse,  $V_{max}$ , is approximately proportional to  $(1 - ce^{-d/x})$ , where  $c, d$  are constants. Thus slower input transitions lead to smaller values of  $V_{max}$ .
- 3) The energy contained in the pulse is independent of  $x$ .

Simulation Cases	Mean Delays (ps)	Minimum Delay (ps)		Maximum Delay (ps)	
		Values	% deviation from mean	Values	% deviation from mean
Nominal Delay	217.3	177.4	18.4	269.5	24.0
Crosstalk Slowdown	315.0	248.0	21.3	400.0	27.0
Crosstalk Speedup	165.5	128.2	22.5	205.7	24.3

Table 1 Effect of process variations on crosstalk delay (pico seconds)

Simulation Cases	Mean Value (V)	Minimum Height (V)		Maximum Height (V)	
		Value	% deviation from mean	Value	% deviation from mean
Crosstalk pulse height	0.65	0.43	33.8	0.93	43.0

Table 2 Effect of process variations on crosstalk pulse height

### 3.2 Impacts of Process Variations on Crosstalk Effects

In this section we illustrate the effect on crosstalk of variations in the values of electrical parameters due to manufacturing. The results are obtained by SPICE simulation of the circuit shown in Fig. 8 and combinations of changes in electrical parameters are selected that are consistent with the correlations that exist in actual process data [22]. The parameter data presented is based on a 0.8 micron process with a single poly and three metal layers.

#### 3.2.1 Crosstalk Delay

The delay of a signal V is influenced by capacitive coupling and the transitions that occur at A and V. For simplicity, only the case where V has a rising transition is considered.

The nominal delay values are calculated for each case using nominal values for all electrical parameters. The worst case behaviors are excited by selecting the appropriate value for each parameter. From the previous discussion about dependence, the maximum delay is obtained by selecting the maximum value of mutual capacitance between the interconnects ( $C_m$ ), the maximum value of interconnect to substrate capacitance ( $C_a$ ), minimum value of  $C_v$ , the maximum transistor gain values (minimum equivalent on-channel resistance) for line A driver, the minimum transistor gain for line V driver, and the minimum and maximum values of line resistances for the affecting and victim lines, respectively. The minimum delay case situation is obtained in a similar way. All parametric values selected are within the acceptable range of the process. We assume inputs switch simultaneously with a rise/fall time of 100ps.

The delay values obtained are shown in Table 1. Due to process variations, the worst case delay varies by about 25% around the mean values. Cross-coupling plus process variation increase the delay from normal to the worst case maximum by almost 85% (from 217.3ps to 400ps); the deviation between the minimum and the maximum delay is 234.5ps (from 165.5ps to 400ps), i.e. 108% of the nominal delay.

#### 3.2.2 Crosstalk Pulse

The height of the crosstalk pulse is determined for the case where A has a falling transition while  $V_{in}$  is stable at 0V. Table 2 shows the values of the pulse height. For worst case process values, the pulse height is 43% larger than its nominal value.

These examples shows that there are significant variations about the mean values for crosstalk pulse and delay due to process variations. The noise margin in a typical circuit may not be large enough to tolerate the effects of both crosstalk and process variations.

## IV. New Design Validation and Test Issues

### 4.1 Design Validation for Crosstalk Noise

In high speed circuits, signal timing is an important issue for correct circuit operation. From previous discussion, crosstalk can have a significant impact on signal delay and even result in erroneous circuit operation. For example, consider a clocked D flip-flop. Due to crosstalk effects, a transition on D may arrive early and/or the clock edge may arrive late. These may cause hold-time violations. Also, if the transition on D arrives late and/or that on the clock arrives early, a setup-time violation may occur. Either of these scenarios can either cause meta- stability or the flip-flop to go into the wrong state.

Due to the high complexity of crosstalk analysis, the development of a methodology to identify pairs (or, in general, sets) of lines where crosstalk noise is likely to exceed the noise margin or timing is essential to any practical validation methodology. The results presented above provide a methodology to identify such pairs of lines by showing that the severity of crosstalk depends on three main factors, (a) the circuit parameters associated with the coupled lines, (b) the nature of inputs that can be applied to these lines, and (c) the nature of the circuit driven by them. The last factor has been discussed in some detail in [21] where it is shown how certain properties of the circuit driven by the coupled lines determines the type

of crosstalk effect, e.g., pulse or delay, and for each type of effect, the characteristic of the effect that in turn determine if an error can occur. In this context, the results of our analysis can be used to identify pairs of circuit lines where crosstalk may be significant and hence should be analyzed explicitly. Our results show that the amplitude of the crosstalk pulse is proportional to the coupling capacitance between the lines and the ratio of the strengths of the drivers driving them (not shown in this paper), and inversely proportional to the load capacitance on each line. These facts can be used to identify candidate pairs of lines for crosstalk analysis. Also the maximum *amplitude* of the crosstalk pulse decreases rapidly with an increase in the rise/fall times of the inputs, while the energy of the pulse is virtually independent of this time. If the rise/fall time of the input to a candidate pair of lines is known to be large, then it may not be necessary to analyze the effect of crosstalk, depending on which of these two characteristics of the pulse is likely to cause an error in the circuit driven by the lines.

We have also shown that process variations have a significant impact on the severity of crosstalk. Hence, parts of circuits where crosstalk does not cause errors for nominal values of parameters can operate erroneously for other parameter values in the *design envelope*. The correctness of a design at all points in the design envelope is verified by validating the circuit at various *design corners*, i.e., extreme combinations of parameter values where the design is likely to fail. However, the design corners that are commonly used during validation do not represent the combination of parameter values where the severity of crosstalk is maximized [21]. Our analysis helps identify new design corners where the candidate lines must be simulated to ensure correct operation even in the presence of crosstalk. For example, we have shown that crosstalk interference is proportional to the mutual capacitance, ratio of strengths of drivers driving the coupled lines, and inversely proportional to the load capacitance on each line. This is obviously different from the most commonly used *fast* and *slow* design corners.

#### 4.2 Test Vector Generation

Even if a design is found to fail at some extreme points in a design envelope, a circuit may not be redesigned, especially if redesign would make the attainment of design objectives impossible. In such a case, the resulting circuit will typically be guaranteed to operate at a vast majority of points within the envelope, but not all. For such a design, each manufactured device must be tested to ensure that it works correctly. The above results specify conditions that a test must satisfy to detect errors caused by crosstalk. For example, it shows that a sequence of two patterns must be applied to cause nearly simultaneous transitions in opposing directions to invoke

worst case crosstalk slowdown. The resulting slowdown must then be propagated along paths with low delay slacks to circuit outputs. The application of a test sequence that satisfies these conditions will identify devices with excessive crosstalk slowdown. (Note that traditional path delay testing tests for excessive delay along logical paths in the circuit, while here excessive delays are caused by coupling between logically unrelated paths.) In a similar manner, the above results provide conditions that a sequence of patterns must satisfy to detect errors caused by other crosstalk effects.

Fig. 12 shows an example of test pattern generation for crosstalk pulse. Assuming that we want to create a positive pulse at V, at least a or b must be set to 1 to provide a constant low at V. However, to decrease the total pulling resistance to GND, only input a is set to 1. Since a sharp transition on A is preferred, both c and d are assigned rising transitions. In addition to the pulse excitation, to propagate the resulting pulse through the next stages, proper values must be set on side fan-in's of each gate, i.e. values for e, f, g must be set accordingly. Backward implication of these conditions will give rise to a sequence of test patterns.

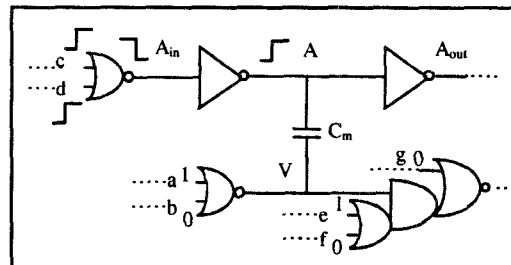


Figure 12 Example circuit for test vector generation

## V. Conclusions

The objective of this paper is to develop a general methodology to analyze crosstalk in order to obtain insight into effects that are likely to cause errors in high speed VLSI circuits. We studied crosstalk due to capacitive coupling between a pair of lines. Closed form equations quantifying the dependence of the pulse attributes on the values of circuit parameters and the rise time of the input transition were derived. These expressions show that the severity of the crosstalk pulse is directly proportional to the coupling capacitance and the ratios of the strengths of the drivers driving the two line. Further, it is shown that while the maximum amplitude of the crosstalk pulse diminishes rapidly as the rise/fall time of the input increases, the energy of the pulse is almost independent of the input rise/fall time for a realistic range of rise/fall time values. We also studied how crosstalk causes speedup/slowdown when signals change in the same/opposite directions. Qualitatively, the dependence of

slowdown and speedup on circuit parameters is similar to that observed for crosstalk pulse. Also, it was found that the faster the transition at A, the greater is the slowdown at V. Finally, it was found that crosstalk slowdown is the highest when both inputs have simultaneous transitions; the magnitude of slowdown decreases as the skew between the input transitions increases.

The crosstalk effect was shown to be significantly aggravated by variations in the fabrication process. The significance of the process variations necessitates the identification of new design corners for validation, some of which have been presented here. Finally, the results of our analysis provide conditions that must be satisfied by a sequence of vectors used for validation as well post-manufacturing testing.

For 0.18 $\mu$ m technology, the aspect ratio of and spacing between wires are such that the capacitance between metal wires on the same layer exceeds the interlayer capacitance. Since there is a high likelihood of having long parallel wires on the same layer, we believe the effects of crosstalk will be more severe.

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