Crosstalk Issues in Deep Sub-Micron VLSI Circuits: DSM issues in Detail

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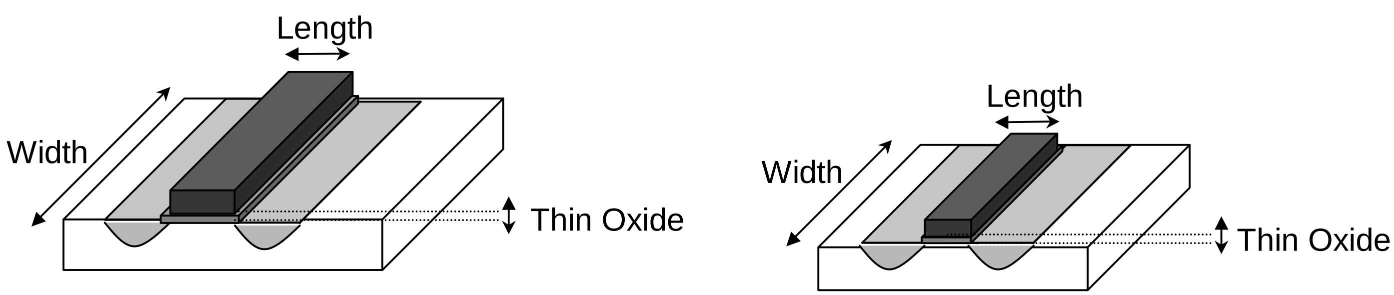
Session 3

What is Deep Sub-Micron?

- VLSI Technology Scaling
- Moore's Law



- Other Factors: Supply Voltage, densities

Different Scaling Techniques

- Constant Field Scaling (electric field is constant):
  1. All dimensions, including vertical
  2. Device voltages
  3. Concentration densities
- Constant Voltage: Voltages are constant, electric field is increased
- Lateral: Widths are not scaled

DSM Effects

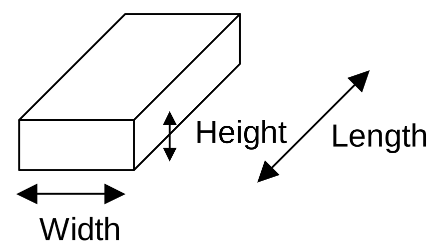
- Interconnect Delay
  - Gate Delay vs. Wire Delay is increased, Wire Delay is dominant in DSM
- Crosstalk Noise and Delay Unpredictability
- Reliability
  - Electro Migration (EM)
  - Current Density
- Power Consumption

Interconnect Delay

- Example:
  - 1mm Metal 1, Technology 0.5 uM, RC delay = 15ps
  - 1mm Metal 1, Technology 0.1 uM, RC delay = 340ps

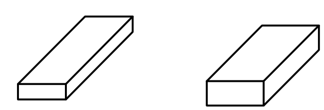
- Source: Wire resistance

$$R = \rho \times \frac{l}{A}$$



$$R_{Scaled} = \rho \times \frac{(1/\alpha)l}{(1/\alpha^2)A} = \alpha R_{Old}$$

- Solution:
  1. Slower rate for Height Scaling
  2. Use better Conductors, e.g: Cupper



Comparison of Solutions

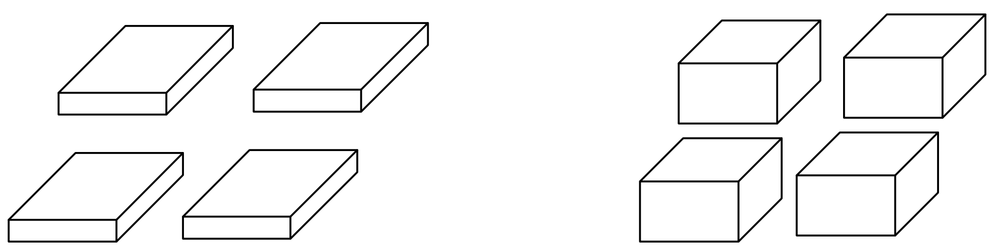
- Cupper Resistivity is 30% Less than that of Aluminum
  - Another Key Advantage: Electro Migration (EM) Cupper is heavier, EM Life time of cupper is 100 longer that of Aluminum
- Increased wire to wire (Horizontal) capacitance due to isolator thickness (Same Layer wires):

$$C = ke_0 \times \frac{A}{d}$$

- Solution: Use Low dielectric material as insulator
  - Instead of Sio2 (k=3.9) Use material of k=3.1: gate delay is decreased by 39% power is reduced by 47%
  - Goal is k=1 (air) material is xerogels

Crosstalk Noise

- High Aspect Raito Lines: Increased coupling Capacitance
- With AR>1: More same layer capacitance than different layer: $C = ke_0 \times \frac{A}{d}$
- Example: Event at 0.25uM technology, 70% of wire capacitance is for wires in the same layer



Effect of Coupling Capacitance

- Total Capacitance Seen: $C = C_{Load} + C_{Coupling}$
- Miller Effect: Capacitance is dependent to Signal Activity
    1. Static Timing Analysis is difficult
    2. Delay are unpredictable
- Delay Deterioration: Capacitance seen by a gate is not constant
- Signal Integrity: A static signal is perturbed by switching activity on adjacent signals

Crosstalk Cont.

- Accurate Design Rules
  - Design Rules for Manufacturing
  - Design Rules for Crosstalk
- Define critical line length
- Re-Design (architectural modifications)
- Re-route (adjacent critical signals)

Power

- Power: Dynamic Power, Static Power, Short Circuit Power
- Dynamic Power Formula: $P = C \times V^2 \times f$
  - Increasing capacitance means increase in Power
  - Smaller size, faster devices, high frequency, high power
  - Dynamic power increases proportionally to chip area
  - Solution: Scale down voltage

- Static Power: $P_{Static} = I_{Static} \times V_{DD}$ $\quad I_{Static} = 10 \times W \times 10^{\frac{-V_t}{95_{mv}}}$
  - Exponential relation between Static current and threshold voltage V_t
  - Threshold voltage is scaled down to boost device performance
  - As a result Static power inreases

Power Cont.

- Example:
  - Circuit is a core of 50,000 Gates
  - Static Power density increases 2500 times from 0.25 uM to a 0.1 uM technology
  - Solution: Use multi V_t technology, high V_t for power sensitive parts, low V_t for speed critical parts.

- Short-Circuit Power: It depends on rise/fall time of signals
  - Rise/Fall time is being decreased as we go in DSM

- It is manageable and remains less than 20% of dynamic power

Summary

- VLSI Scaling
- Plunge into DSM
- Problems: Delay, Power, Crosstalk
- Solutions: New Materials, New design rules, Redesigning, Re-routing
- All solutions are before manufacturing or during it