

Homework Set 6
EECE2412: Electronics – Spring 2013
Due Wednesday, 3 April 2013

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Complete the following problems from Hambley's book

1 NMOS Transistor Design

Problem 5.7 & Comment on the effect of varying λ .

2 Triode Operation

Problem 5.13

3 Fixed– Plus Self–bias Design

Problem 5.24

4 Fixed– Plus Self–bias Design 2

Problem 5.25

5 CCD

A CCD is created with square pixels measuring $7\ \mu\text{m} \times 7\ \mu\text{m}$ and contains an oxide layer that is 250 nm thick with an $\epsilon = 3.8\epsilon_0$. the oxide layer has a maximum potential of 1 volt. Answer the following questions:

- What is the capacitance per unit area?
- What is the full well capacity?
Remember, The full well capacity is the maximum number of electrons that can be stored in the pixel. It is important because it affects the signal to noise ratio.
- If you utilized these pixels to build a square, 1–megapixel CCD camera, what would its dimensions be?

6 Logic Gate

Figure 1 illustrates some BJT logic gate. The DC signal for inputs 1 and 2 are binary and can be either 0 or 5 volts. Answer the following questions:

- There are 4 unique voltage combinations for inputs 1 and 2. What is the value of V_{out} for each of these combinations?
- When V_{out} is high, what is the current traveling through R_1 ?
- When V_{out} is low, what is the current traveling through R_1 ?
- If there is no voltage is applied to Input 1 or 2, what is V_{out} ?

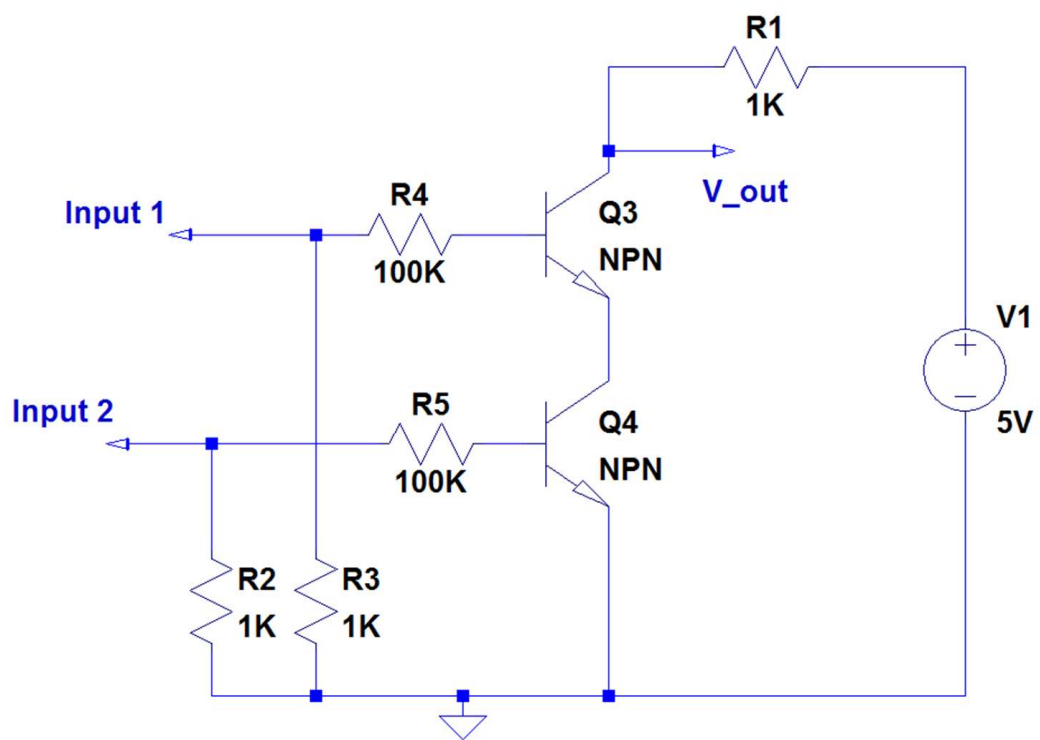


Figure 1: BJT logic gate