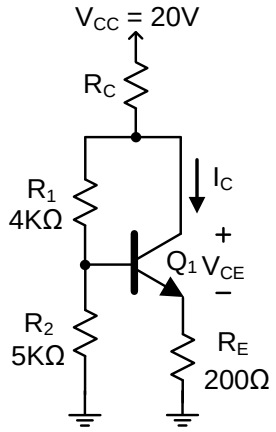
EECE 2412 – Homework 6 – Fall 2016

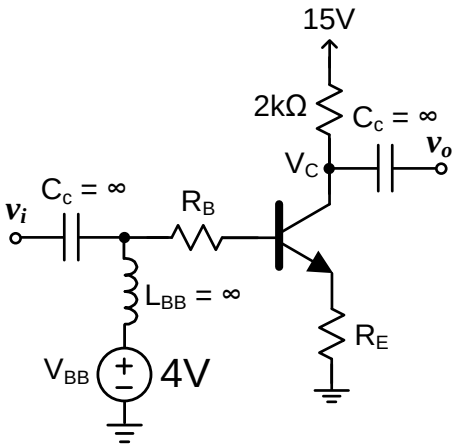
Due: Wednesday, November 2, 2016

1) Problem 4.20 on page 281 of the textbook (Allan R. Hambley, Electronics, 2nd edition). Provide the values of V_{CE} and I_B for the minimum and maximum Q-points. Is the output voltage signal at the collector terminal clipped?

2) The bipolar junction transistor in the circuit below has a β value of 80. Assume $|V_{BE}| = 0.5V$ in this DC analysis.
   a) Determine the value of R_C that establishes a collector current of $I_C = 4mA$
   b) Calculate the corresponding value of V_{CE} for the R_C resistance value in part a).



3) Consider the circuit below.
   a. DC analysis: Assume that a DC operating point (Q-point) value for the collector current (I_C) between 4mA and 5mA is required to ensure proper ranges for small-signal parameter values, and that β of the BJT can vary between 100 and 300. (This implies that I_C should be 4mA when β = 100, and equal to 5mA when β = 300 to guarantee: $4mA \leqslant I_C \leqslant 5mA$). Find values for R_B and R_E that satisfy the requirements.
   b. Small-signal parameter calculation: Calculate the small-signal parameters g_m, r_π, and r_{ce} at room temperature (300K), assuming that the Early voltage (V_A) is 100V (refer to the slides from lectures 18 and 19). Use the max. I_C and min. I_C cases from part a) in the calculations to determine the expected ranges of the small-signal parameter values.
   c. Draw the small-signal equivalent circuit using the hybrid-π model that includes the parameters from part b). FYI: This is the circuit that you would use for AC analysis at mid-band frequencies (gain, input/output impedance, etc.).
   d. Setup the simplified DC circuit (in which the capacitors and the inductor are excluded appropriately) from part a) with your calculated values in PSPICE, and simulate it to verify your results. Use the procedure described in homework 5 to model the BJT with the Qbreakn device model and the specified values of β. Submit the schematics that show the collector current values for the min. and max. cases in part a).
   e. Sweep the DC bias voltage at the base (V_{BB}) of the BJT from 0 to 15V using the Q2N2222 transistor model for the BJT. Plot the DC transfer characteristic curve at the collector (V_C vs. V_{BB}), and label the voltages at which an output signal at the collector would begin to clip. Submit the labeled plot. What is the maximum peak-to-peak output voltage swing that can be achieved when the Q-point is in the middle of the linear range?



4) Consider the two-supply bias arrangement shown in the figure below using ±3V for $+V_{CC}$ and $-V_{EE}$. Assume that it is required to design the circuit so that I_C = 3mA while V_C = 0V (placed midway between $+V_{CC}$ and $-V_{EE}$).
   a) With β = ∞ (simplified analysis for estimation of the conditions with very high β values), what values are required for R_E and R_C?
   b) If the BJT is specified to have a minimum β of 90, find the largest value for R_B that still ensures a voltage drop across R_B equal to one-tenth of the voltage drop across R_E.
   c) What standard 5%-resistor values would you use for R_B, R_E, and R_C? Make your selection such that the resistance values are somewhat lower than the calculated values to allow for the effects from low β.
   d) For the values you selected in part c), calculate I_C, V_B, V_E, and V_C for β = ∞ and for β = 90.
   e) Simulate your design in PSPICE to check it with the values from part c). Use the procedure described in homework 5 to model the BJT with the Qbreakn device model and a specified value of β. Run one simulation with β = 90 and another one with β = 400, and submit the print outs of the schematics with displayed DC voltages and currents.