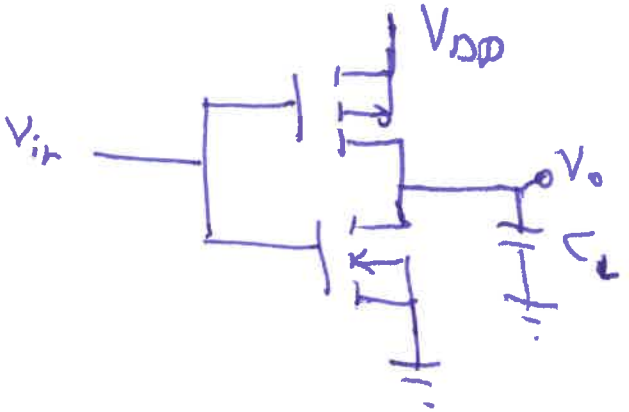
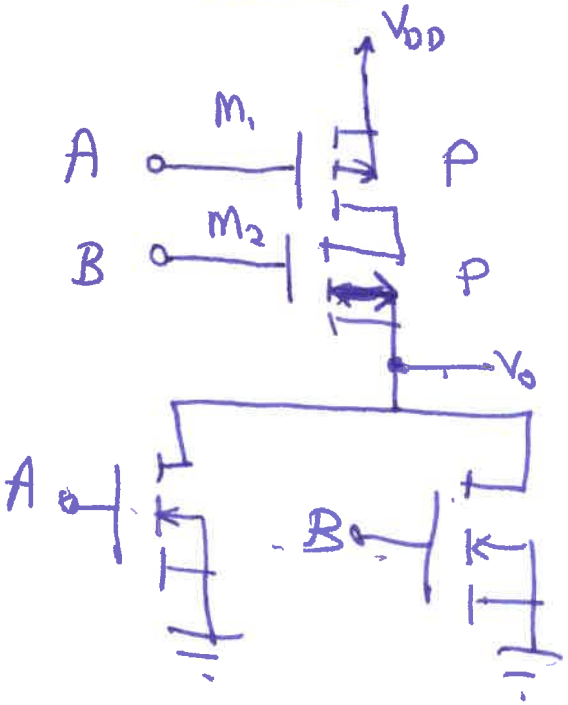
Mon 4 Dec 2016

Announcements:
- HW 10 wed
- Clock Blackboard
- Review wed
- Watch website
- Email Re Final conflicts

Reminder: Inverter



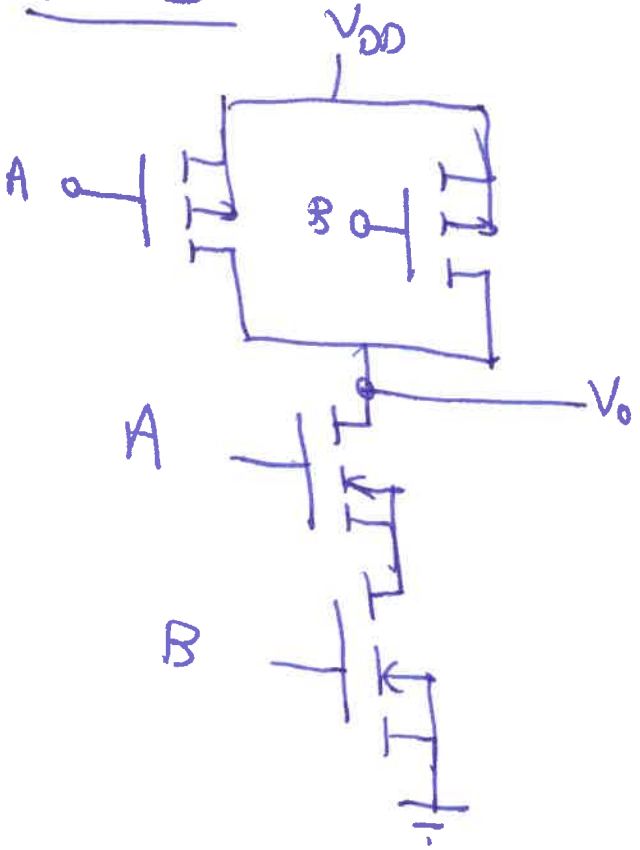
NOR



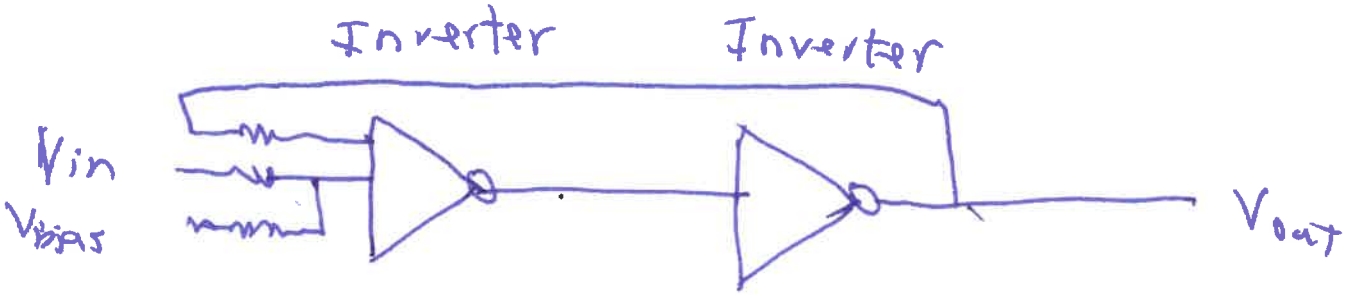
A	B	OUT
H	H	L
H	L	L
L	H	L
L	L	H

Not (A or B)

NAND



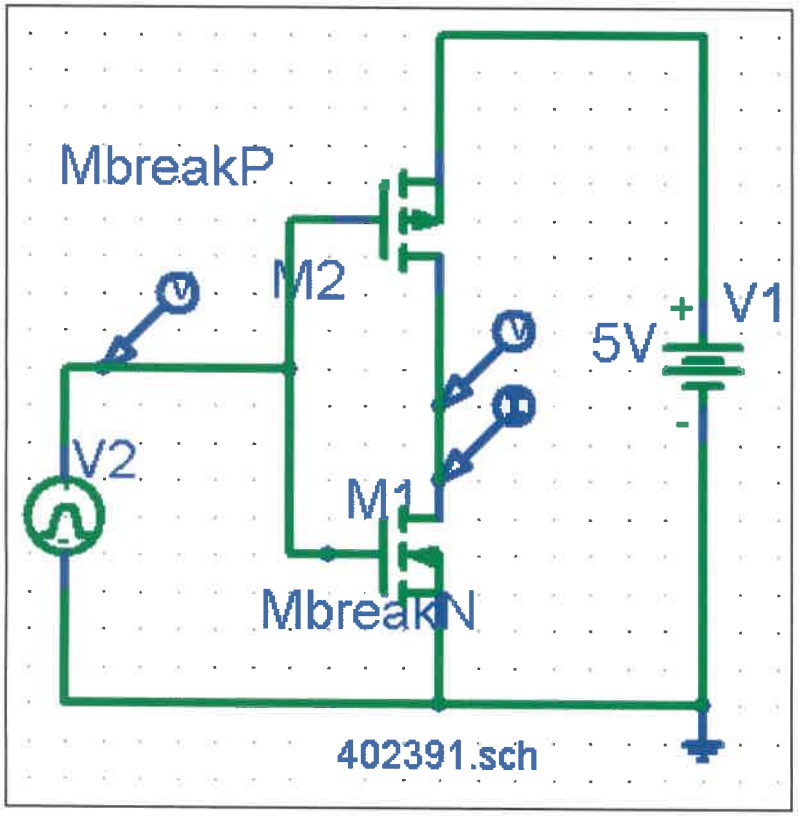
Memory

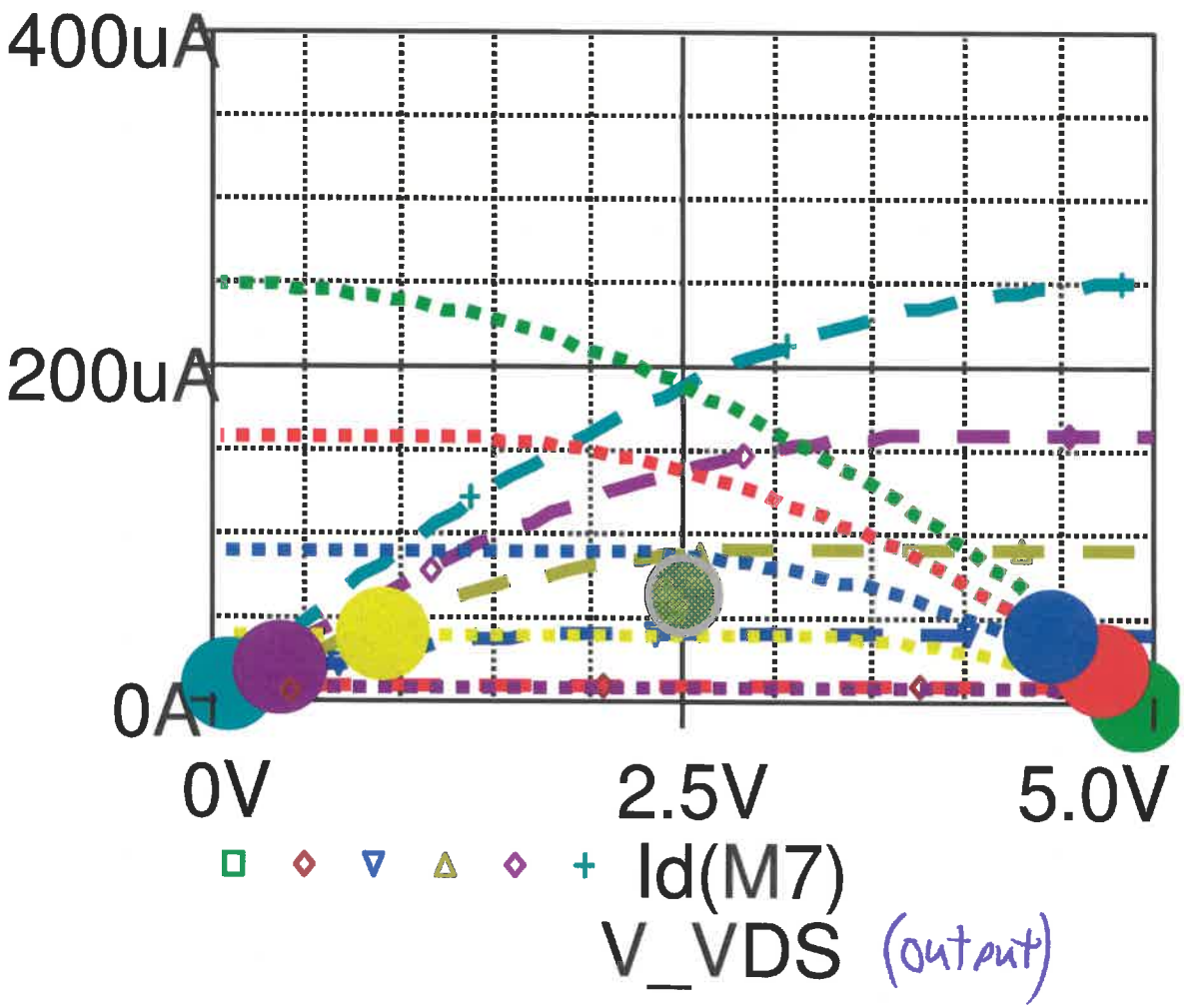


5	0	5
0	5	0

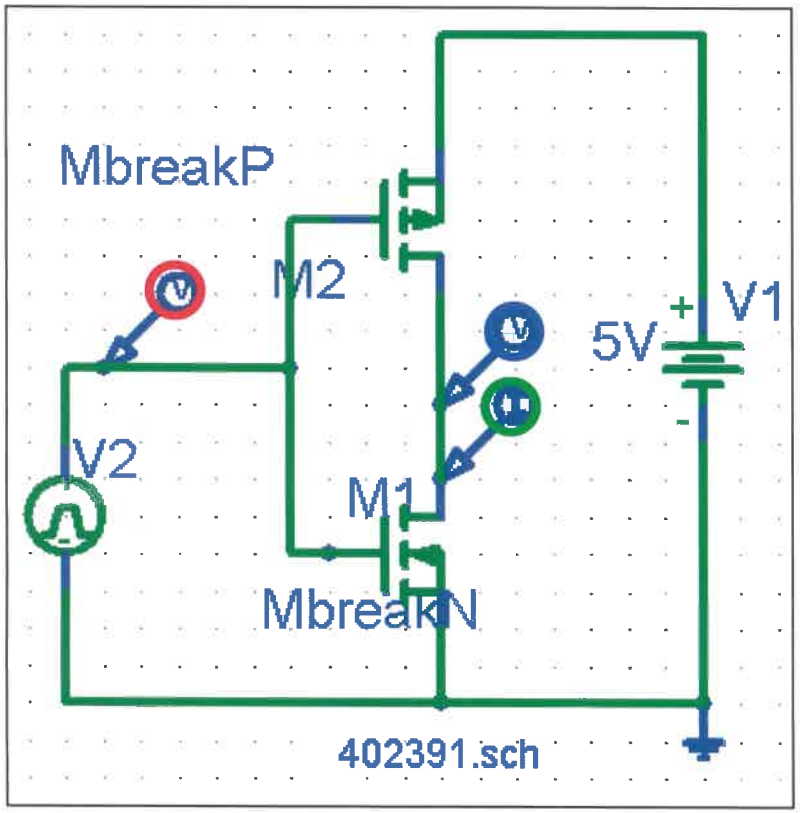
Non linearity
Positive feedback } — Bistable system

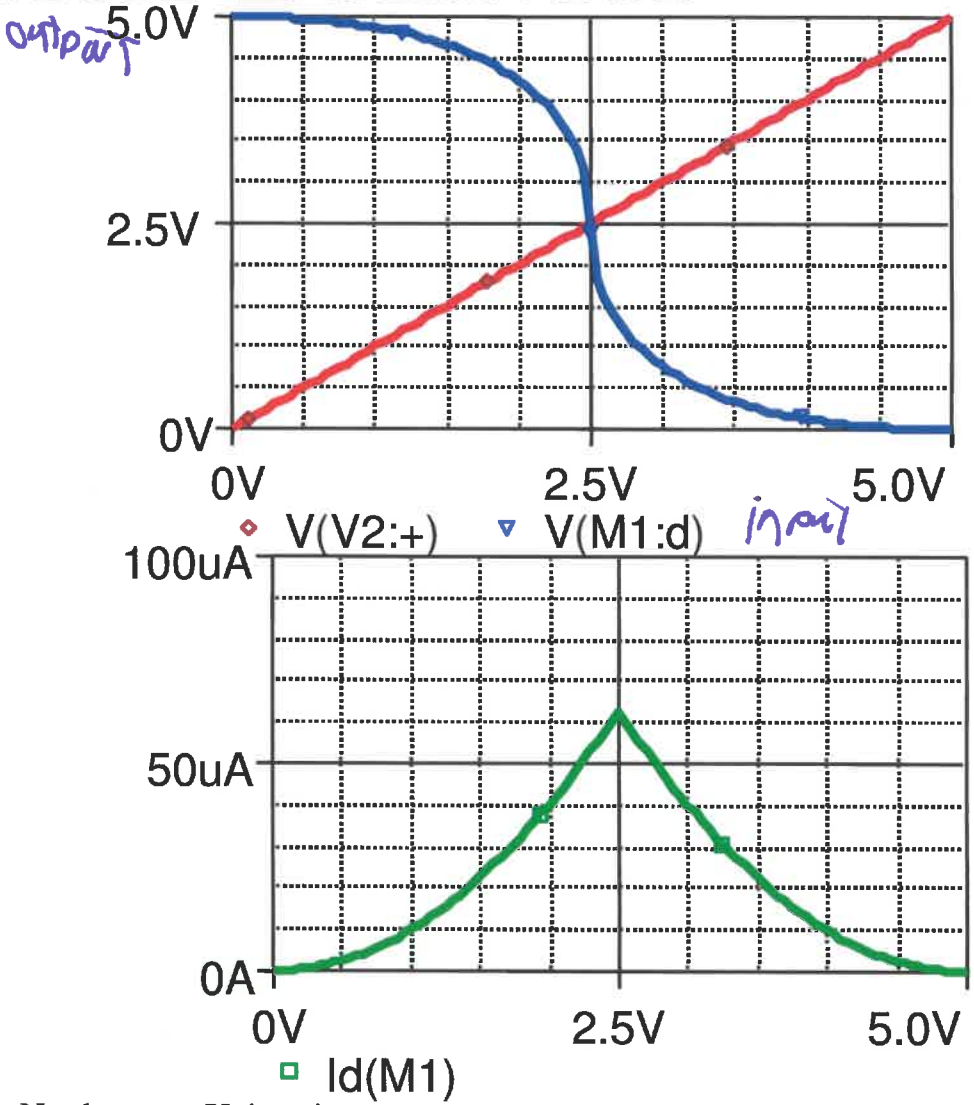
CMOS Logic Inverter



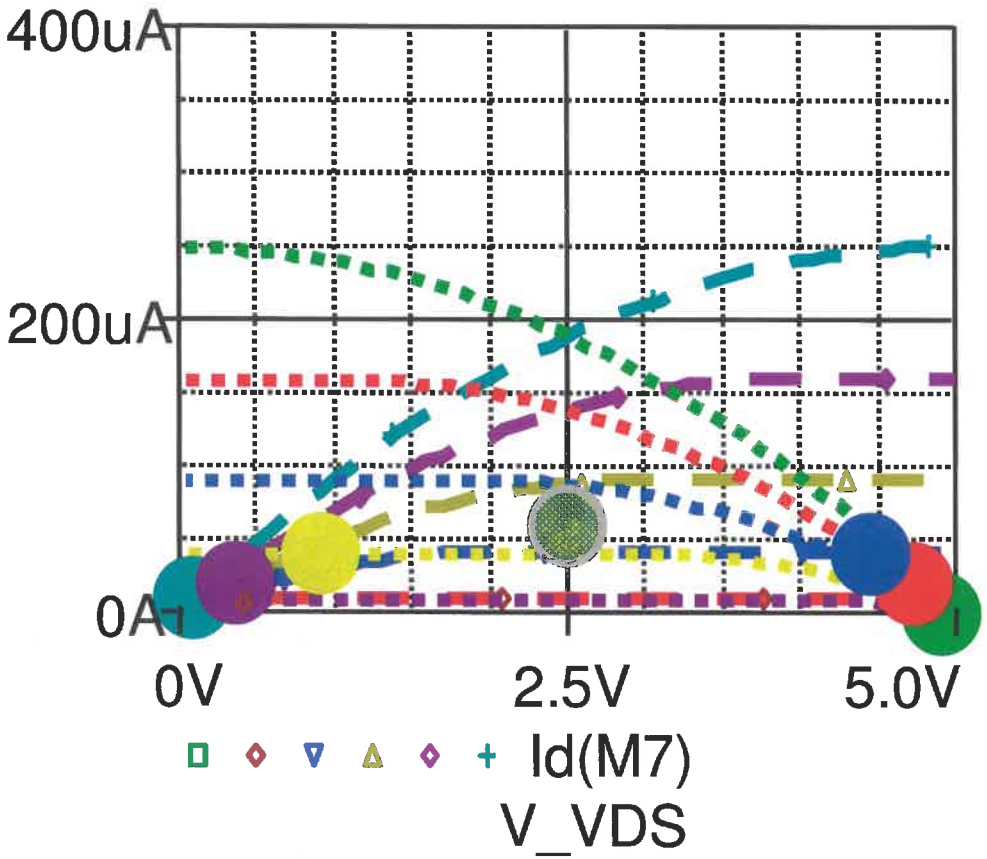


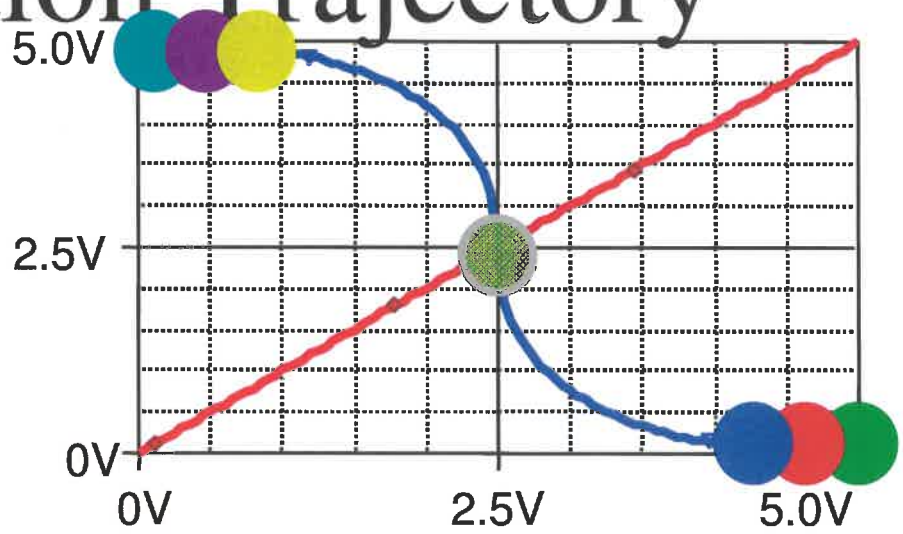
CMOS Inverter Behavior

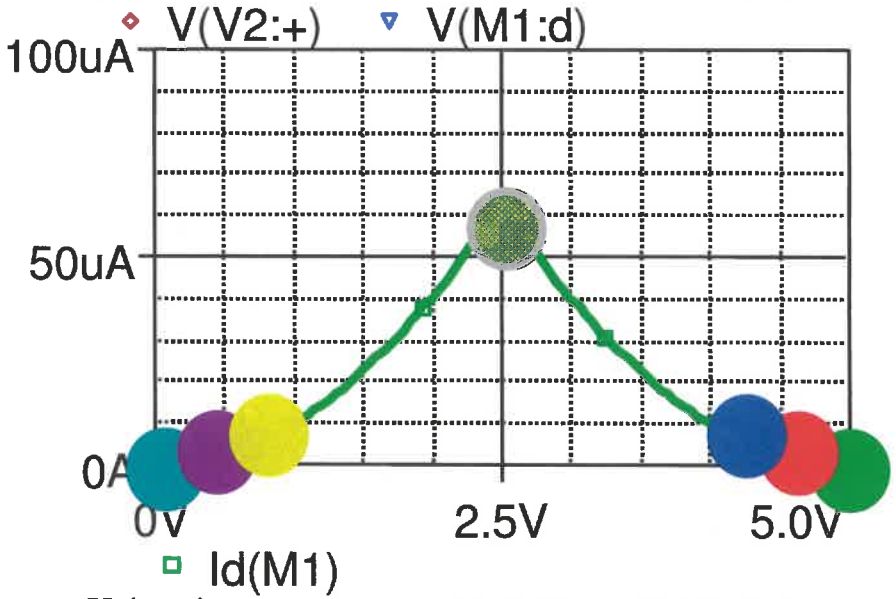




Inverter Transition Trajectory



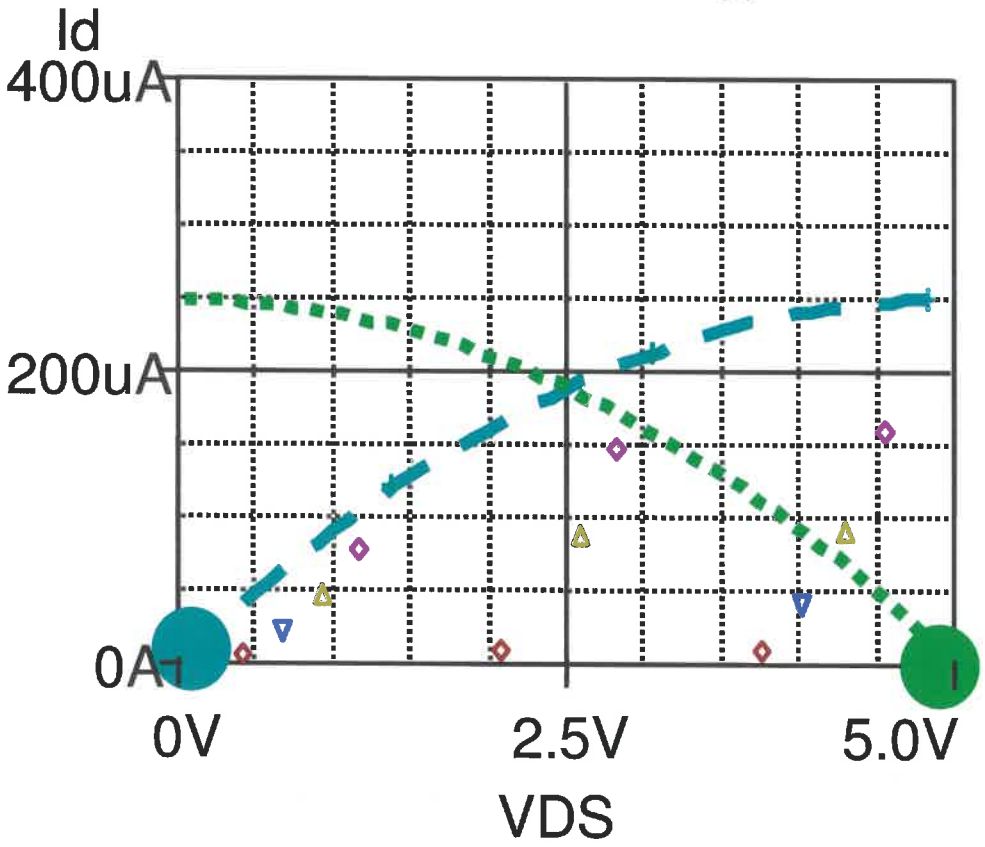




FET Logic Characteristics

- Wide Voltage Swing (0 to 5 V)
  - Good noise margins
- Near Zero Power Consumption (static)
- Low Output Resistance
  - Can Drive Large Loads
  - Low Noise
- High Input Resistance

Output Resistance



- Transistor with High v_{GS} $(=v_{DD})$is in Triode
  - Steep IV Slope=Low R

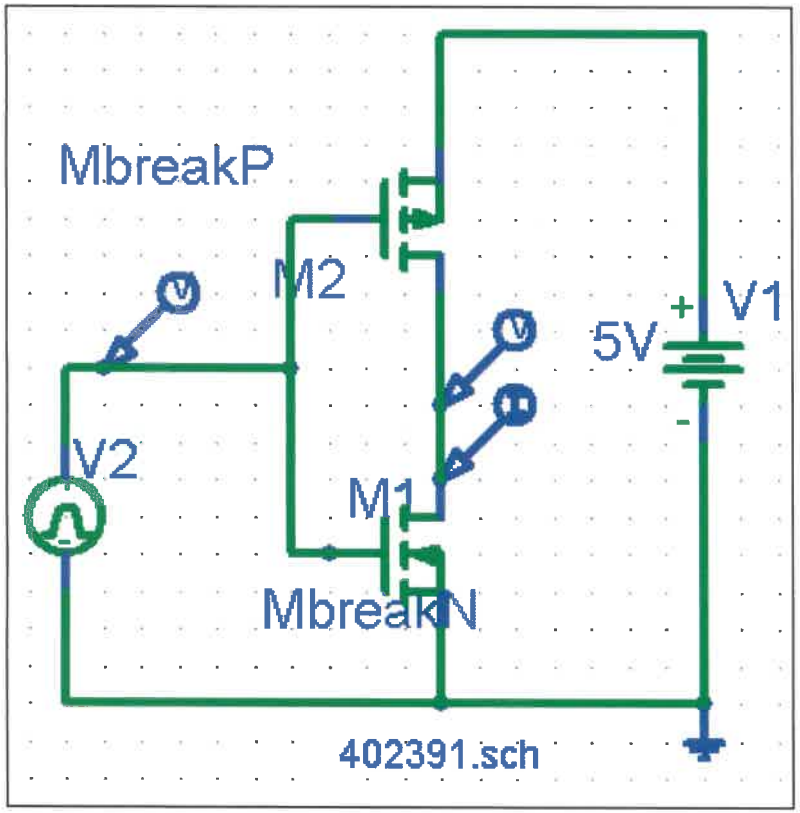
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[\left(v_{GS}-v_{thr}\right)V_{DS}-\frac{1}{2}v_{DS}^2\right]$$

$$\frac{di_D}{dv_{DS}} = \mu_n C_{ox} \frac{W}{L}\left[\left(v_{GS}-V_{thr}\right)-v_{DS}\right]$$

$$\frac{di_D}{dv_{DS}} \approx \mu_n C_{ox} \frac{W}{L}\left[\left(v_{DD}-V_{thr}\right)-0\right]$$

$$R_{DS} \approx \frac{1}{\mu_n C_{ox}\frac{W}{L}\left(v_{DD}-V_{thr}\right)} \approx \frac{1}{20\times10^{-6}\left(\text{A/V}^2\right)\times50\times5\text{V}} = 200\,\Omega$$

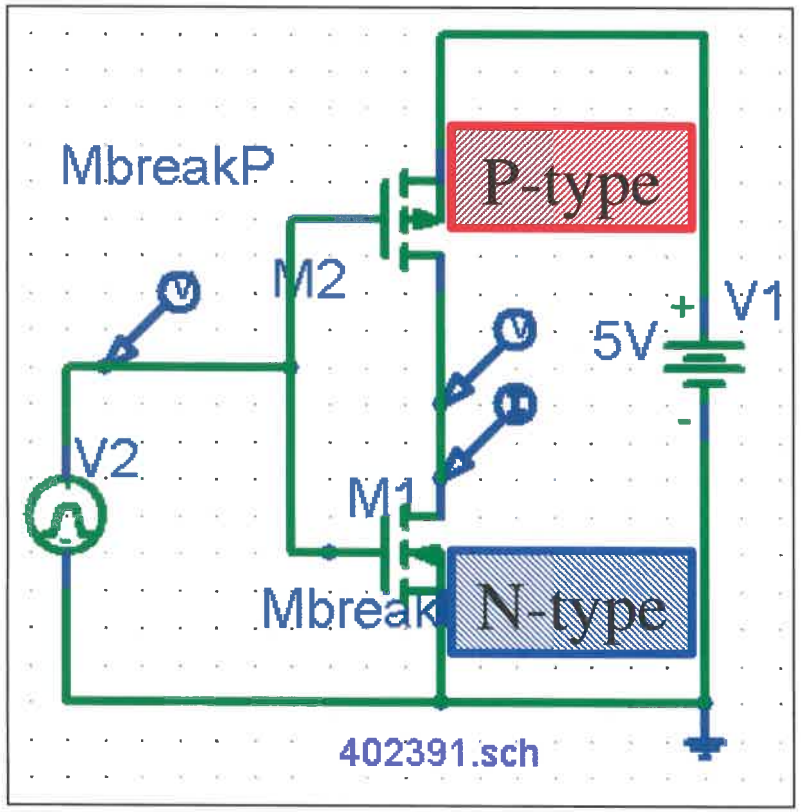
Input Resistance



- Input to Gates Only
  - Infinite Resistance

3 cases: Triode + Sat
sat + Triode
sat + sat

Equations for FET Logic (1)



Triode $v_{out} < v_{in} - V_{thr}$

$$i_{DP} = \mu_p C_{ox} \frac{W}{L}\left[\left(V_{DD} - v_{in} - |V_{thr}|\right)\left(V_{DD} - v_{out}\right) - \frac{1}{2}\left(V_{DD} - v_{out}\right)^2\right]$$

Saturation

$$i_{DP} = \mu_p C_{ox} \frac{W}{L} \frac{\left(V_{DD} - v_{in} - |V_{thr}|\right)^2}{2}\left(1 + \frac{V_{DD} - v_{out}}{V_A}\right)$$

Triode $v_{out} > v_{in} + |V_{thr}|$

$$i_{DN} = \mu_n C_{ox} \frac{W}{L}\left[\left(v_{in} - V_{thr}\right)v_{out} - \frac{1}{2}v_{out}^2\right]$$

Saturation

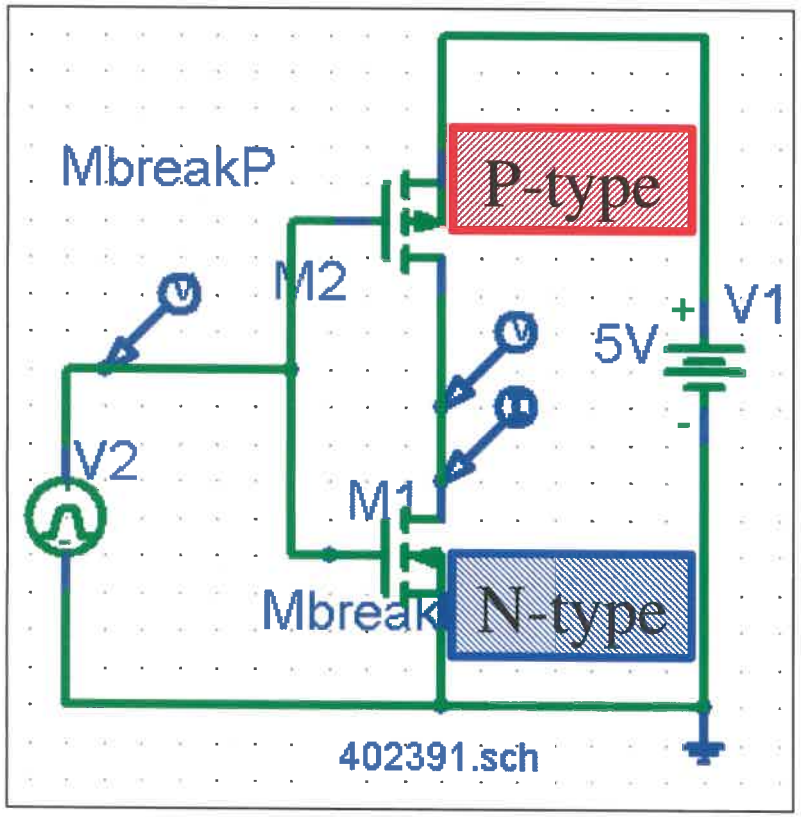
$$i_{DN} = \mu_n C_{ox} \frac{W}{L} \frac{\left(v_{in} - V_{thr}\right)^2}{2}\left(1 + \frac{v_{out}}{V_A}\right)$$

Now, Assume $\mu_n = \mu_p$ ×2

Also Same ~~W/L~~ and V_{thr}

$\left(\frac{W}{L}\right)_n = \frac{1}{2}\left(\frac{W}{L}\right)_p$

Equations for FET Logic (2)



Both in Saturation

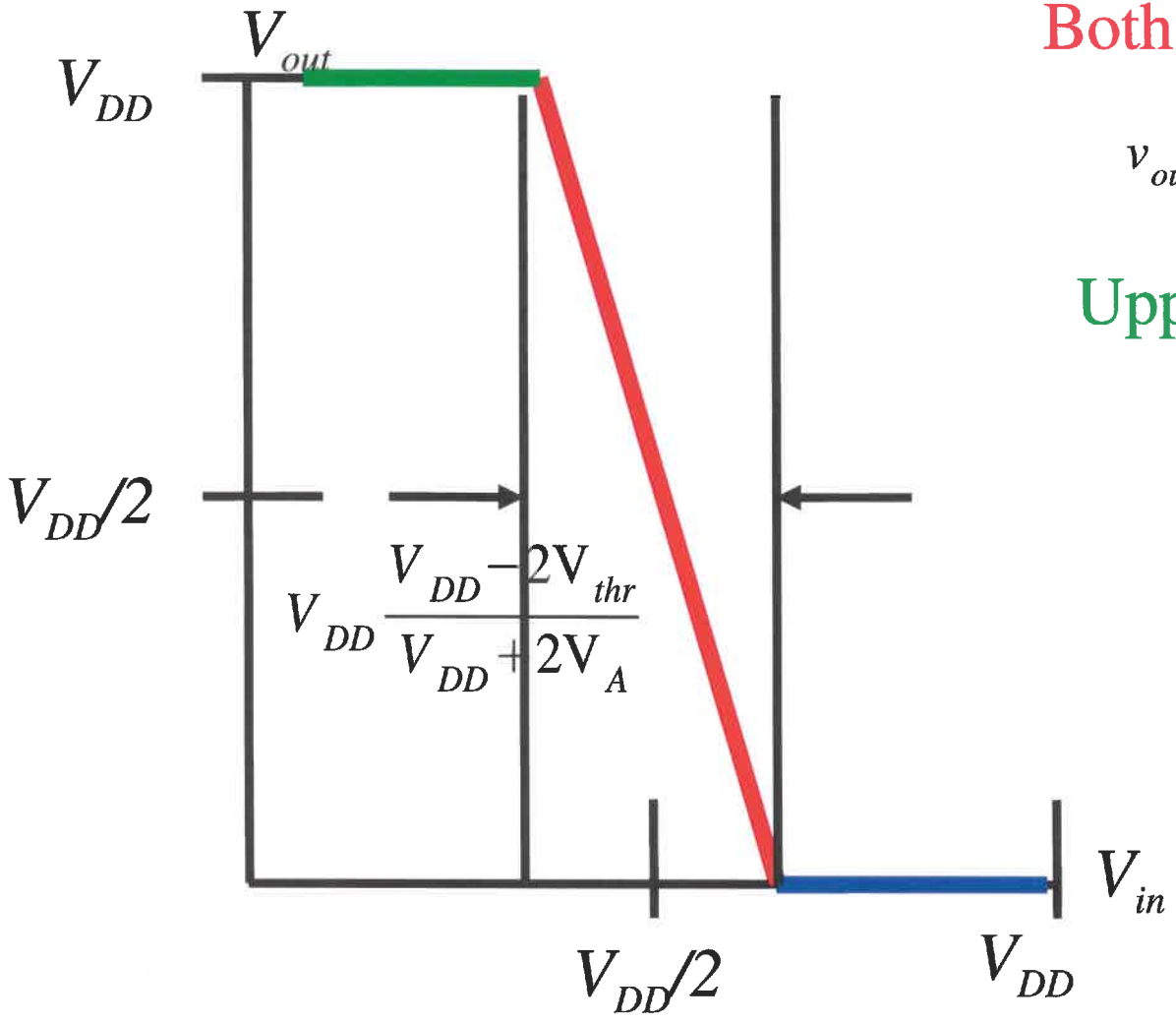
$$i_D = \mu C_{ox} \frac{W}{L} \frac{\left(V_{DD} - v_{in} - |V_{thr}|\right)^2}{2} \left(1 + \frac{V_{DD} - v_{out}}{V_A}\right)$$

$$i_D = \mu C_{ox} \frac{W}{L} \frac{\left(v_{in} - V_{thr}\right)^2}{2} \left(1 + \frac{v_{out}}{V_A}\right)$$

$$\frac{\left(V_{DD} - v_{in} - |V_{thr}|\right)^2}{2} \left(1 + \frac{V_{DD} - v_{out}}{V_A}\right) = \frac{\left(v_{in} - V_{thr}\right)^2}{2} \left(1 + \frac{v_{out}}{V_A}\right)$$

Trust Me $$v_{out} = \frac{V_{DD}}{2} - \frac{V_{DD} + 2V_A}{V_{DD} - 2V_{thr}} \left(v_{in} - \frac{V_{DD}}{2}\right)$$

Equations for FET Logic (3)



Both in Saturation

$$v_{out}=\frac{V_{DD}}{2}-\frac{V_{DD}+2V_A}{V_{DD}-2V_{thr}}\left(v_{in}-\frac{V_{DD}}{2}\right)$$

Upper Limit $v_{out}=V_{DD}$

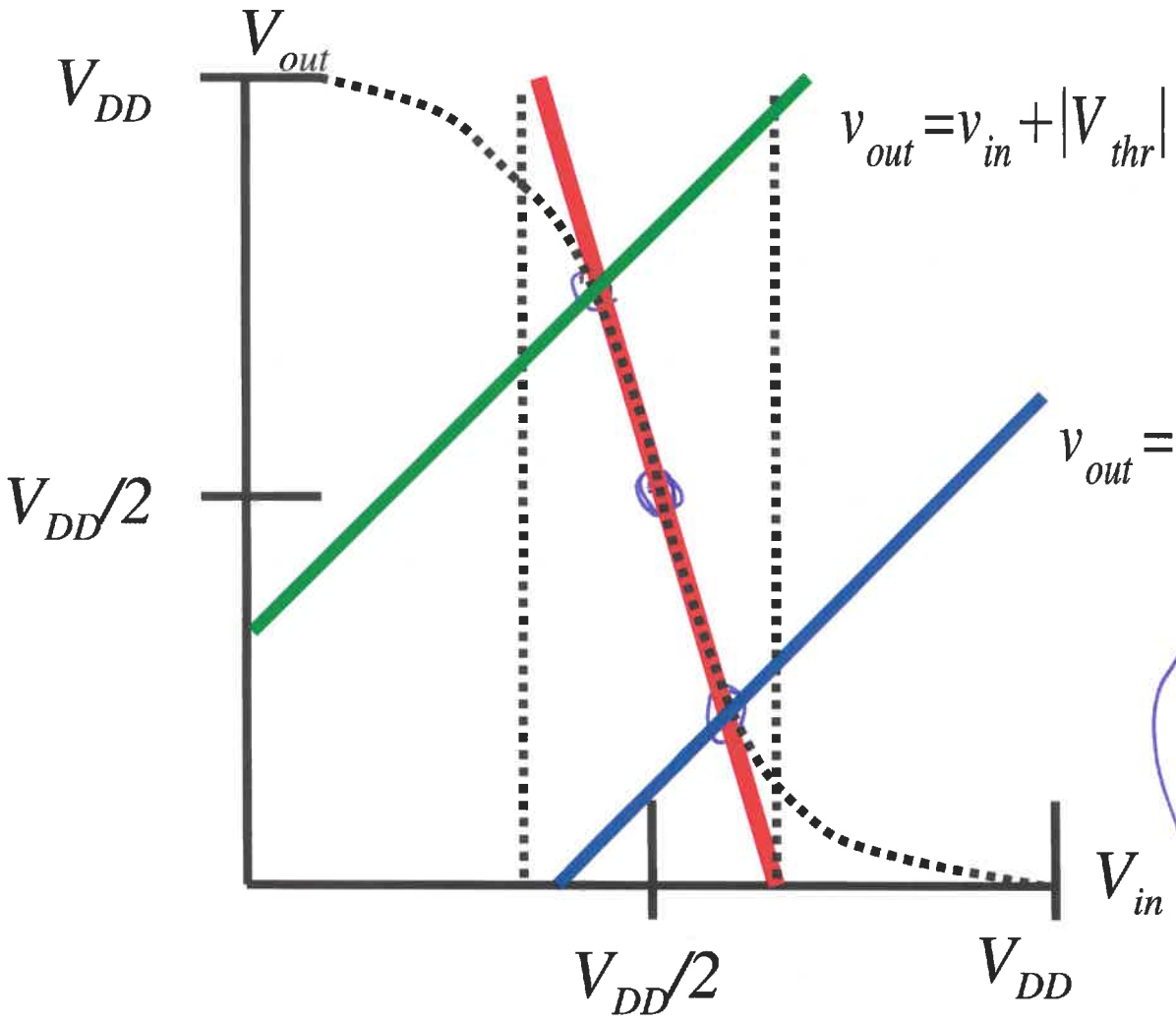
$$\frac{V_{DD}}{2}=-\frac{V_{DD}+2V_A}{V_{DD}-2V_{thr}}\left(v_{in}-\frac{V_{DD}}{2}\right)$$

$$v_{in}=\frac{V_{DD}}{2}-\frac{V_{DD}}{2}\frac{V_{DD}-2V_{thr}}{V_{DD}+2V_A}$$

Lower Limit $v_{out}=0$

$$v_{in}=\frac{V_{DD}}{2}+\frac{V_{DD}}{2}\frac{V_{DD}-2V_{thr}}{V_{DD}+2V_A}$$

Regions of Operation



It is left as an exercise for the student to calculate the curve in the other two regions.