EECE2412— INTRODUCTION TO ELECTRONICS— Spring 2017

Syllabus

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OFFICE HOURS:	TBD Feel free to email questions as well.

TEXT:	Hambley, Allan R. *Electronics*, Second Edition, Prentice–Hall.

OTHER RESOURCES:	For PSPICE, you can download a student version from http://www.electronics-lab.com/downloads/schematic/013/ There will be some use of Matlab or other software for calculations. I recommend Matlab, but I don't insist on it. I will put pointers to other resources on the class website.

LOCATION:	309KA

12198syl:1 — 9 December 2016

TIME:	Mon, Wed, Thu, 4:35 — 5:40 PM

LAB:	As scheduled, in 9HA EECE2413, Electronics Lab. This lab must be taken simultaneously since the material in the lab supplements the lecture. Note that students from the two lectures sections are intermixed in the labs.

READING:	Reading is to be done before the start of the week. When I lecture, I will assume that you have read the related material.

COURSE DESCRIPTION:	In this course you will learn about four types of electronic devices: op–amps, diodes, bipolar junction transistors (BJTs), and metal-oxide-semiconductor field effect transistors (MOSFETs). You will learn how to design and analyze useful electronic circuits (such as amplifiers and logic circuits) using these components.

GRADING:	20 % on homework (Equal weight on best $n-1$ of n assignments where $n \approx 10$) 50 % on 2 mid–term exams 30 % on final exam. Please discuss questions regarding homework grading first with the TA and then with the instructor. Discuss questions regarding exam grading with the instructor.

HOMEWORK:	Homework is typically given on Thursday and due at the beginning of class the following Thursday. Be sure to show all steps. Simply writing the answer is not acceptable. Keep a photo of your homework for your own use while grading is being done. Working together is acceptable, and even encouraged, on homework, BUT the work that you submit must be your own (no copies of the group's solution!) If you are working with a group, make certain you understand every part of your solution. If you work in a group, indicate the names of members of the group (on each problem if applicable). Late homework will incur a penalty of 10 points out of 100 until solutions are posted. After that, late homework will not be graded and will be scored as a zero in the gradebook.

ETHICAL BEHAVIOR:	The following paragraph is specifically modified to allow for collaboration on homework. No collaboration, except as specifically authorized, is allowed under penalty of failure. Plagiarism and cheating will not be tolerated; they will be dealt in accordance with University policies described in the Student Handbook. All engineering majors should be familiar with the Honor Code of our College of Engineering that is included in the freshman course material, and with professional engineering codes of ethics. Although students are encouraged to collaborate on homework assignments to develop a deeper understanding of the topics presented in this course, each student is expected to prepare and submit his/her own narrative reports, drawings, and other materials. If two students' work is suspiciously similar, a penalty may be assessed to both students. If a situation arises in which you are uncertain if cooperation with another student would constitute cheating or some other violation of the honor code, please ask the instructor for guidance and clarification of these rules. Violators will be referred to the Student Court for review, where penalties may include but are not restricted to: zero credit on the work, student placed on probation, submission of information on judgment in the students' permanent record.

SPECIAL NEEDS:	The University will make reasonable accommodations for persons with documented disabilities. Students should notify the Disability Resource Center located in 20 Dodge Hall and their instructors of any special needs. Instructors should be notified the first day of classes.

Tentative Schedule

1	9,11,12 Jan	Administrivia. Schedule. Expectations. Syllabus. Introduction. Course overview. Review of Circuits Properties and uses of controlled sources. Amplifier models. **Reading:** Sections 1.4 to 1.8.

Monday 16 Jan — MLK Holiday: No class

2	18,19 Jan	Op–Amps: Basic Applications. **Reading:** Sections 1.9 to 1.11, 2.1 to 2.5.

3	23,25,26 Jan	Amplifier Circuits: Applications. Deviations from Ideal in Op–Amps. **Reading:** Sections 2.6 to 2.11. **Lab:** 1 (Op Amps) Parts 1-2: 24 or 27 Jan.

4	30 Jan, 1,2 Feb	Diodes: Characteristics, modeling, and applications. **Reading:** Sections 3.1 to 3.6 and 3.12. Conference Travel **Lab:** 1 (Op. Amps) Part 3: 31 Jan or 3 Feb.

5	6,8,9,13 Feb	Diode Circuits. Physical operation of the junction diode. **Reading:** Sections 3.7 to 3.11. **Lab:** 2 Part 1 (Diode Circuits): 7 or 10 Feb.

6	15 Feb	Review Day **Lab:** 2 Part 2 (Diode Circuits): 14 or 17 Feb.

	16 Feb	Exam 1. Two sheets of notes, both sides.

Monday 20 Feb — Presidents' Holiday: No class

7	22,23 Feb	Introduction to the biopolar junction transistor (BJT): Physics of operation and circuit models **Reading:** Sections 4.1 through 4.4. **Lab:** No Lab 21 or 24 Feb.

8	27 Feb, 1,2 Mar	BJT Circuit Analysis: Large signal and small signal analysis of BJT circuits. **Reading:** Sections 4.5 to 4.7. **Lab:** 3 Part 1 (BJT): 28 Feb or 3 Mar.

Monday 6 Mar to Friday 10 Mar — Spring Break

9	13,15,16 Mar	BJT Applications: Amplifiers and Logic circuits. **Reading:** Sections 4.8 and 4.9. **Lab:** 3 Part 2 (BJT): 14 or 17 Mar.

10	20,22,23 Mar	Introduction to the field–effect transistor (FET): Physical operation, large–signal analysis. **Reading:** Sections 5.1 to 5.3. **Lab:** 4 Part 1 (BJT Amplifier): 21 or 24 Mar.

11	27 Mar	FET Small Signal Analysis. **Reading:** Sections 5.4 to 5.6. **Lab:** 4 Part 2 (BJT Amplifier): 28 or 31 Mar.

	29 Mar	Review Day

	30 Mar	Exam 2. Two sheets of notes, both sides.

12	3,5,6 Apr	FET Circuits: Digital Logic **Reading:** Section 6.1–6.5. **Lab:** 5 Part 1 (MOS): 4 or 7 Apr.

13	10,12,13 Apr	Digital Logic: Basic logic circuits in MOS and CMOS. **Reading:** Sections 6.6 to 6.9. **Lab:** 5 Part 2 (MOS): 11 or 14 Apr.

Monday 17 Apr — Patriots' Day Holiday: No class

14	19 Apr	CMOS Logic and Review Day

Reading Day: No Class, 21 April

	TBD	Final Exam (2 hours). Closed–book with three sheets of notes (both sides) allowed.

Notation

This is the notation used by the text to represent voltages and currents. While I like the choice, I've found it adds some extra confusion for the student. This table may help.

Quantity	V or I	Subscript	Voltage Example
Total Instantaneous Signal	lower case	CAPITAL	v_A
DC Signal	CAPITAL	CAPITAL	V_A
AC Signal	lower case	lower case	v_a
Phasor of AC	CAPITAL	lower case	V_a

Thus, any signal is represented by

$$v_A = V_A + v_a \qquad \text{Text}$$

and a sinusoidal signal is represented by

$$v_A = V_A + V_a \sin(\omega t + \phi) \qquad \text{Text}$$

Remember that the RMS of an AC signal is $V_a/\sqrt{2}$.

Decibels

Decibels are a convenient concept to describe gains and losses in electronic systems. The gain of an amplifier is described in terms of the power ratio of output to input, and is expressed in dB. (note lower–case "d," meaning "deci–," and capital "B" for "Bel.") as

$$g = 10 \log (p_{OUT}/p_{IN}).$$

If the output and input impedances are the same, then the power gain is the square of the voltage (or current) gain, and

$$g = 10 \log \left(\frac{v_{OUT}}{v_{IN}} \right)^2] = 20 \log (v_{OUT}/v_{IN}).$$

Although it is not needed for this course, signals are often expressed in dBm. This is not a measure of gain, but of signal level. It is the ratio of the power to one milliwatt.

$$y = 10 \log (p/10^{-3}\text{W}).$$

Typically, this concept is used with 50–Ohm impedances common in RF work, and

$$y = 10 \log (v^2/10^{-3}\text{W}/50\text{Ohms}).$$