EECE 2412 – Homework 8 – Spring 2017

Due: Wednesday, April 19, 2017

1) Problem 6.5 on page 406 of the textbook. In addition, for each part of the problem, draw a logic circuit (with basic logic gates such as in Fig. P6.6) that implements the Boolean expression.

2) A certain logic family has V_{OL} = 1V, V_{OH} = 4.5V, V_{IL} = 1.5V, and V_{IH} = 3V. Determine the noise margins.

3) Problem 6.58 on page 409 in the textbook. Solve this problem based on the equations in section 6.6 of the book.

4) Design a CMOS inverter with a DC transfer characteristic in which the output transitions between logic 0 and 1 ($V_o \approx 2.5V$) when the input is $V_{DD}/2 = 2.5V$. That is, the trip point should be located close to half of the 5V supply voltage.
   a) Find the required ratio (W_P/W_N) for the widths of the PMOS and NMOS transistors assuming the following parameters: $KP_N = \mu_n \cdot C_{ox} = 150\mu A/V^2$, $KP_P = \mu_p \cdot C_{ox} = 50\mu A/V^2$, $\lambda = 0.02V^{-1}$, $V_{toN} = 0.7V$, $V_{toP} = -1V$, $L = L_{min} = 0.6\mu m$.
   b) Select the transistor widths that make the maximum current during the transition equal to 3mA.
   c) Sketch the DC transfer characteristic of the inverter and label the trip point.

5) A 100fF load capacitance is driven by an inverter with a switching frequency of 100MHz with logic levels of V_{DD} = 3V and 0V. Determine the dynamic power dissipation.

6) Sketch a suitable pull-up network (PUN) the corresponding pull-down network (PDN) to realize a complex CMOS logic gate whose output has the following logic function: $Y = A\overline{B} + \overline{A}B$.

7) Consider the CMOS gate shown below. Specify the W/L ratios for all transistors in terms of the W/L ratio (n) of the NMOS transistor or the W/L ratio (p) of the PMOS transistor in a basic inverter. The minimum ratios should be selected, but such that the worst-case t_{PHL} and t_{PLH} delays of the gate are equal to those in the basic inverter.