EECE2412 Final Exam

with Solutions

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My file 11480/exams/final

General Instructions:

1. You may use a calculator.
2. You may use one page of notes (both sides).
3. Do not ask the proctor questions. Make your best guess, and explain it in writing on the exam.
4. Place phones, laptops, other electronic devices out of sight.
5. Use the workspaces provided by the vertical bar. You may use the back of the paper if needed. Write your answer on the line provided.
6. The appearance of academic dishonesty will be dealt in accordance with University policies described in the Student Handbook.

Note that the transistor is different in the two FET problems. Don't expect your answers in Problem 3 to match the parameters in Problem 4.

1 Short Answer Questions

The following questions relate to topics discussed in lectures. You should be able to answer each of them with a few words. No equations or long discussions are needed.

1.1 BJT Amplifiers

In which mode of operation is a BJT used for an amplifier? (Cutoff, Saturation, Active, Passive, Triode, or Pentode)

Active

What type of BJT amplifier is the best choice to produce a large voltage gain?

Common Emitter.

Why is it good practice to keep the AC base–emitter voltage below 10 mV in an amplifier circuit?

To prevent non–linear behavior.

What is the ideal gain of a common–collector amplifier?

1.

Is it possible to design a DC–coupled amplifier using a single BJT? Why or why not?

No. The base, emitter, and collector must be at different voltages.

1.2 FET DC Analysis

On which terminal of an FET is the arrow in the symbol we used in class?

The source.

Which terminal of a FET carries no current?

The gate.

In a current mirror, two or more identical FETs are used. The circuit controls the current in the first, and the remaining ones all produce the same current. If we want to change the current in one of the "mirror" transistors, which parameter would we change?

Width, W.

Analyzing a particular FET circuit with the triode equation, we obtain two solutions, one with $V_{DS} = 2.8$ V and the other with with $V_{DS} = 1.2$ V. Which one is valid? Why?

The second, with the smaller V_{DS}. The higher one will be beyond the boundary and thus into the triode region.

1.3 FET Amplifiers

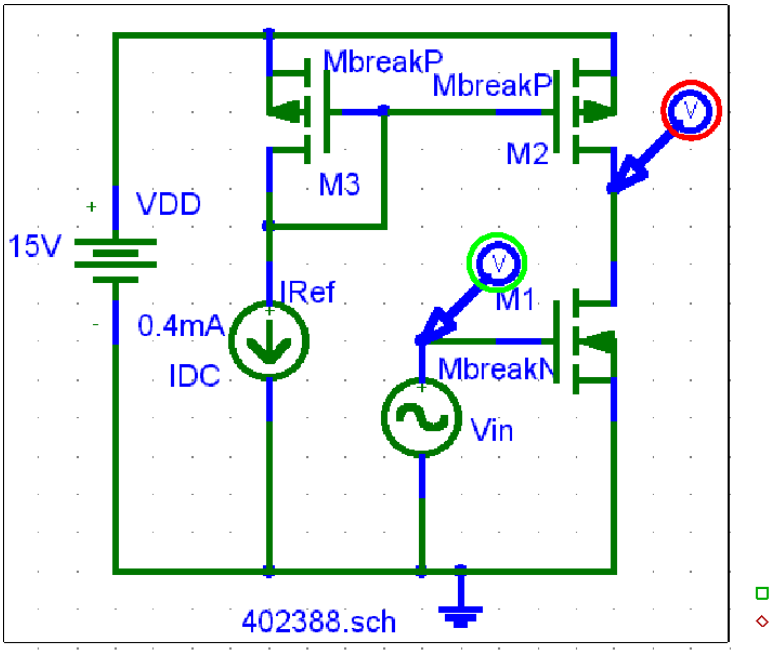
In which mode of operation is a FET used for an amplifier? (Cutoff, Saturation, Active, Passive, Triode, or Pentode)

Saturation

A depletion FET is an attractive choice for a DC–coupled voltage amplifier. Why?

The gate and drain can be at the same DC levels while the transistor is in saturation.

In the circuit shown in this figure,$M1$ is the amplifier transistor. The input is on the gate, and the output is on the drain.



What type of amplifier is this?

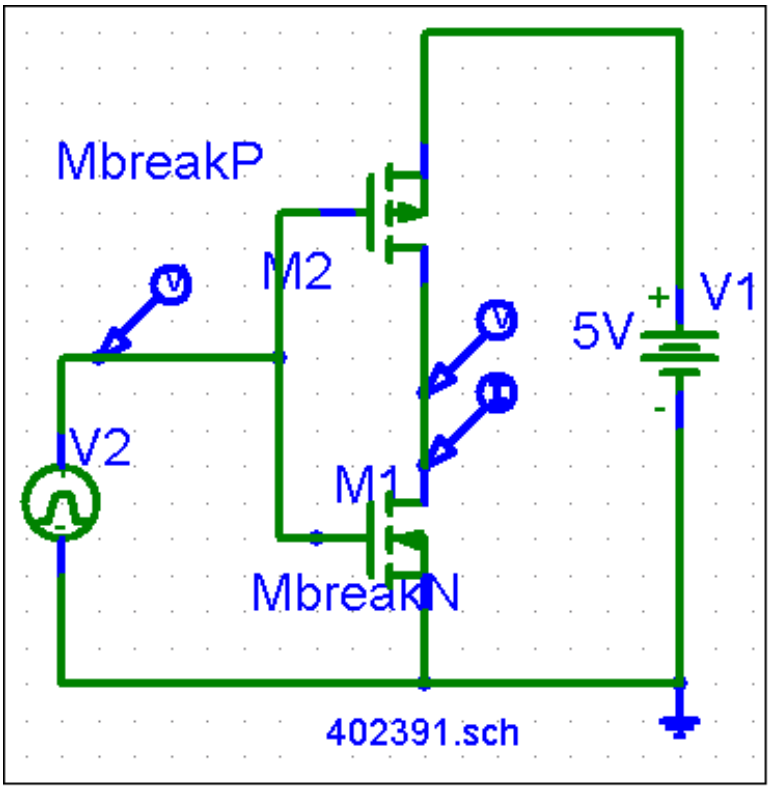
Common source.

What parameters of the circuit determines the output resistance? Hint: There are two.

The r_0 of $M2$.

1.4 Logic

Here is a typical CMOS logic inverter.



What is the current at the current marker in this circuit when the input, $V2$, is high? What is it when the input is low?

Zero, Zero.

What is the voltage at the output voltage marker in this circuit circuit when the input, $V2$, is high? What is it when the input is low?

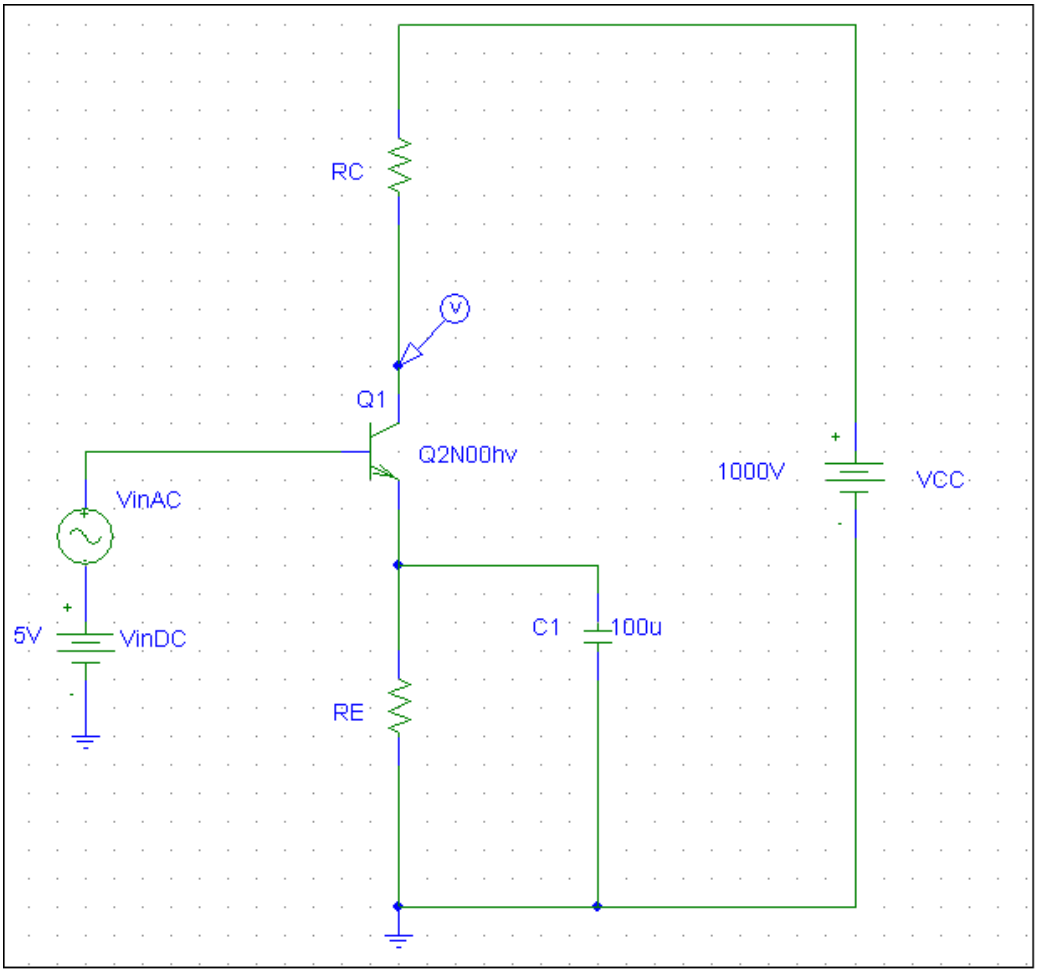
Zero, 5V.

2 High–Voltage Piezoelectric Driver

A piezoelectric transducer is a device which can move objects through small distances up to hundreds of micrometers, with the distance being proportional to an applied voltage. However, several hundred volts may be required. We would like to amplify a low–voltage control signal to provide voltage for the piezoelectric transducer. Fortunately the transducer has a relatively high resistance, so we can probably use just a voltage amplifier. Also fortunately, transistors capable of working with these high voltages are available. Otherwise these drivers would have to use vacuum tubes and I would have to find another exam problem.

Let's build an amplifier using the circuit below, with the piezoelectric transducer connected to the collector. We would like a voltage gain of $|A_V| = 100$. so that, as the input swings through 10 V the output swings through 1000 V. The supply voltage is 1000 V, and we would like 2.5 mA of DC collector current at the nominal operating point with a 500 V output on the collector. We will use $V_B^{(DC)} = 5$ V as the nominal input voltage. For this transistor

$$\beta = 55. \tag{2.1}$$



2.1 Resistor Selection

Determine the values for the two resistors.

$$RC = \frac{1000\ \text{V} - 500\ \text{V}}{2.5\ \text{mA}} = 200\ \text{k}\Omega \tag{2.2}$$

The gain of the amplifier is nominally

$$A_V = -\frac{RC}{RE}, \tag{2.3}$$

so

$$RE = 2\ \text{k}\Omega. \tag{2.4}$$

2.2 Currents and Powers

What is the base current at the operating point?

Use KVL,

$$5\ \text{V} - 0.7\ \text{V} = (\beta + 1)\, i_B^{(DC)} R_E \tag{2.5}$$

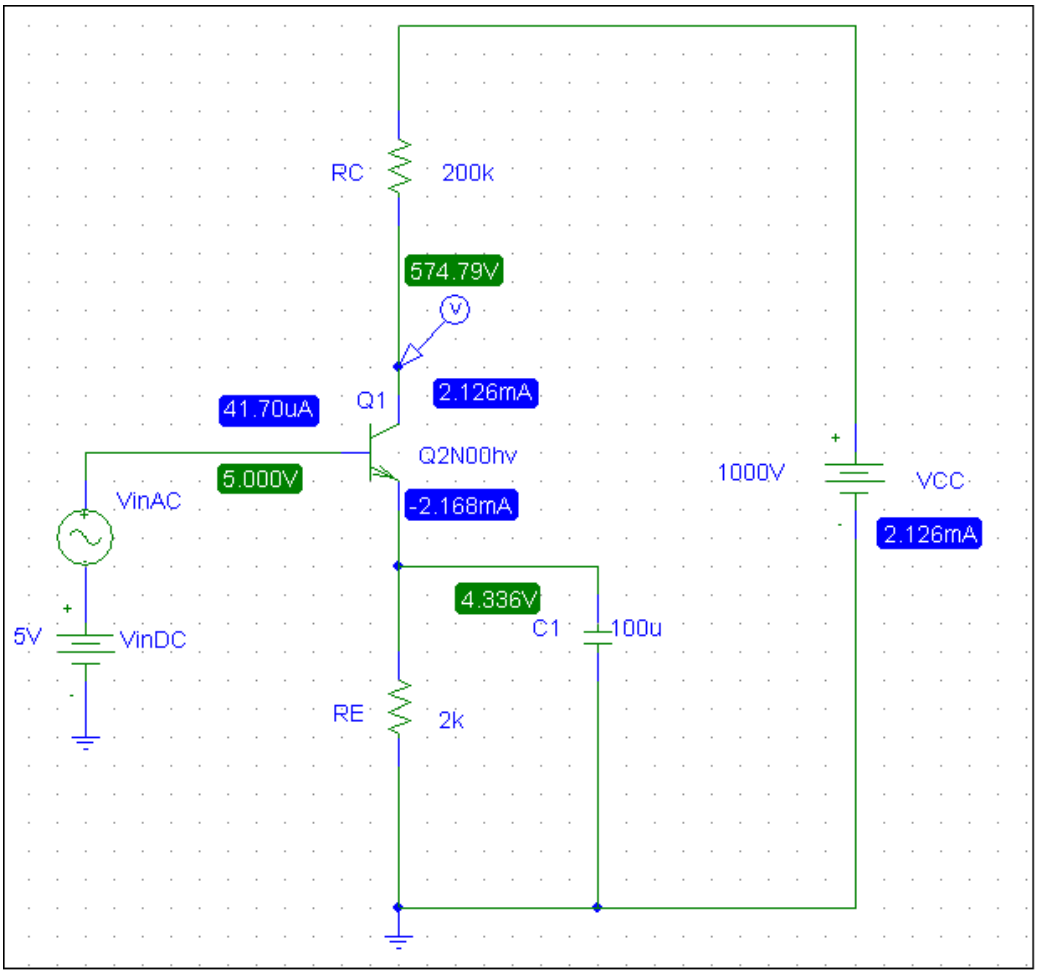
$$i_B^{(DC)} = 38\ \mu\text{A}. \tag{2.6}$$

How much power is dissipated in each resistor at the operating point?

$$P_C = I_C^{(DC)} RC = (2.5\ \text{mA}) \times 200\ \text{k}\Omega = 1.25\ \text{W}. \tag{2.7}$$

$$P_E = I_C^{(DC)} RE = (2.5\ \text{mA}) \times 200\ \text{k}\Omega = 12.5\ \text{mW}. \tag{2.8}$$

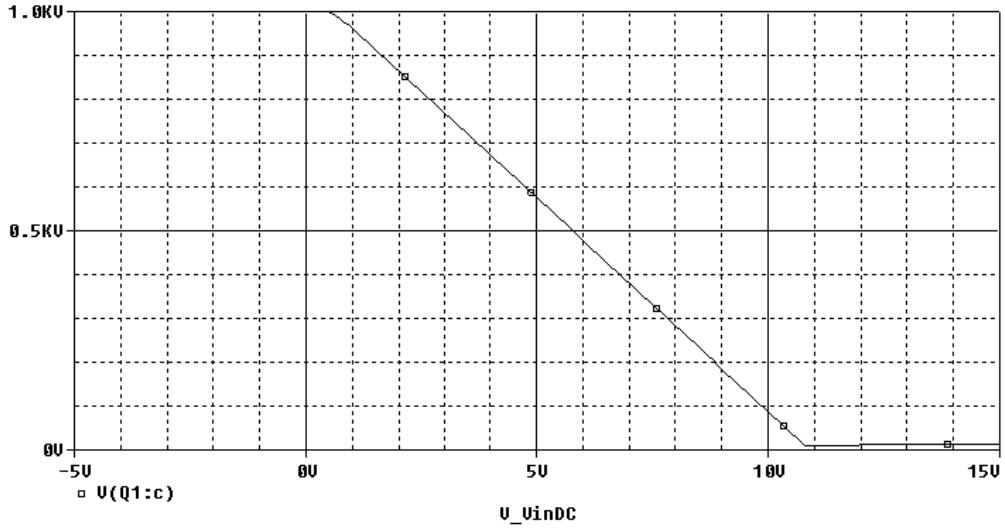
A SPICE analysis is shown below.



2.3 Transfer Function

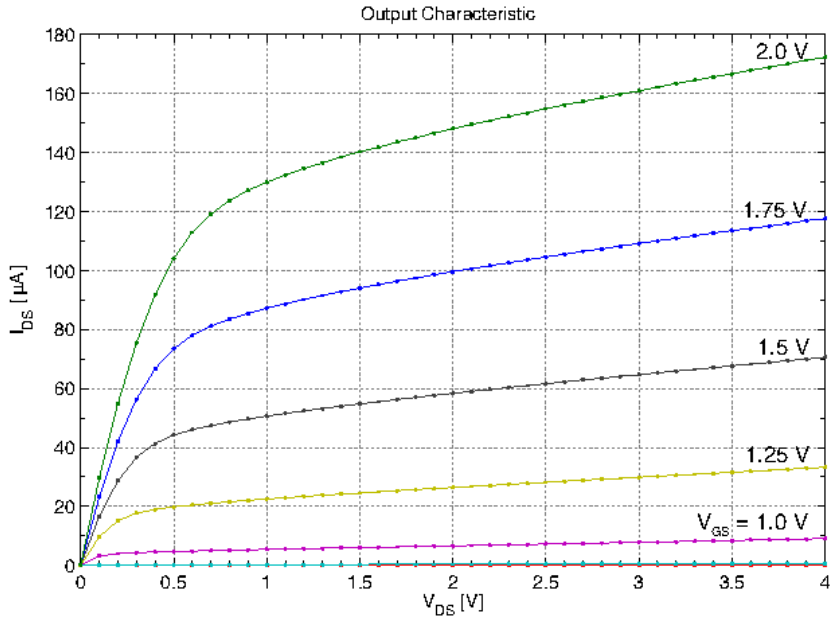
What are the maximum and minimum input voltages required to cover the full 1000 V range of output voltages? Draw the transfer curve carefully.

Minimum is 0.7V. Maximum is 10.7V.

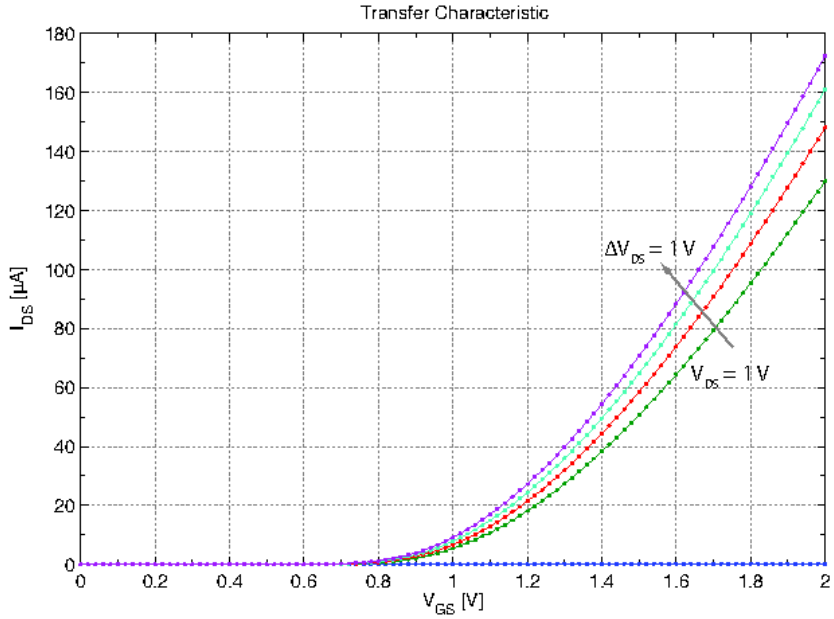

1.0KV
0.5KV
0V
-5V
0V
5V
10V
15V
V(Q1:c)
V_VinDC

3 FET DC Analysis

Here we see the characteristic curves of an actual 3–micron N–channel FET at a temperature of 297.5K (a balmy 24.35C or 75.83F). The first figure shows the usual i_D–*vs.*–v_{DS} curves for different gate voltages. These values are different from most of the FETs we used in class.



The next plot shows the current for different values of v_{DS}, from 1 Volt to 4 Volts in 1–Volt steps, as a function of v_{GS}.



3.1 DC Parameters

Determine the numerical value of the threshold voltage.

0.75 Volts

Determine the numerical value of $\mu_n C_{ox} W/L$.

At

$$V_{GS}^{(DC)} = 4 \text{ V}, \tag{3.1}$$

$$I_D^{(DC)} = \mu_n C_{ox} \frac{W}{L} \frac{\left(V_{GS}^{(DC)} - V_{Thr}\right)^2}{2} \left(1 + \lambda V_{DS}\right). \tag{3.2}$$

Extrapolating back to $V_{DS}^{(DC)} = 0$,

$$\mu_n C_{ox} \frac{W}{L} = \frac{2 I_D^{(DC)}}{\left(V_{GS}^{(DC)} - V_{Thr}\right)^2}. \tag{3.3}$$

$$\mu_n C_{ox} \frac{W}{L} = 2 \frac{120 \ \mu\text{A}}{(4 \text{ V} - 0.75 \text{ V})^2} = 22.7 \ \mu\text{A/V}^2. \tag{3.4}$$

Estimate the numerical value of the Early Voltage. How accurately can you determine it from this graph?

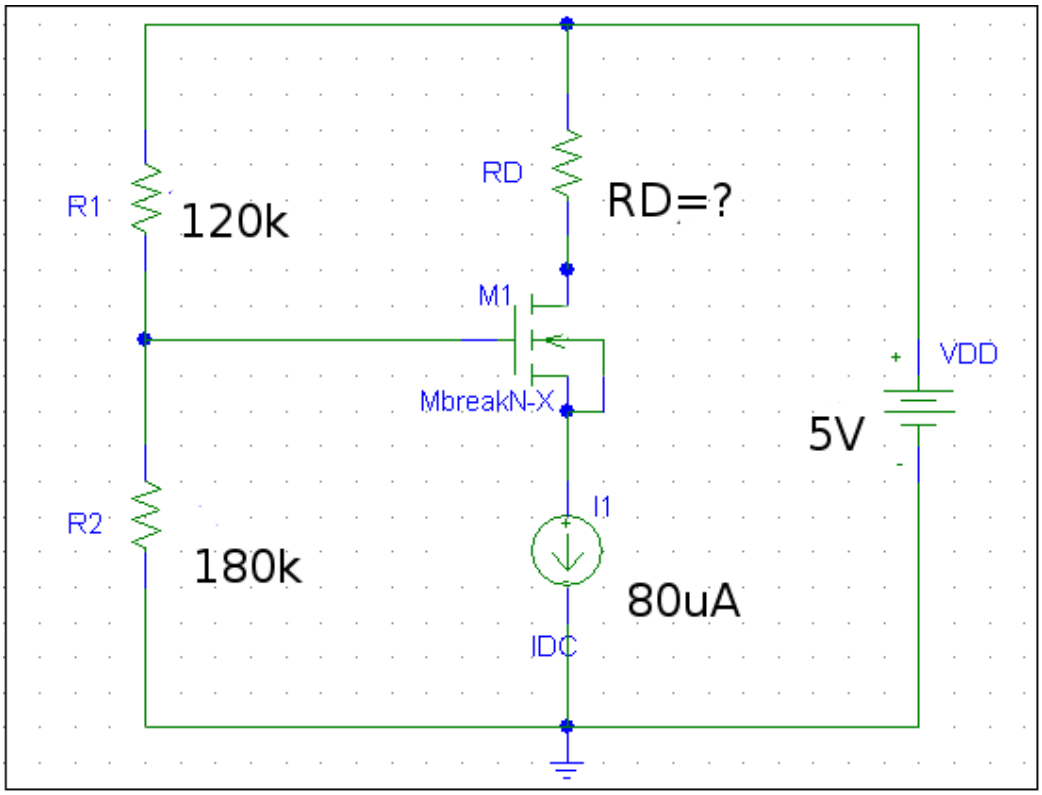
$$V_A = \frac{i_D}{\lambda} \tag{3.5}$$

$$\lambda = \frac{172 \ \mu\text{A} - 130 \ \mu\text{A}}{4 \text{ V} - 1 \text{ V}} = 14 \ \mu\text{A/V}. \tag{3.6}$$

$$V_A = 8.6 \text{ V}. \tag{3.7}$$

3.2 DC Circuit

Now consider this transistor in the following circuit. Use the curves instead of equations where possible. The equations are simple enough but a bit time–consuming.



What is the numerical value of $V_G^{(DC)}$?

$$V_G^{(DC)} = 5\text{ V} \times \frac{180\text{ k}\Omega}{120\text{ k}\Omega + 180\text{ k}\Omega}. \tag{3.8}$$

$$V_G^{(DC)} = 3.0\text{ V}. \tag{3.9}$$

If I want to operate at $V_{GS} = 2$ V, what is the voltage on the source?

$$V_S^{(DC)} = V_G^{(DC)} - V_{GS}^{(DC)} = 1\text{ V} \tag{3.10}$$

What is the value of R_D?

From the curves, $V_{DS}^{(DC)} = 0.3$ V, so

$$V_D^{(DC)} = V_S^{(DC)} + 0.3\text{ V} = 1.3\text{ V}. \tag{3.11}$$

The current is 80 μA, so

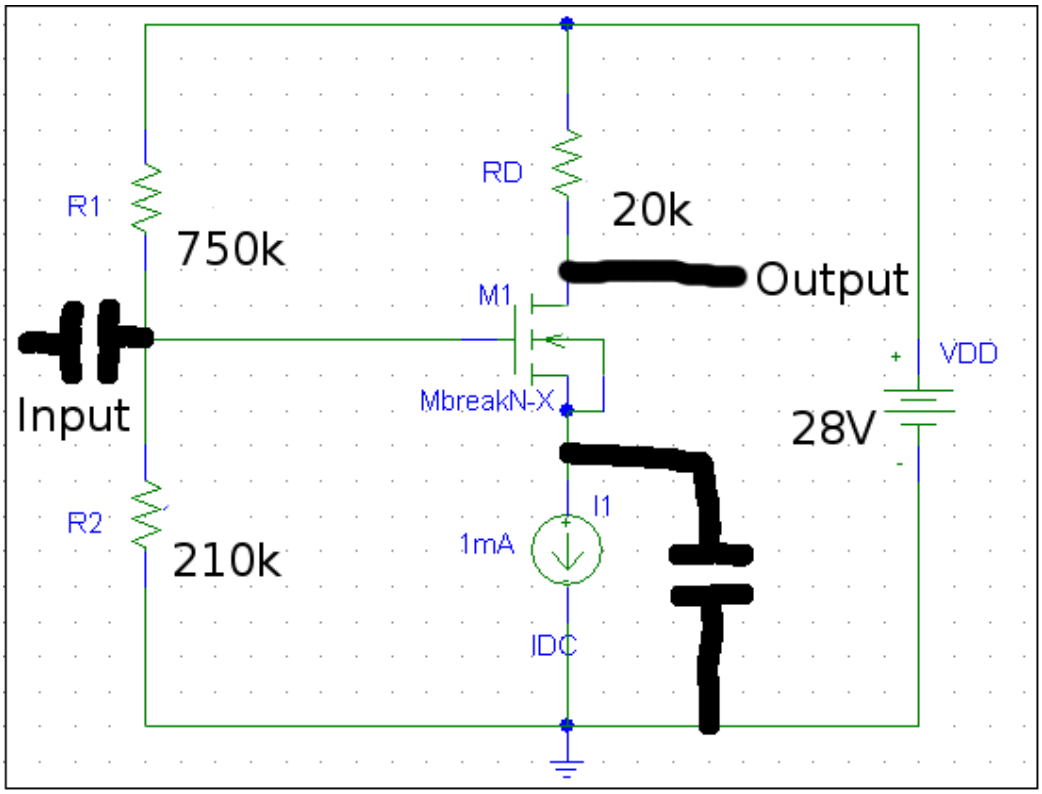
$$R_D = \frac{5\text{ V} - 1.3\text{ V}}{80 \times 10^{-6}\text{ A}} = 46\text{ k}\Omega. \tag{3.12}$$

Is the transistor is in saturation or triode?

Triode, from the curves.

4 FET Amplifier

Consider the following circuit. In this case, $\mu_n C_{ox} = 20\ \mu\text{A/V}^2$, $L = 2\ \mu\text{m}$ and $W = 10\ \mu\text{m}$, $V_{thr} = 2$ V, and $V_A = 150$ V.



4.1 Small–Signal Parameters

Compute the small–signal parameters, g_m and r_0, using the equations we used in class.

$$g_m = \sqrt{2 I_D^{(DC)} \mu_n C_{ox} \frac{W}{L}} \tag{4.1}$$

$$g_m = 440\ \mu\text{A/V} \tag{4.2}$$

$$r_0 = \frac{V_A}{I_D^{(DC)}} \tag{4.3}$$

$$r_0 = 150\ \text{k}\Omega. \tag{4.4}$$

4.2 Amplifier

The input is on the gate, and the output is on the drain. What is the voltage gain of this amplifier?

$$A_V = -g_m \left(RC \parallel r_0 \right) \tag{4.5}$$

$$A_V = -8 \tag{4.6}$$

What is the output impedance?

$$R_{out} = \left(RC \parallel r_0 \right) = 17 \text{ k}\Omega. \tag{4.7}$$

How large can the input signal be before the transistor leaves the saturation region?

We need to find the operating point. The drain voltage is

$$V_D^{(DC)} = V_{DD} - I_D^{(DC)} R_D = 8 \text{ V}. \tag{4.8}$$

The AC output must be much less than 8 V. Thus the input must be

$$\left| v_{in}^{(AC)} \right| \ll \frac{8 \text{ V}}{|A_v|} = 1 \text{ V}. \tag{4.9}$$