EECE 2413
Electronics Laboratory

Lab #5: MOSFETs and CMOS

Goals

This lab will introduce you to MOSFETs (metal-oxide-semiconductor field effect transistors). You will build a MOSFET *inverter* and determine the voltage transfer characteristic of this device (V_{out} vs. V_{in}). From this transfer characteristic you will learn how to extract information about the MOSFET such as threshold voltage (V_T) and the device constant K.

In the cutoff and triode regions the MOSFET approximates the operation of a switch. In between these two regions lies the saturation region. In saturation the MOSFET makes a good amplifier.

Next, the CMOS inverter will be examined. This circuit also uses an n-channel MOSFET as the active driver, but replaces the drain resistor (R_D) with a p-channel MOSFET. This configuration dramatically reduces power consumption.

As always, take your time during these experiments. Think about *what* you are being asked to do and *why* the experiments are important.

Once you are comfortable with these basic MOSFET configurations, you will design and test either a CMOS logic gate or an AM radio transmitter using the CD4007 integrated circuit.

Prelab

Prelabs will be submitted prior to the lab session. Keep a copy for your own use during the lab!

1. In Fig. 3 find R_{G1} and R_{G2} such that $V_{GS} = 2$ volts. Compute I_D and V_{DS} if $V_T = 1$ Volt and $k_n'(W/L) = 0.5$ mA/V^2 (see eqns. 4.5a,b in the 5th edition of Sedra and Smith). (If you only have the 2nd edition of Hambley, refer to Section 5.3 and use the values of 1 volt for V_{to} and K = 0.25 mA/V^2 in equation 5.18.) Remember that this is a DC analysis, so set $v_{in} = 0$. (Note: there are many correct solutions for R_{G1} and R_{G2} !)

2. Read the lab experiment and see the instructor with any questions you may have.

3. Read Part 2, choose one of the two design projects, and sketch a circuit you think will work. (You may change your design as you work through the lab, however.) Remember to indicate the values of the resistances and capacitors used in your design.

Part 1: MOSFET characteristics

The MOSFETs that you will be using for this lab are in a 14-pin package as shown in Fig. 1. Study this diagram and become familiar with the layout of the individual MOSFETs within the CD4007 chip. Notice there are three n-channel devices and three p-channel devices. Although some devices share pins, all terminals for each device are available at an external pin on the chip.

MOSFETs are actually 4-terminal devices: gate, drain, source, and substrate. In the CD4007 the *substrates* for *all* n-channel devices are connected to pin 7. Likewise, the substrates for all p-channel devices are connected to pin 14. *For proper function of the MOSFETs you must attach pin 7 to the lowest potential in your circuit (usually ground) and you must attach pin 14 to the highest potential in your circuit (V_{DD}).*

MOSFETs are susceptible to electrostatic discharge (ESD). You have no doubt experienced large ESDs if you have ever scuffed your feet across a carpet and touched a metallic object. Even very small ESDs can damage a MOSFET by blowing-out the gate oxide. This is mainly because the gate oxide is very thin (<<100 nm). These MOSFETs have been protected from minor forms of ESD by two clamping diodes attached to each gate. One diode prevents V_{GS} from exceeding V_{DD} *(pin 14)* + 0.7 V. The other prevents V_{GS} from becoming more negative than V_{SS} *(pin 7)* - 0.7 V. See Fig. 1 on the spec sheet.

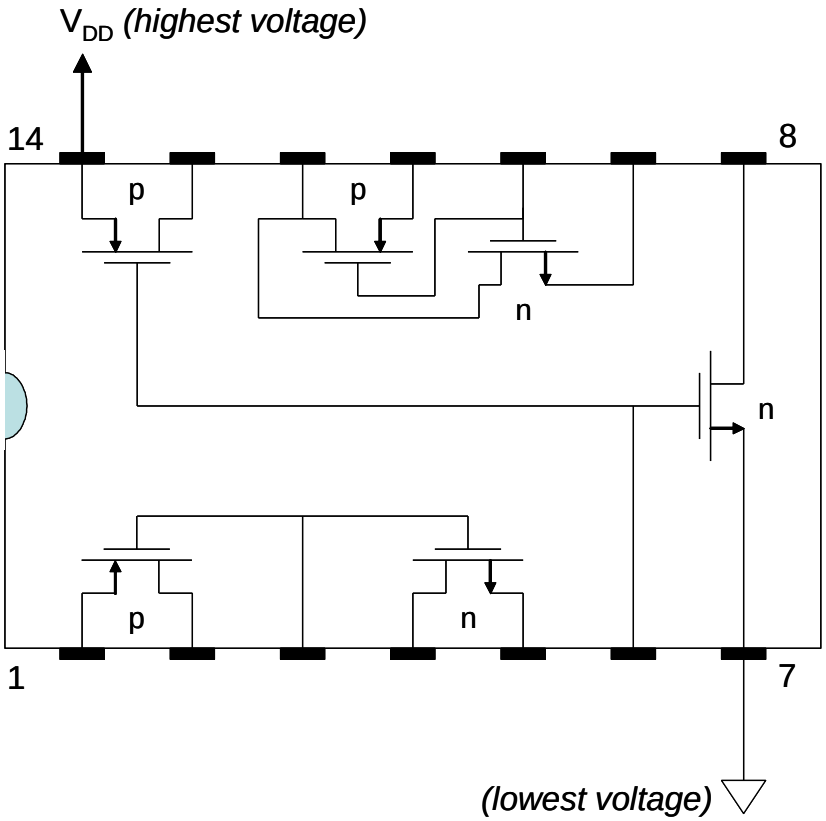


Figure 1. The CD4007 Integrated Circuit.

Concept: The DC transfer characteristic of a MOSFET inverter

Build the simple MOSFET inverter shown in figure 2. You may use any of the three n-channel MOSFETs on the CD4007, but don't forget to connect pins 7 and 14 as described above!

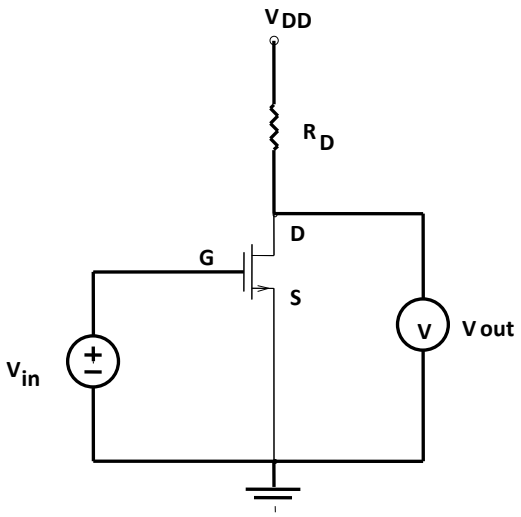


Figure 2. A MOSFET Inverter
R_D = 10 kΩ, V_{DD} = 10 V, 0≤V_{in} ≤10 V.

a) Measure the voltage transfer characteristic for the MOSFET inverter by varying V_{in}. Use the table below to guide you in selecting the appropriate data points.

Important: Please time yourself, and **record** the time taken to complete step a).

Table for Inverter Transfer Characteristic

V_{in}	V_{out}	I_D (Calculated) *
0	10	
	9.95	
	9	
	8	
	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0.5	
10		

* From V_{out}, V_{DD}, and R_D.

Notice that the circuit is an inverter: When the input voltage is "high," the output voltage is "low" and vice versa. **What is the total power dissipation of this inverter when V_{in} = 0? What is the power dissipation when V_{in} = 10 v?**

b) i) When the gate reaches the threshold voltage, the MOSFET begins to conduct current through the drain (I_D). Based on the measurements in part (a), **what is the approximate Threshold voltage (V_T) for this MOSFET?**

ii) At home, plot the square-root of Drain current against Input voltage (V_{GS}). The trace now becomes a straight line. Extrapolate this straight line to the Input voltage axis . The intercept gives us the **accurate Threshold voltage V_T**.

c) Remember that in the saturation region, $I_D = ½ k_n'(W/L)(V_{GS} - V_T)^2$. Find $½k_n'(W/L)$ for this MOSFET using the data from part (a), where the equation for I_D is based on the notation in the Sedra and Smith textbook.

d) Carefully and accurately plot the voltage transfer characteristic (*i.e.*, V_{out} vs. V_{in}) in your notebook and lab report. **Identify the three regions of MOSFET operation on your plot:**

Cut-off:	$V_{GS} < V_T$
Saturation:	$V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$
Triode:	$V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$

Concept: The MOSFET used as a switch

If we wanted to use the MOSFET as a switch, we would design a circuit so that the MOSFET was either in the cut-off region (*the switch is opened between D and S*) or the triode region (*switch closed ~ short circuit*). As an example, it is possible to redesign your night-light circuit from Lab 3 using a MOSFET rather than a BJT.

e) **Calculate the "on" resistance of this MOSFET when $V_{in} = 10$ v, where $R_{on} = V_{DS}/I_D$. Next find R_{off} when $V_{in} < V_T$. Comment on the quality of this device as a switch.** (Ideally, $R_{on} = 0\ \Omega$ and $R_{off} \rightarrow \infty$).

Concept: The MOSFET amplifier

The voltage gain of a circuit is defined as $A_V = \Delta V_{out} / \Delta V_{in}$. By looking at the plot you made in part (d), it is easy to see that A_v is nearly zero in the cut-off and triode regions since the slope in these regions is approximately zero.

f) Find the bias point (V_{GS}, V_{DS}) where $|A_V|$ is maximum using the voltage transfer characteristic that you found in part (a).

g) *Graphically* determine the small signal voltage gain at this bias point. (Watch the ± sign!)

Analog Option: Ask you instructor if you should perform parts (h) and (i) below! If not, please skip to the *CMOS Logic* section.

To use the circuit in Fig. 2 as an amplifier, we need to add a circuit to the *gate* which sets the bias point (V_{GS}). One way to do this is shown in Figure 3 below:

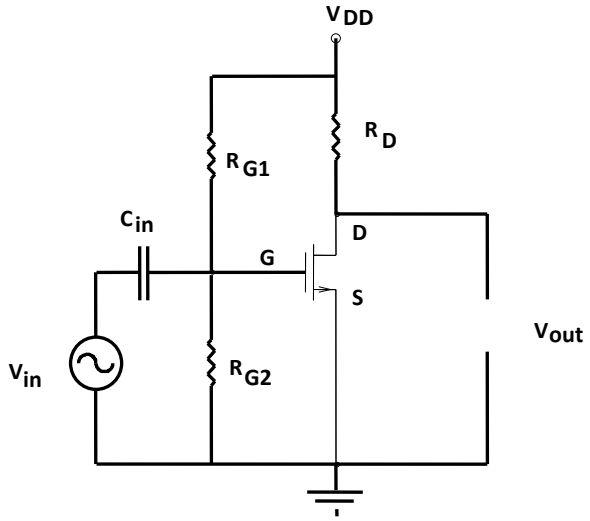


Figure 3. A common-source (CS) MOSFET amplifier
C_{in} = 1.5 μF, R_D = 10 kΩ, V_{DD} = 10 volts
R_{G1} and R_{G2} are to be determined.

Recall that the gate current in a MOSFET is zero and that C_{in} acts like an open circuit under DC conditions.

h) Find values for R_{G1} and R_{G2} that result in the optimum operating point determined in part (f). Notice that there is no unique solution to this design problem. Using larger resistors will increase the input impedance of the amplifier (which is usually good), but will also increase the amplifier's susceptibility to noise. **Record** the values for the two resistors. Also **measure** and record the operating point of the circuit (when v_{in} = 0). **Explain why your MOSFET is biased in the saturation region. NOTE:** Finding the exact resistors to implement your design may be tricky. When designing, pick one of the two values from those resistors in your parts kit. Use series and parallel combinations for the other -- see the instructor or lab tech if you need a resistor that is not in the kit.

i) Use the signal generator to apply a small signal to the amplifier's input. Measure and record the voltage gain. **Compare this gain with the gain that you determined graphically in part (g).** (Remember, a "small signal" should *not* produce distortion at the output of the amplifier.)

Notice that the voltage gain of this amplifier is much lower than the gain of a comparable BJT amplifier. This is because g_m is typically lower for a MOSFET than a BJT.

Concept: CMOS Logic

The logic inverter in Figure 2 has one major flaw. The power dissipation is too high when the output is low. This would not be a practical logic gate in a modern integrated circuit because a large number of these gates would use a huge amount of power. The CMOS logic family significantly reduces power dissipation by replacing the drain resistance (R_D) with a p-channel MOSFET as shown in Figure 4.

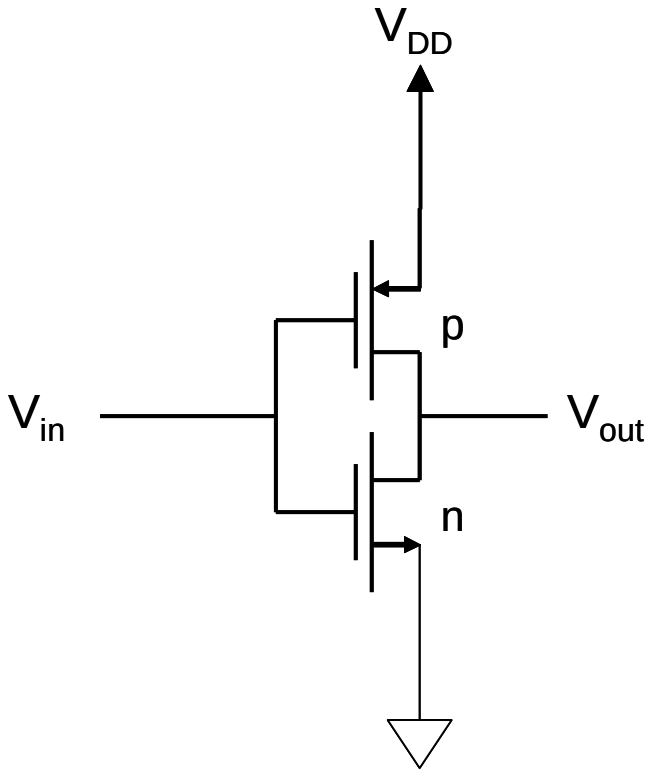


Figure 4: The CMOS inverter

j) Build the CMOS inverter shown in Figure 4. Here, use output 2 from the Power Supply for V_{dd} = 10V, and output 3 for V_{in}. *Remember from previous labs that channel 1 of the Keysight EDU36311A Tripple Output Programmable DC Power Supply can only go up to 6V of supply voltage. Therefore, use channel 2 and 3 for your V_{dd} and V_{in}.*

k) Repeat the measurements in the form from part a) to characterize the CMOS inverter. Around the midpoint, you might have to take measurements with smaller increments on the x-axis. Plot the Voltage Transfer Characteristic for the CMOS inverter using any plotting software of your choice (e.g., MATLAB, Excel)

l) Find on the plot the bias point (V_{in}) where the voltage gain of the CMOS inverter is at a maximum. Then, use the input and output voltage arrays to determine the small signal voltage gain ($A_v = \Delta V_{out} / \Delta V_{in}$) at this bias point.

m) Using an Ammeter, determine the total power dissipation of this inverter when V_{in} = 0 and when V_{in} = 10V. Assume that the two inverters (Figure 2 and Figure 4) are in the high state 50% of the time and in the low state 50% of the time for many logic applications. **Compare the average power dissipation of the two inverters and**

describe the benefit of CMOS logic.

Part 2: MOSFET Design

Choose one design project below: Remember to hand-in your signed lab notebook before leaving the lab!

1. CMOS Logic

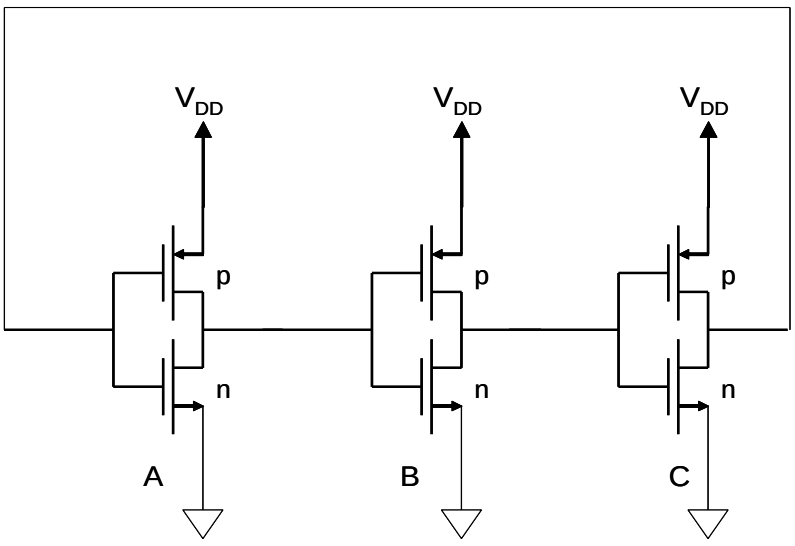
As you discovered in lab last week, the advantage of CMOS logic is that no drain current flows through the MOSFETs when the output is either high or low. Because the CMOS logic family is based on the inverter, the logic functions of NOT, NAND, and NOR are easy to create. The logic functions AND and OR, however, require us to build a NAND or NOR gate and then add an inverter to the gate output: AND = NAND+NOT

Design a 3-input CMOS OR-gate using MOSFETs on the CD4007 chip. Make certain that the power dissipation is zero when the output is both logic 1 and logic 0. As an added challenge, design the OR gate using the minimum number of CD4007 chips. Remember, pins 7 and 14 are committed to ground and V_{DD}, and this limits the placement of these two MOSFETs in your circuit. Add push-button switches to the inputs of the OR gate so that pushing the button applies a logic "1" to the gate and releasing the button applies a logic "0".

2. CMOS Ring Oscillator and AM radio transmitter

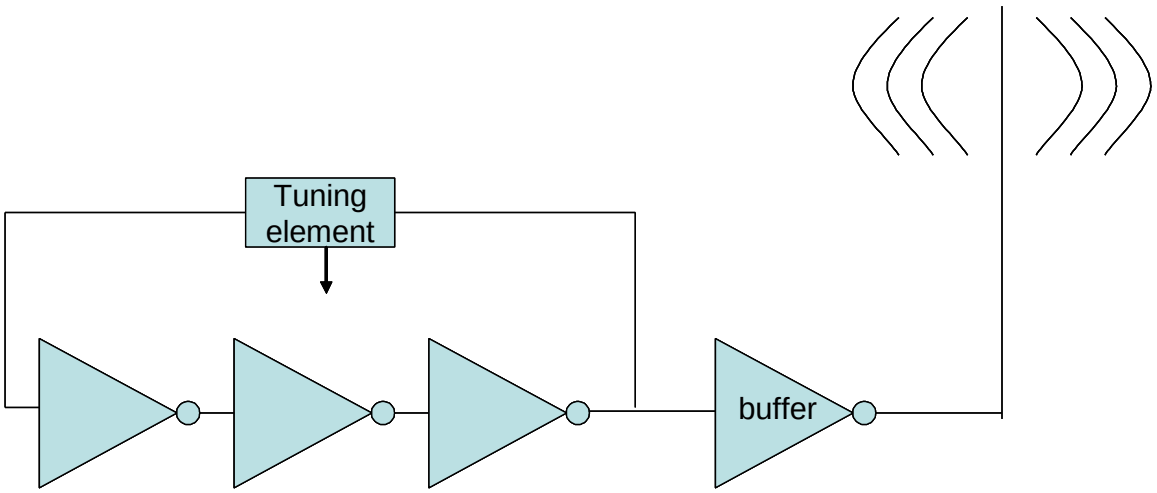
For this design, you may borrow (through your Instructor / TA) an AM radio from the Instrument Room. This radio will be used to test your AM transmitter.

A *ring oscillator* is made by connecting an *odd* number of inverters in a closed ring as shown below. To see how this oscillates, *assume* that inverter **A** has an input of zero and the output of inverter **A** is V_{DD}. Then the input to **B** is V_{DD}, and the output of **B** is zero. This, in turn means the input to **C** is zero and the output of **C** is V_{DD}. This *switches* the input to inverter **A** from zero to V_{DD}. The circuit "chases its tail" causing the inverters to continuously switch from high to low. The oscillation frequency, f_{osc}, depends on the *propagation delay time,* which is the small time it takes to charge the (gate) capacitance and switch the state of any individual inverter, and is given by $f_{osc} = 1/(2Nt_p)$. Here *N= # of inverters* and t_p*=average propagation delay* of an inverter driving another identical inverter.



The oscillation frequency can be controlled by changing the RC time constant between any two inverters. This will increase the time it takes to switch the input state. Modifying the RC time constant can be accomplished by inserting a resistor between any output and the next input (increasing R) or by inserting capacitance between any input and ground (increasing C).

The AM radio band is between 540 kHz and 1610 kHz. Design a ring oscillator to generate an output frequency in the AM band. Choose a frequency where there are no radio stations. It is strongly advised to connect a piece of wire to act as an antenna. The antenna has a large capacitance and therefore will change the oscillator frequency by increasing the propagation delay. To avoid this, add another CD4007 inverter between the output of the oscillator and the antenna! This fourth inverter acts like a buffer. A basic block diagram is shown below:



CMOS ring oscillator

The ring oscillator generates the *carrier frequency* that your AM radio is tuned to. There is *no information* contained in this frequency, however. To add information, we modulate the carrier frequency in amplitude. Here we will just turn the carrier on and off. To accomplish modulation, use the function generator (you could also use a 555 timer). The function generator should be set up to produce a 1 kHz square wave between 0 and 5 volts. Use the DC OFFSET and AMPLITUDE controls to adjust the function generator output while viewing it on the oscilloscope. Once you have the necessary waveform, apply it to V_{DD} and ground of your buffer. Now the oscillator's output is turning on and off at 1 kHz. Tune the AM radio until you hear the 1 kHz signal being transmitted.

Finally, place a push-button switch in the circuit so that you can interrupt the transmission. Pushing the switch on and off will allow you to send Morse Code to an AM radio.

When your design is complete, get the instructor's approval of your fully documented schematic.

Hand-in your lab notebook for grading prior to leaving the lab!

Equipment List -- Lab #5

Note: "*" indicates this component was used in Lab 1 & 2.

Keysight EDU33212A Waveform Generator*
Keysight DSOX1204G Digital Storage Oscilloscope *
Keysight EDU36311A Tripple Output Programmable DC Power Supply *
Keysight EDU34450A Digital Multimeter
Proto-Board model PB-103 *
Dell OPTIPLEX 755 Desktop PC*
#20 hook up wire *
wire strippers *
Banana plug-terminated test leads *
BNC-to-BNC cable *
BNC-to-Banana plug cable (2) *
BNC Tee *
Momentary contact push-button switches (3)
AM Radio ------- shared by class
Transistors:

CD4007	complementary MOSFETs	(3)

Resistors: 1/4 W unless otherwise specified

2.2 kΩ	±5%	(1) *
10 kΩ	±5%	(2) *
47 kΩ	±5%	(2) *
100 kΩ	±5%	(2) *
309 kΩ	±5%	(2) *
1 MΩ	±5%	(3)

Capacitors:

1.5 μF	non-polarized	(5)

CD4007 data sheets from http://focus.ti.com/lit/ds/symlink/cd4007ub.pdf

Please refer to Figure 1 for the terminal diagram of the CD4007UBE integrated circuit used in this lab.

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS018C – Revised September 2003

CD4007UB Types

CMOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

■ CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

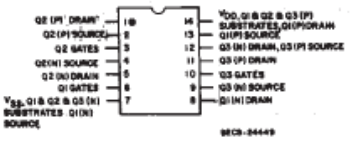
More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:

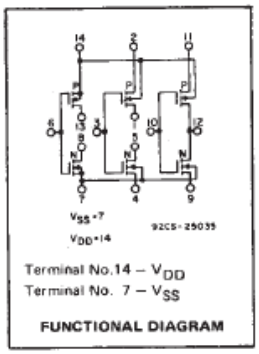
- Extremely high-input impedance amplifiers
- Shapers
- Inverters
- Threshold detector
- Linear amplifiers
- Crystal oscillators

TERMINAL DIAGRAM
Top View



Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation – t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative **Standard No. 13B, "Standard Specifications** for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C



Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

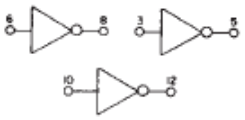
CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

a) Triple Inverters



(14,2,11); (8,13); (1,5); (7,4,9)

92CS-15550

b) 3-Input NOR Gate



92CS-15549

(13,2); (1,11); (12,5,8); (7,4,9)

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS	LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance	C_{IN}	Any Input	10	15	pF

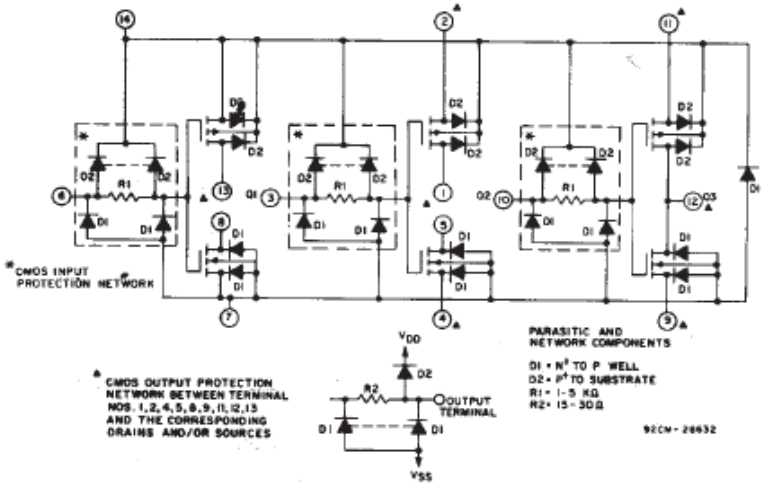


Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

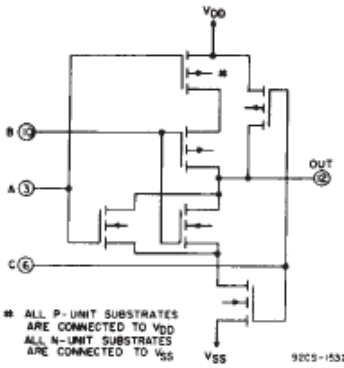
c) 3-Input NAND Gate



(1,12,13); (2,14,11); (4,8); (5,9)

92CS-15548

d) Tree (Relay) Logic



(13,12,5); (4,9,8); (14,2); (1,11)

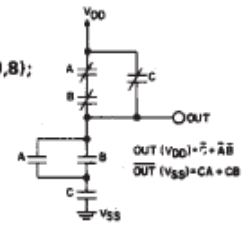
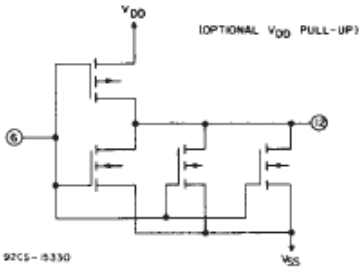
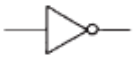


Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB.

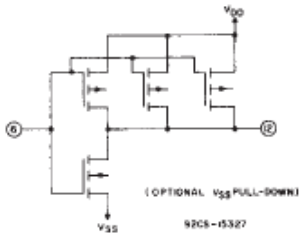
e) High Sink-Current Driver



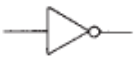
(6,3,10); (8.5, 12); (11,14); 7,4,9)



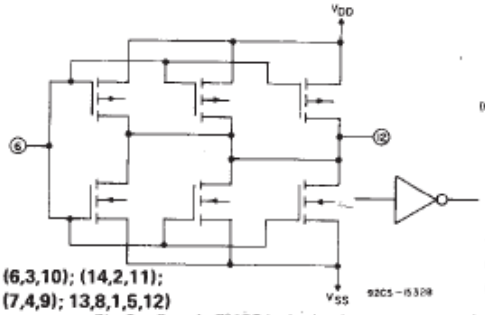
f) High Source-Current Driver



(6,3,10); (13,1,12); (14,2,11); (7,9)

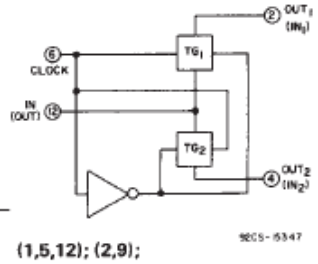


g) High Sink - and Source-Current Driver



(6,3,10); (14,2,11); (7,4,9); 13,8,1,5,12)

h) Dual Bi-Directional Transmission Gating



(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB (Cont'd).

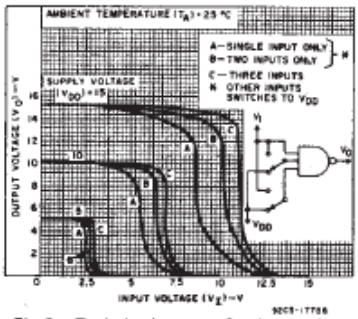


Fig. 3 – Typical voltage-transfer characteristics for NAND gate.

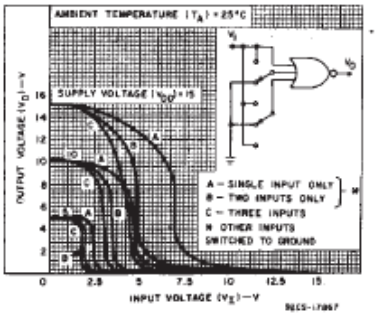


Fig. 4 – Typical voltage-transfer characteristics for NOR gate.

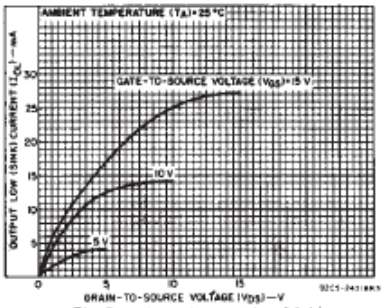


Fig. 5 – Typical output low (sink) current characteristics.

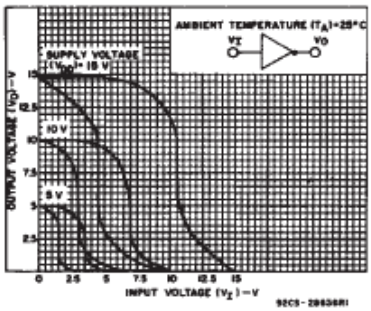


Fig. 6 – Minimum and maximum voltage-transfer characteristics for inverter.

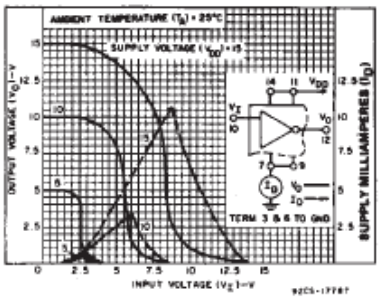


Fig. 7 – Typical current and voltage-transfer characteristics for inverter.

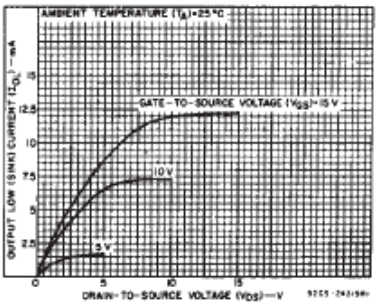


Fig. 8 – Minimum output low (sink) current characteristics.