Fundamentals of Electronics
Week 10

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Agenda

- BJTs and FETs
- Field–Effect–Transistor Symbols
- FET Basic Physics
- Structure
- I–V Terminal Characteristics
- Biasing
- Amplifiers
  - FET Taxonomy
  - Pi and Tee Models
  - Biasing — The Details (Current Mirrors and Steering)
  - Three Amplifiers
- Logic Circuits (Next Week)

Field–Effect Transistor (1)

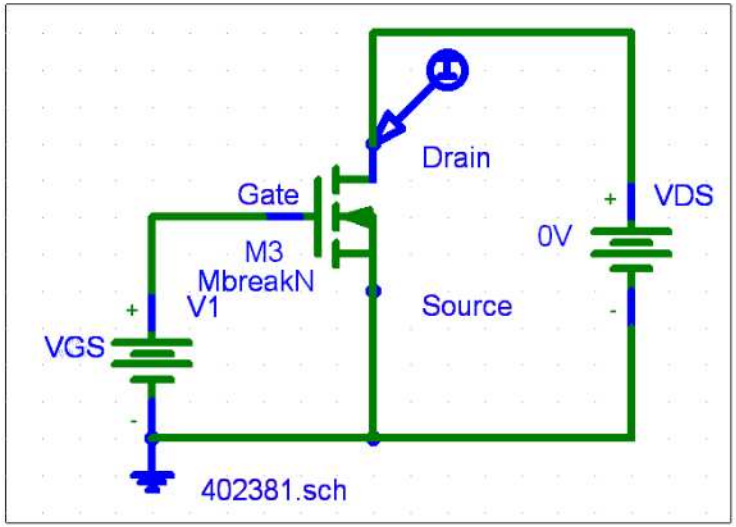
- Different Physics, Some Different Equations. . .
- . . . but Many Similarities
- Similar Materials
  - Silicon
  - P– and N–Doped
- 3 Terminals
  - Emitter $\longleftrightarrow$ Source
  - Base $\longleftrightarrow$ Gate
  - Collector $\longleftrightarrow$ Drain

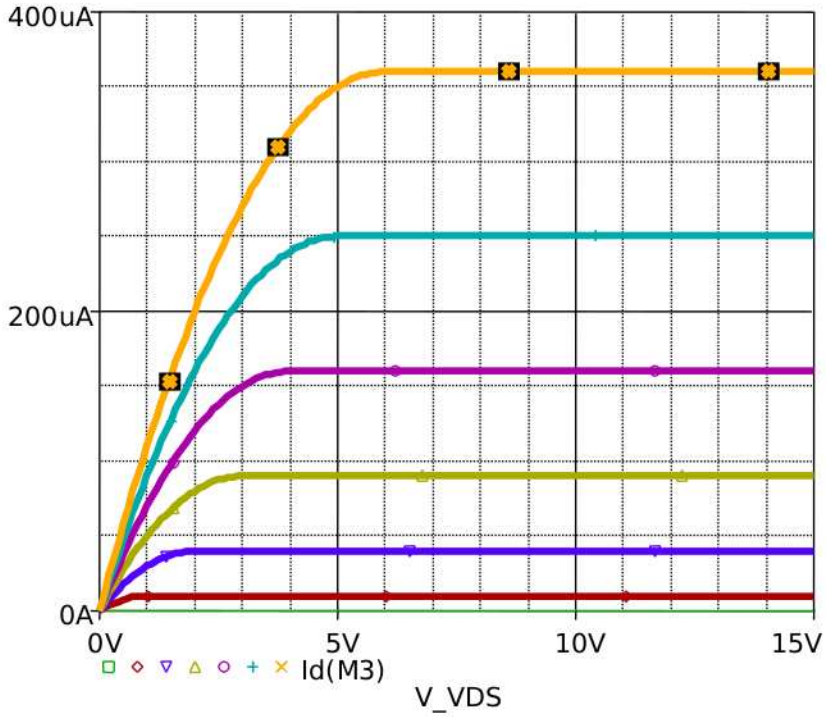
Field–Effect Transistor (2)

- 3 Operating Regions
  - Active $\longleftrightarrow$ Saturation (Amplifiers)
  - Saturation $\longleftrightarrow$ Triode (Logic)
  - Cutoff $\longleftrightarrow$ Cutoff (Logic)

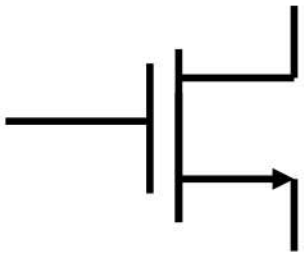
- 3 Amplifers
  - Common Emitter t$\longleftrightarrow$ Common Source (Large A_v)
  - Common Base t$\longleftrightarrow$ Common Gate ($A_i = 1$)
  - Common Collector t$\longleftrightarrow$ Common Drain ($A_v = 1$)

N–FETs in a Nutshell



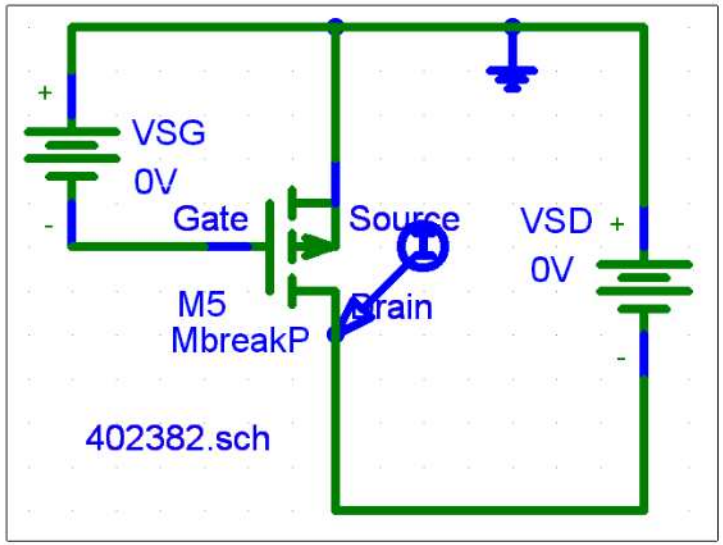


N-Channel FET

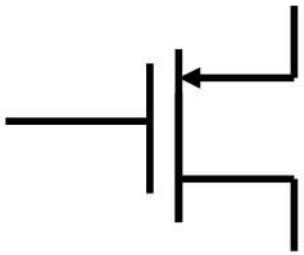


Another Symbol

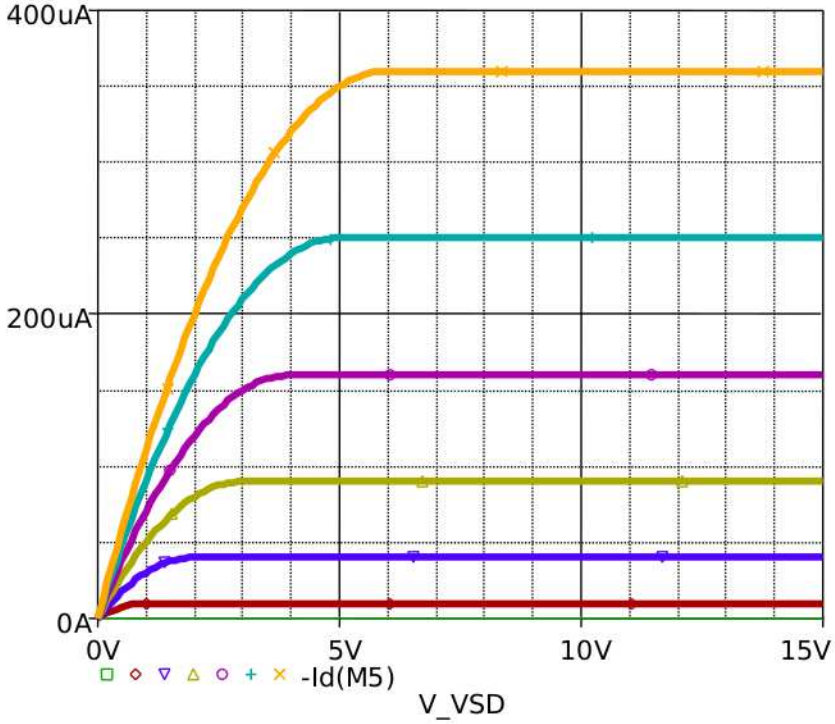
P–FETs in a Nutshell



P-Channel FET



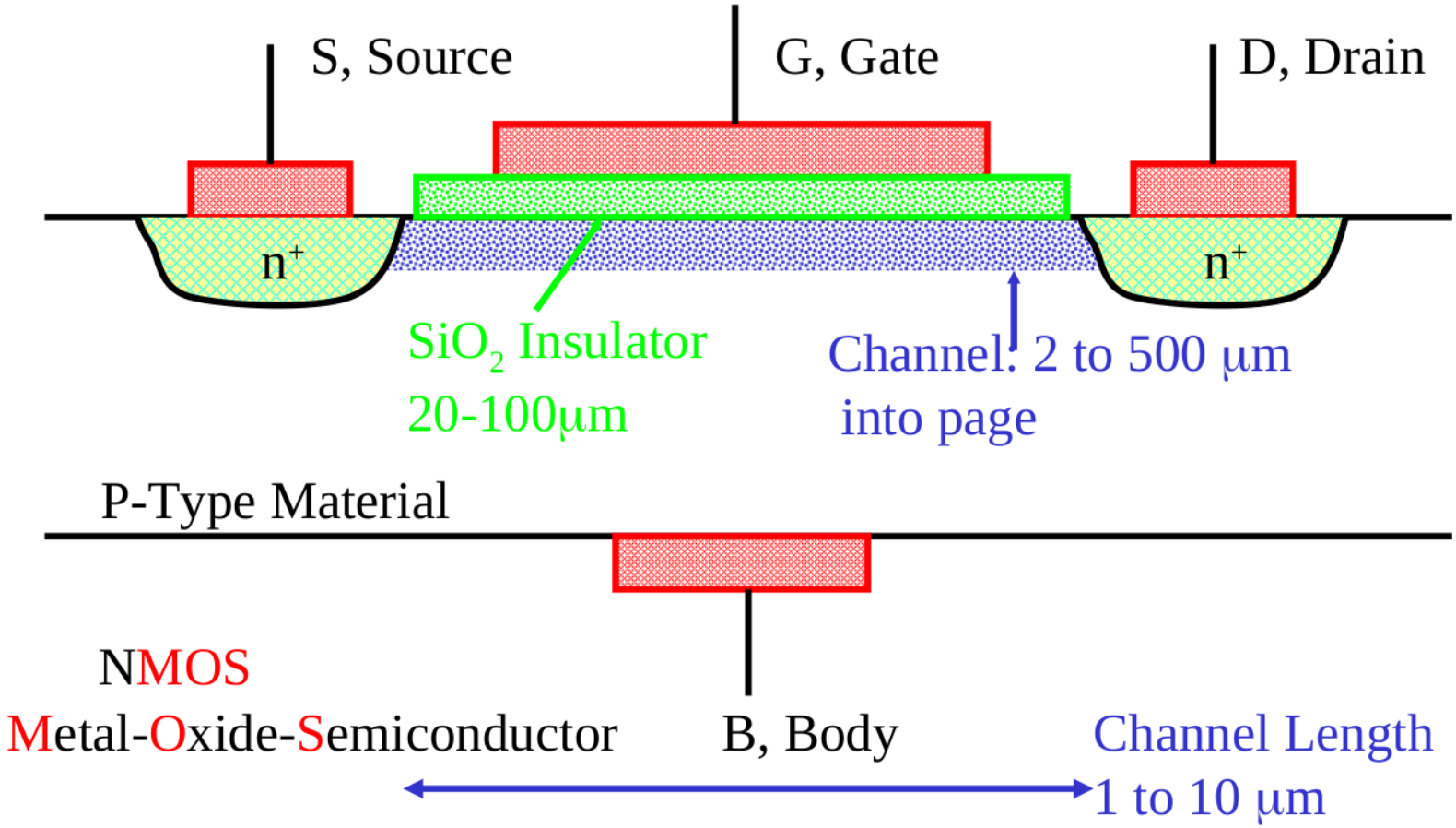
Another Symbol



FET Advantages

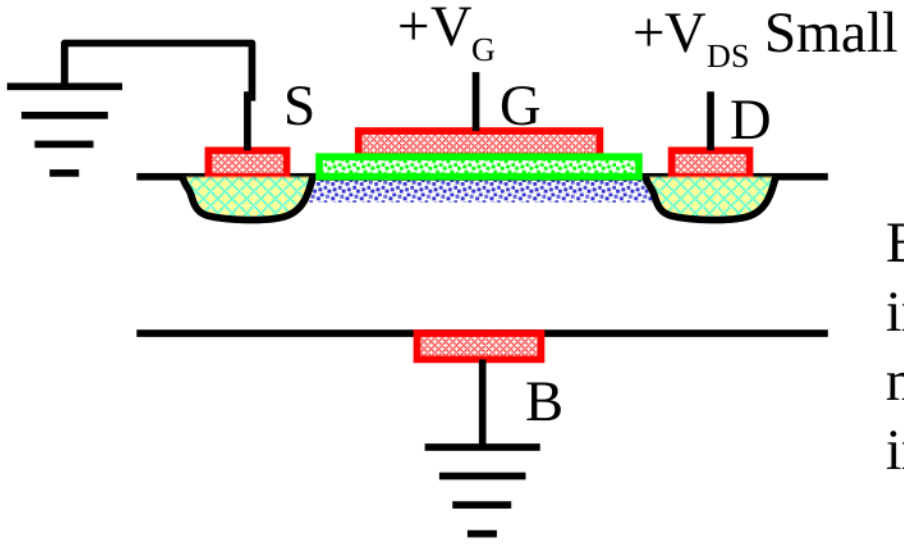
- Small Size
- High Speed
- Mass Production
- Minimal Resistors and Capacitors

N–FET Structure



N–FET at Low V_D (1)

- V_{GS}=*0:* No current (back-to-back diodes)
- Normal Bias Configuration:



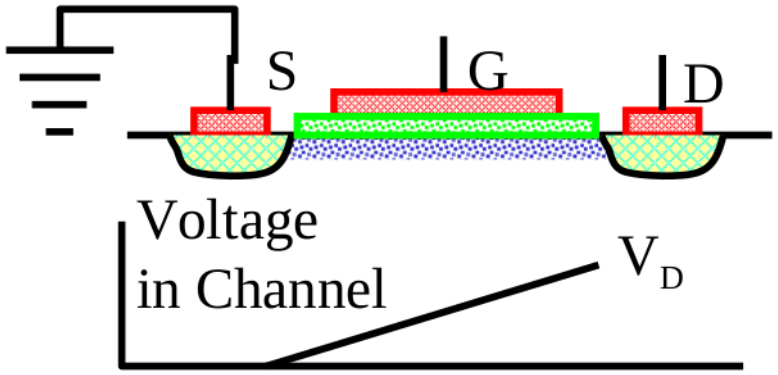
Body tied to source in discretes, and to most negative rail in NMOS.

N–FET at Low V_D (2)

- $V_{GS}>0$: Creates a field in substrate
  - Perpendicular to Channel
  - Moves Minority Carriers “down” into substrate
- Electrons move in from source and drain
  - Create an N-Channel
- Channel Exists at $V_{GS}=V_{Thr}$ (a threshold)
  - Typically $V_{Thr}=1$ *to* 3 Volts
- Carrier Concentration Grows as V_{GS}-V_{Thr}
  - Source-Drain Resistance Goes as $1/(V_{GS}$-$V_{Thr})$

N–FET Pinch–Off (1)

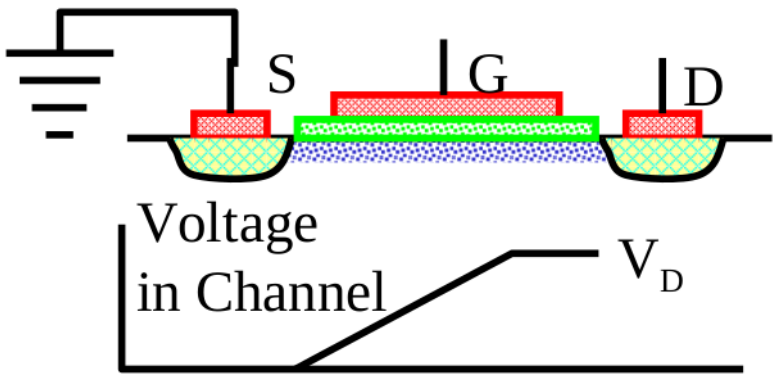
- As Drain Voltage increases, Field Varies with position
  - Lower field to right
  - Smaller channel
  - Lower Conductivity



- Voltage Grows, and Current Stays Almost Constant.

N–FET Pinch–Off (1)

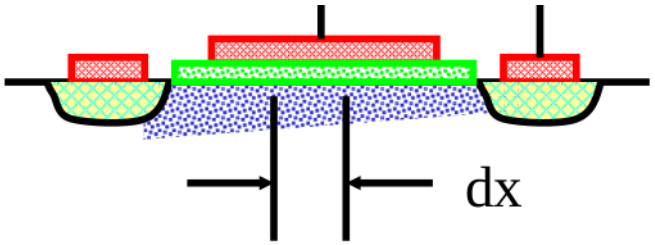
- As Drain Voltage increases, further, pinch-off moves to left
- Channel Length is shorter
- Current goes up



Horizontal Field is higher in pinched region

N–FET Equations (1)

Oxide Capacitance per unit Area $C_{ox} = \frac{\varepsilon_{ok}}{t_{ox}}$



Incremental Charge $dq(x) = - C_{ox} W dx \left[V_{GS} - V(x) - V_{thr} \right]$

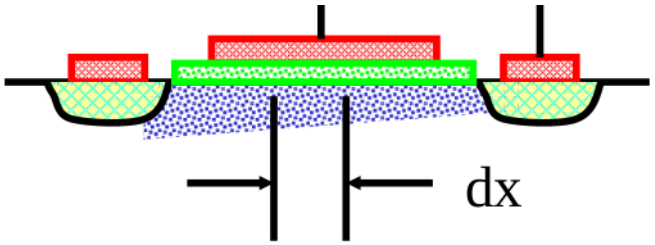
Field Defined: (|| channel) $E(x) = - \frac{dV(x)}{dx}$

Charge Velocity $\frac{dx}{dt} = - \mu_n E(x) = \mu_n \frac{dV(x)}{dx}$

N–FET Equations (2)

Charge Velocity

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dV(x)}{dx}$$



Drain Current

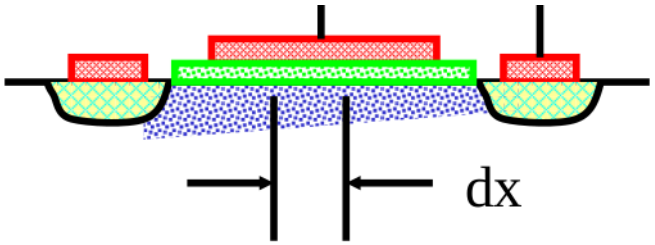
$$i_D = \frac{dq(x)}{dx}\frac{dx}{dt} = \mu_n C_{ox} W \left[V_{GS} - V(x) - V_{thr}\right]\frac{dV(x)}{dx}$$

Drain Current is Independent of x:

$$i_D dx = \mu_n C_{ox} W \left[V_{GS} - V(x) - V_{thr}\right] dV(x)$$

N–FET Equations (3)

$$i_D dx = \mu_n C_{ox} W \left[V_{GS} - V(x) - V_{thr} \right] dV(x)$$



Integrate Both Sides

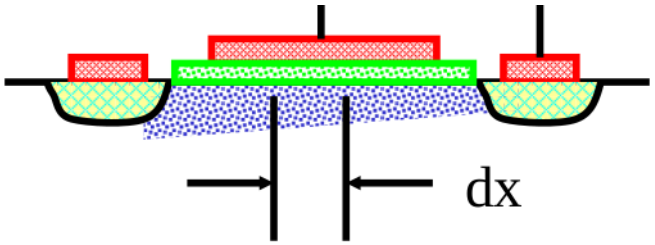
$$\int_0^L i_D dx = \int_0^{V_{DS}} \mu_n C_{ox} W \left[V_{GS} - V(x) - V_{thr} \right] dV(x)$$

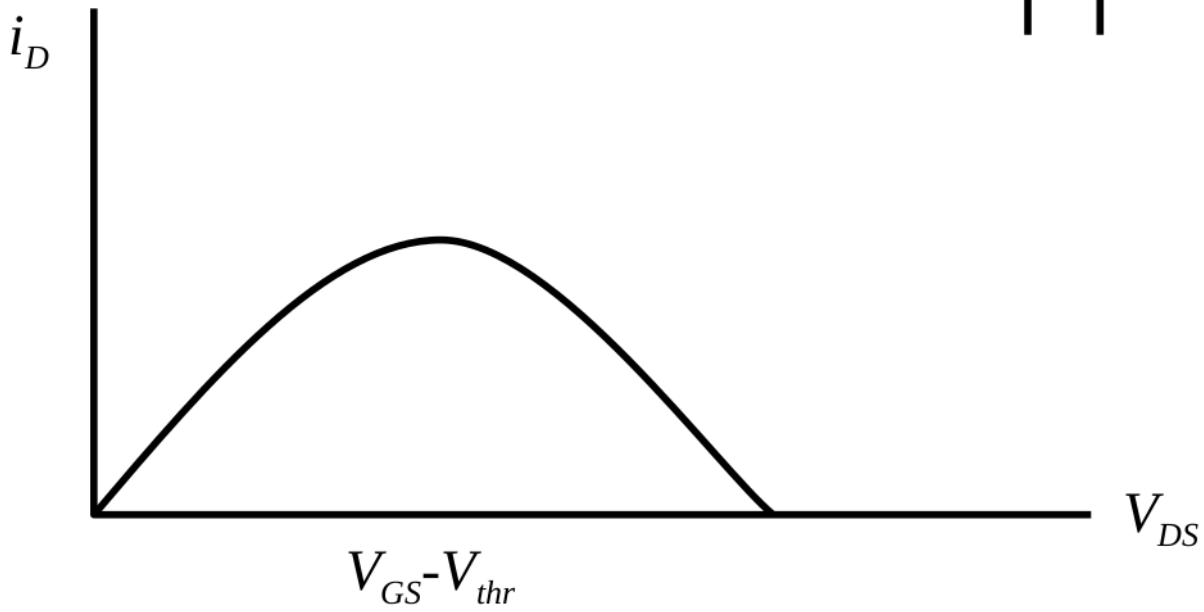
"Triode Region"

$$i_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{thr}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

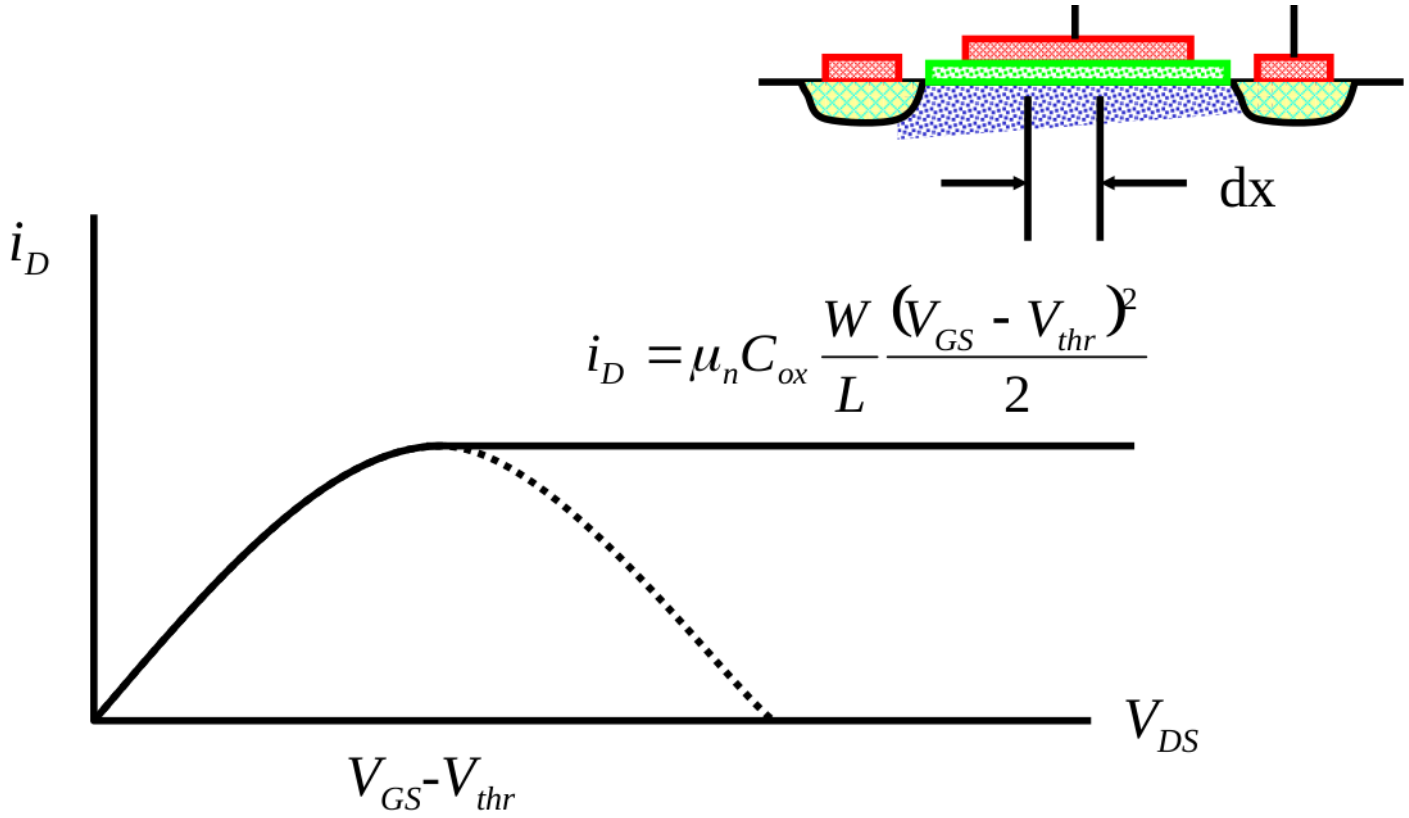
N–FET Equations (4)

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{thr})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$





Saturation Region



Triode–Saturation Boundary

Triode

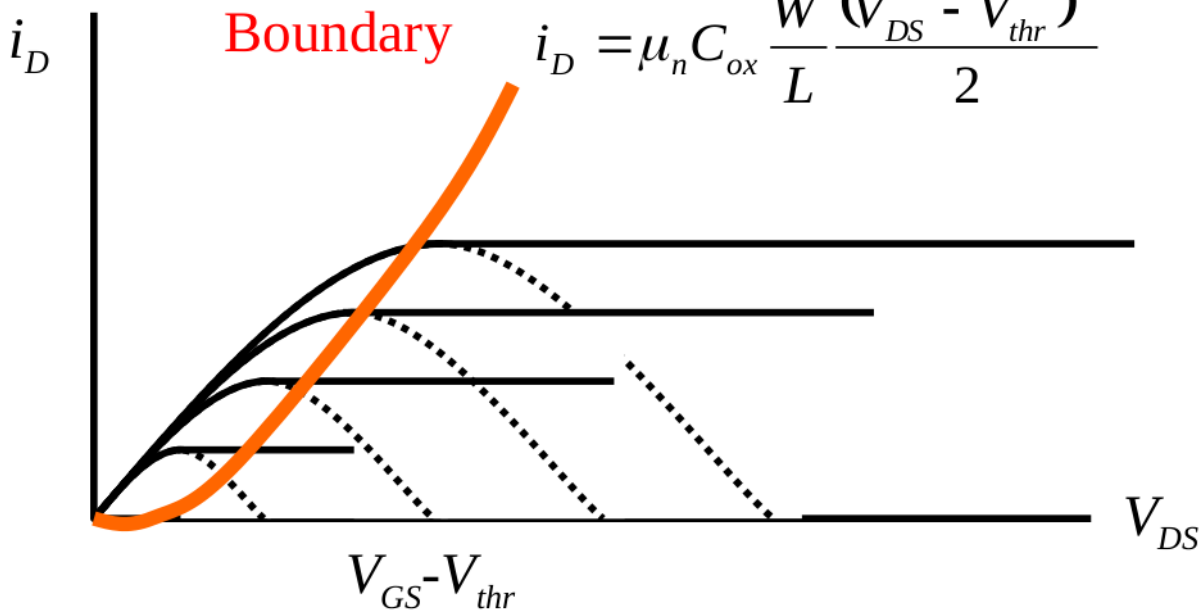
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{thr})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Saturation

$$i_D = \mu_n C_{ox} \frac{W}{L}\frac{(V_{GS} - V_{thr})^2}{2}$$

Boundary

$$i_D = \mu_n C_{ox} \frac{W}{L}\frac{(V_{DS} - V_{thr})^2}{2}$$



Some Comments

- Current goes up with increasing width
- Current goes down with increasing length
- Typical Values:

Process Transconductance Defined $k_n' = \mu_n C_{ox}$

$$20 < k_n' < 100 \mu A/V^2$$

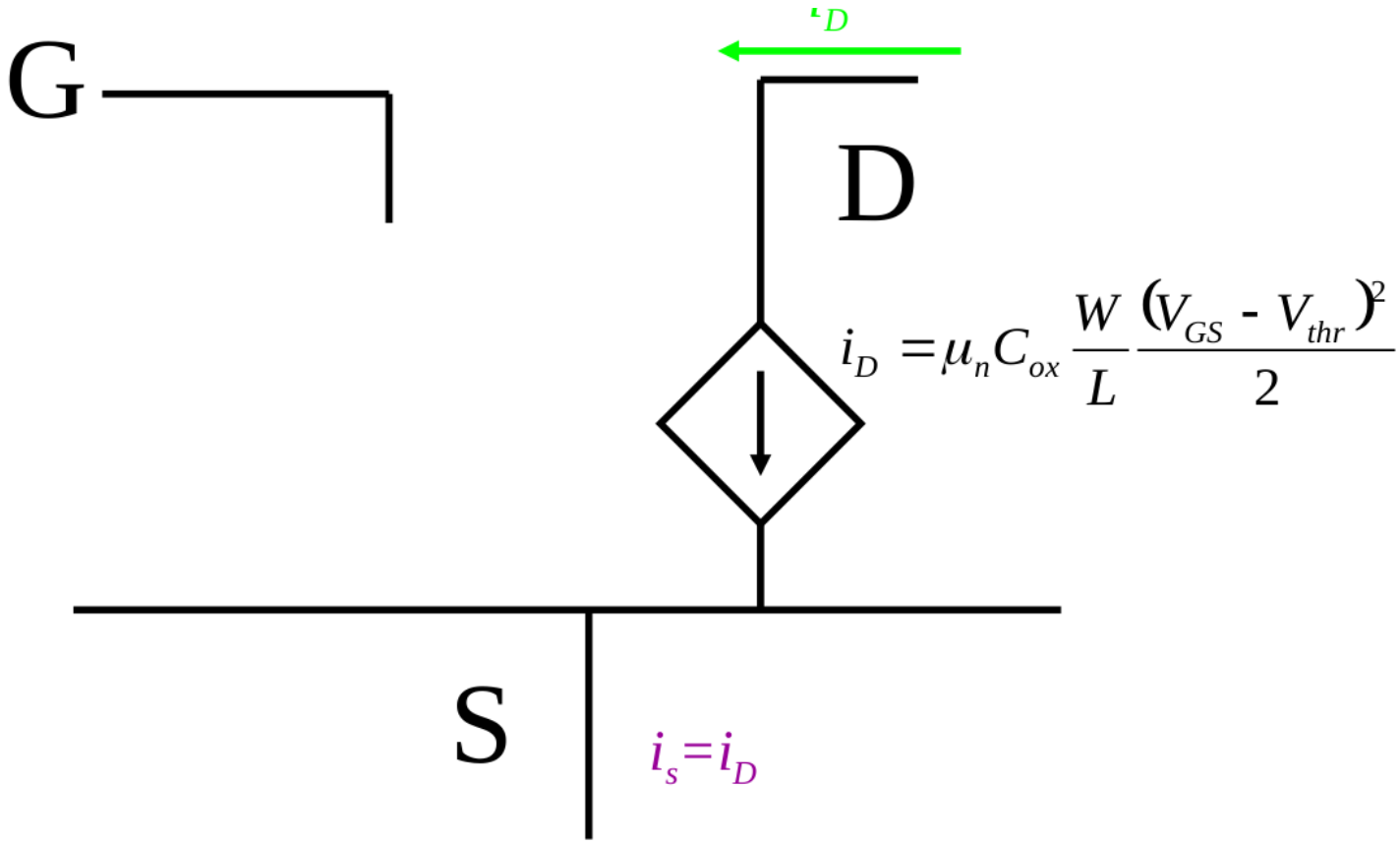
$$2 < \frac{W}{L} < 50$$

Guess: $g_m = k_n' \frac{W}{L} (V_{DS} - V_{thr})$

$$40 < g_m < 5000 \mu A/V$$

Lower than BJT (40 mA/V)!

The Pi Model in Saturation



The Early Voltage

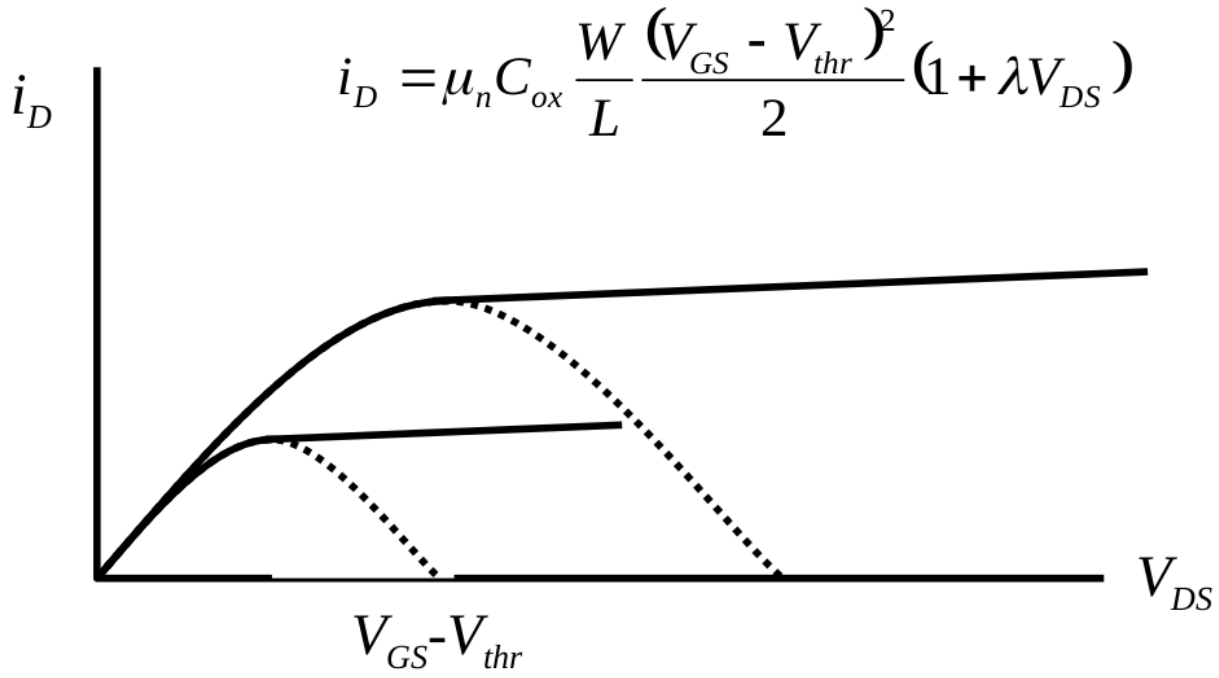
- Effect of Pinch Off as Resistance
  - Increasing Current with Voltage

Previous Eqn. for Saturation $$i_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2}$$

Modified $$i_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2} (1 + \lambda V_{DS})$$

$$\lambda = \frac{1}{V_A}$$

I–V Curves with Early Voltage

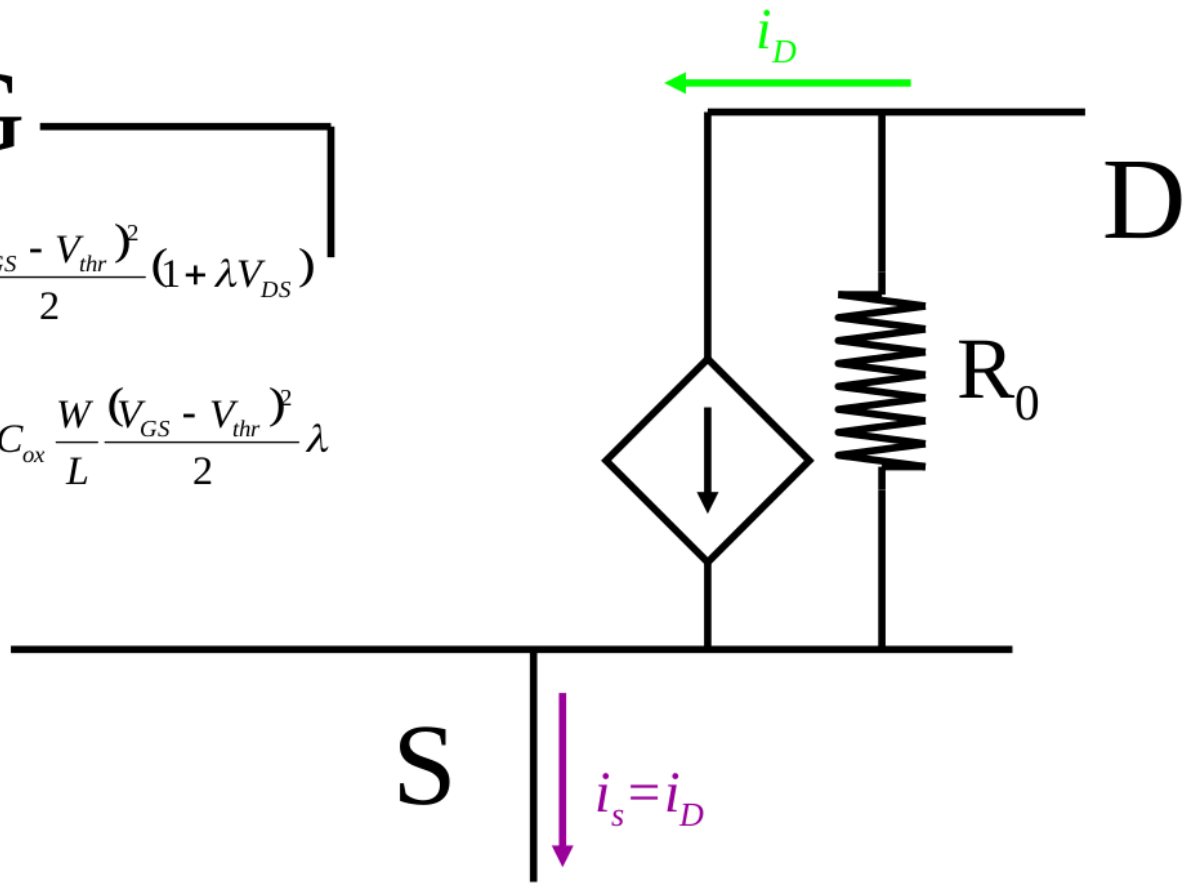


Early Voltage in Model

$$i_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2} (1 + \lambda V_{DS})$$

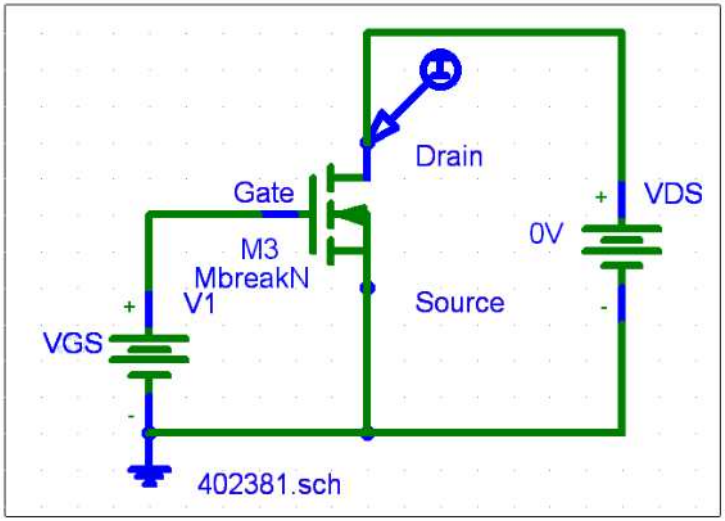
$$\frac{1}{R_0} = \frac{di_D}{dV_{DS}} = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2} \lambda$$

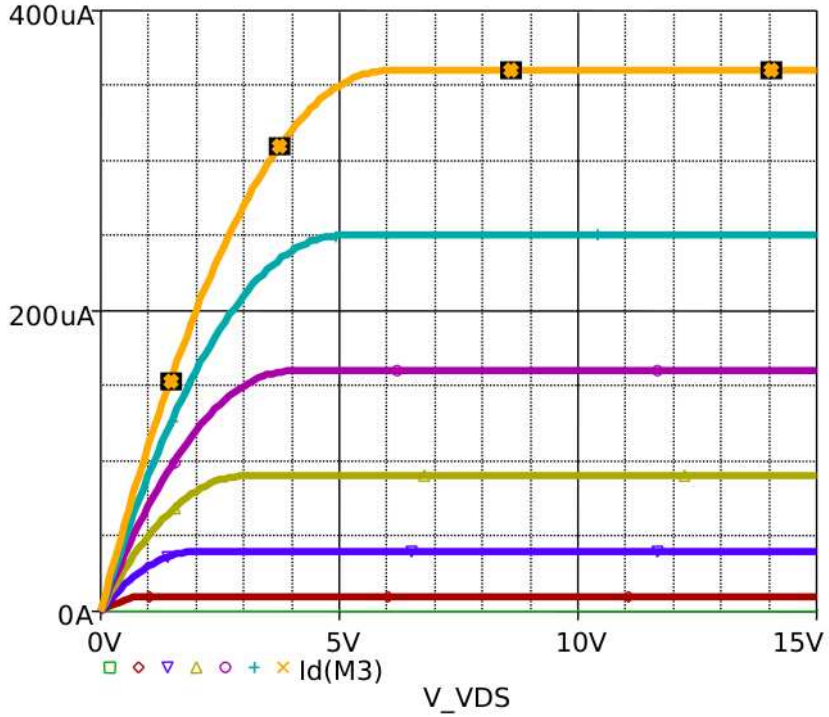
$$= \frac{1}{\lambda I_D^{(DC)}} = \frac{V_A}{I_D^{(DC)}}$$



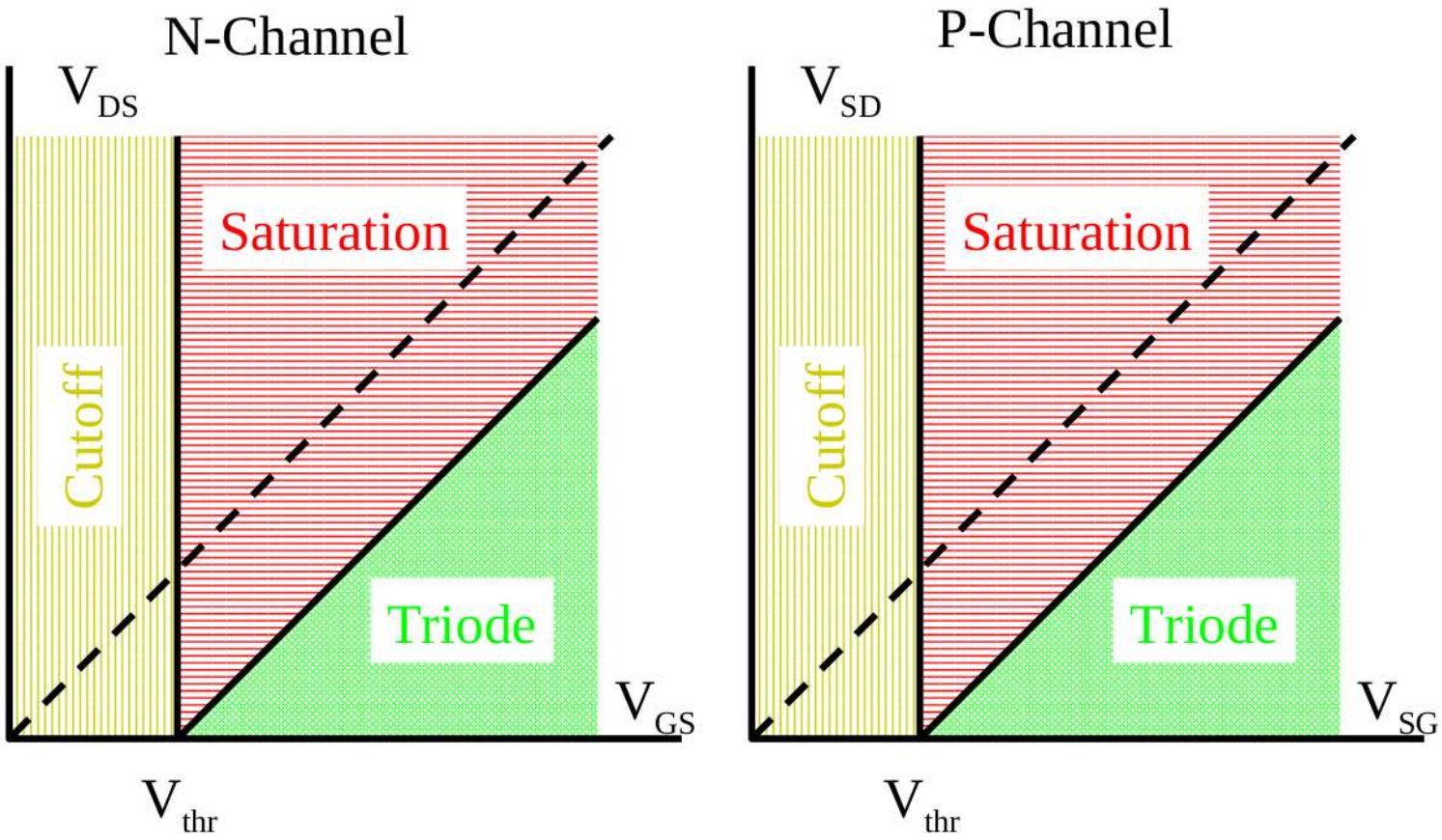
Terminal Characteristics

- V_{GS}=[0:1:6]V

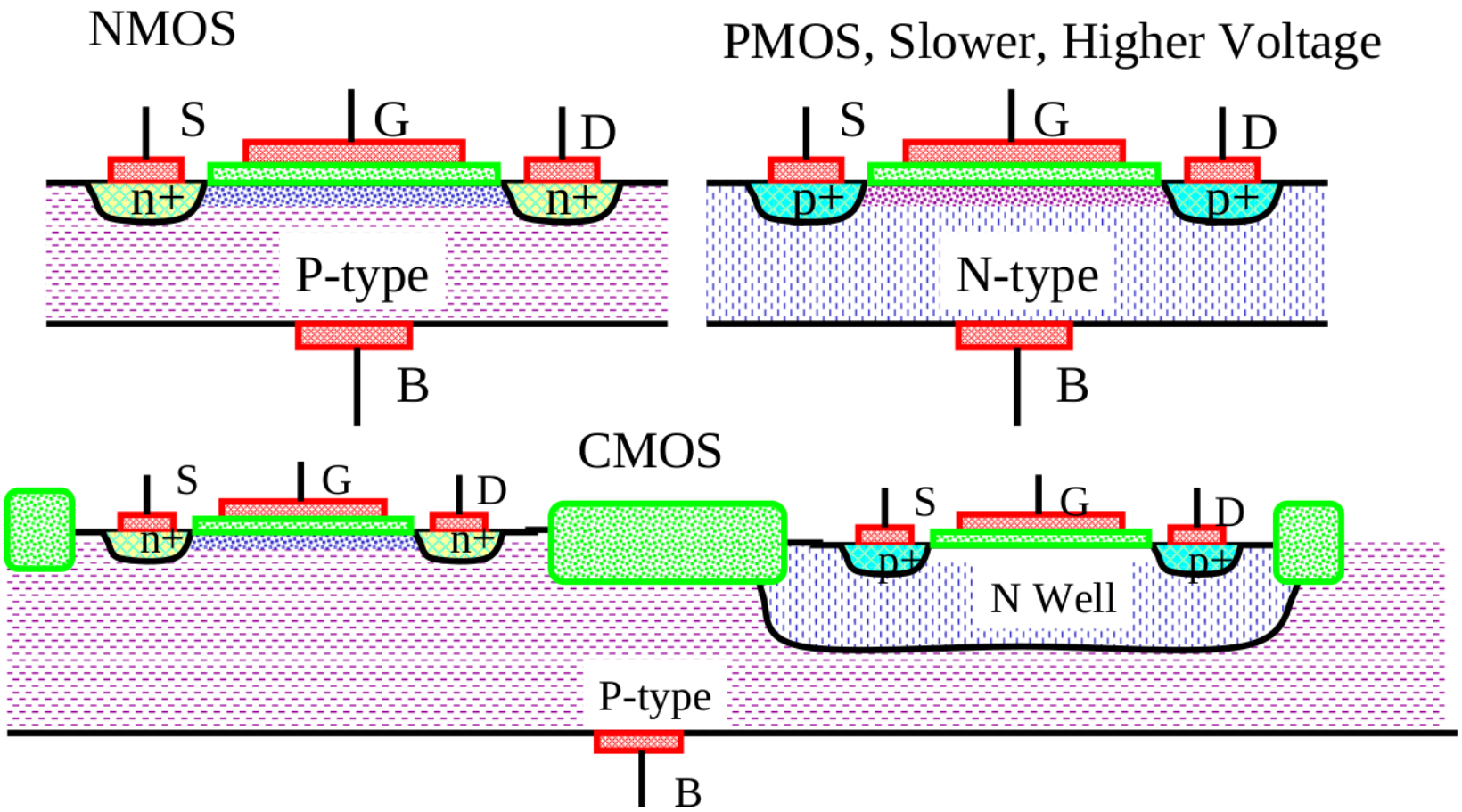




REgions of FET Operation



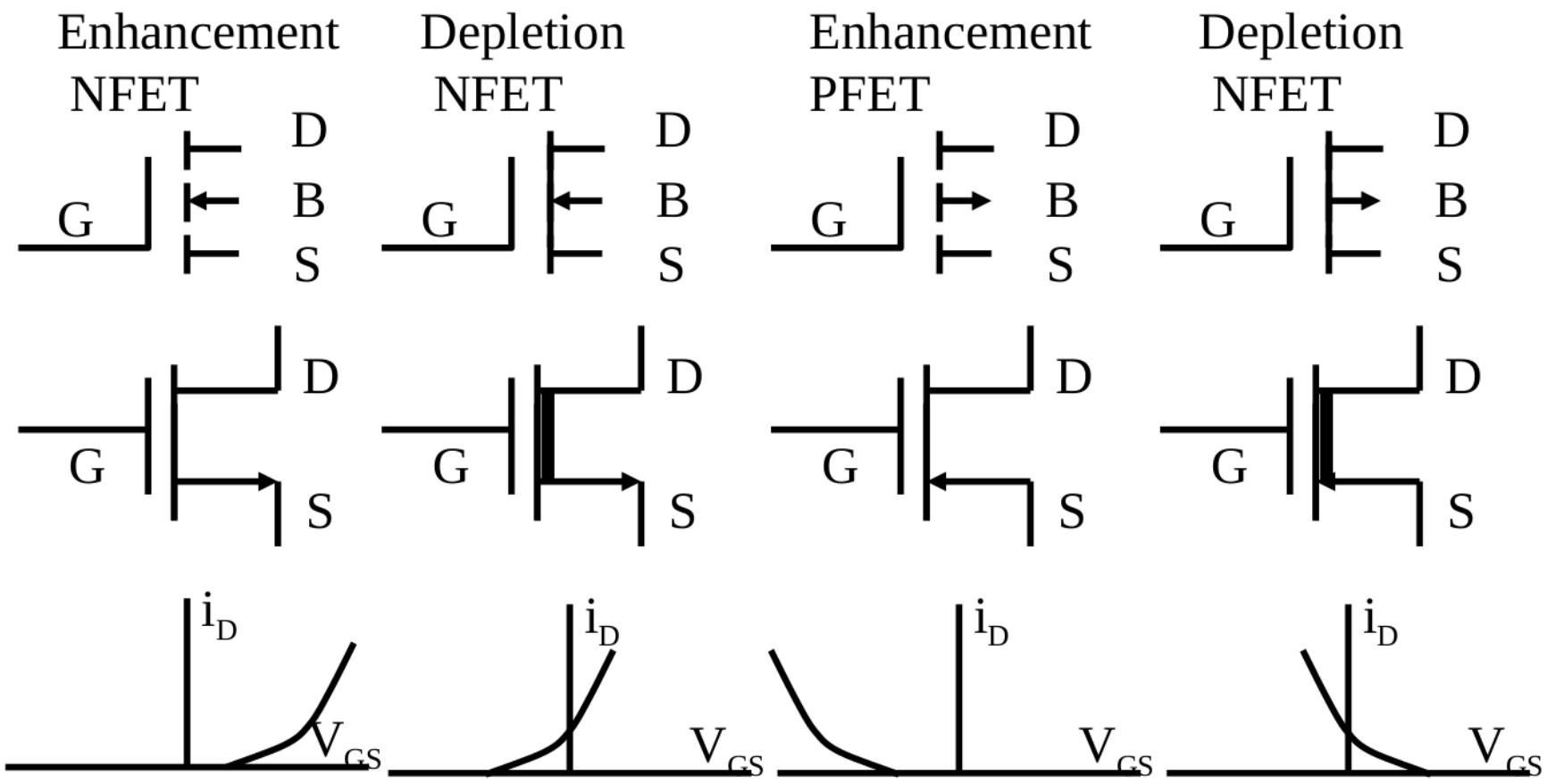
NMOS, PMOS, CMOS



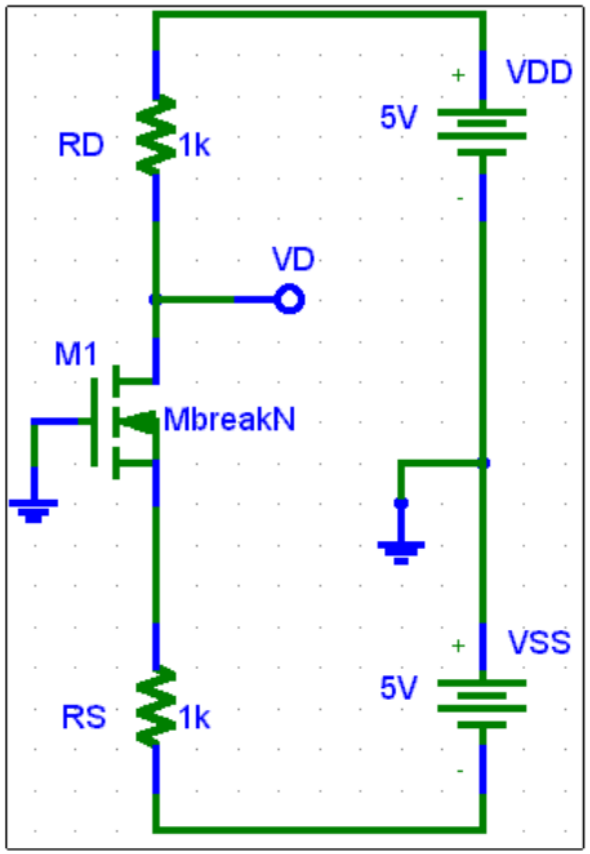
Depletion FET

- Implant a channel (n-type in n-channel)
- Current flows at $V_{GS}=0$, for any V_{DS}
- $V_{GS}>0$ Enhances Channel
- $V_{GS}<0$ Depletes Channel
- And Eventually $V_{GS}<V_{thr}$ Cuts off Channel

Circuit Symbols



DC FET Circuit Example (5.1)



Given:

L=10 μm, W =400 μm

k'_n=20 μA/V^2, λ=0

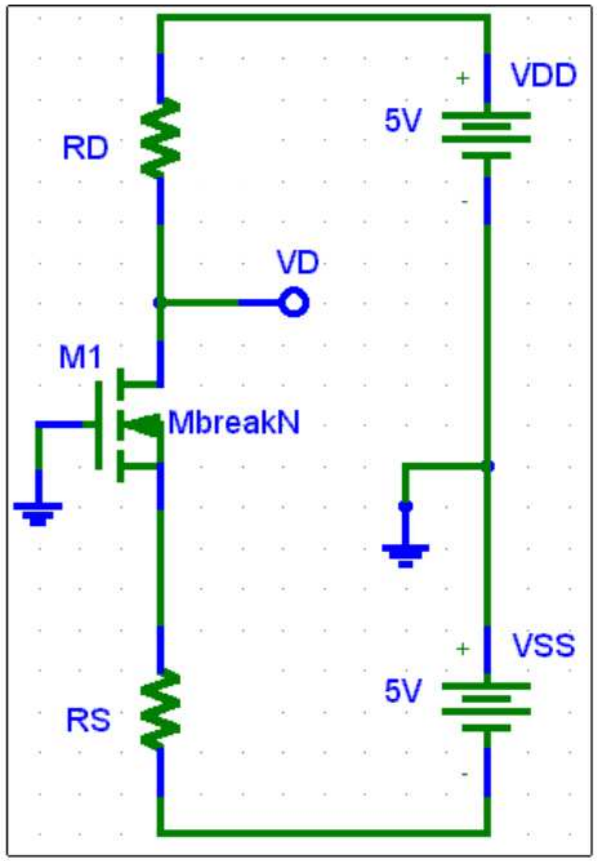
V_{thr}=2V

Goal:

I_D=0.4mA

V_D=1V

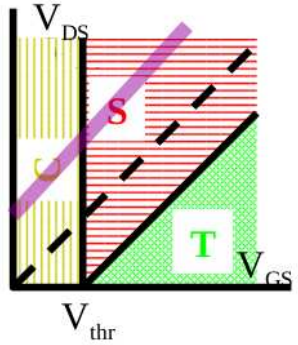
Solution to 5.1 (1)



1 Saturation, Cutoff or Triode?

$V_{DG} = 1\text{V}$

$V_{DS} = V_{GS} + 1\text{V}$

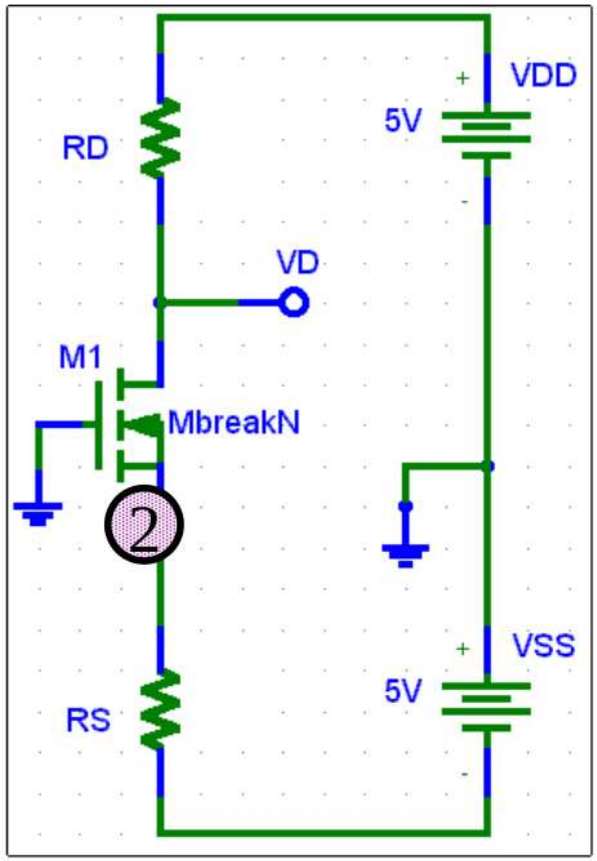


Either Saturation or Cutoff (assume saturation).

2

$$i_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2}$$

Solution to 5.1 (2)



2

$$i_D = k'_n \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2}$$

$$V_{GS} - V_{thr} = \sqrt{\frac{2L}{Wk'_n} i_D} =$$

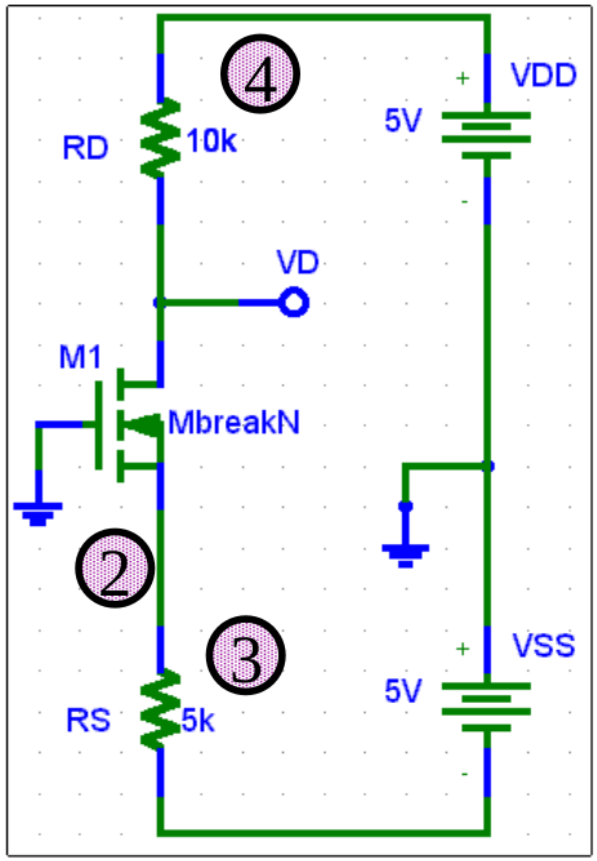
$$\sqrt{\frac{2 \times 10\mu\,\mathrm{m}}{400\mu\,\mathrm{m} 20\mu\mathrm{A/V}^2} 0.4\mathrm{mA}}$$

$$= \pm 1\mathrm{V}$$

V_{GS}=1V (I_D=0, Not True) or

V_{GS}=3V

Solution to 5.1 (3)



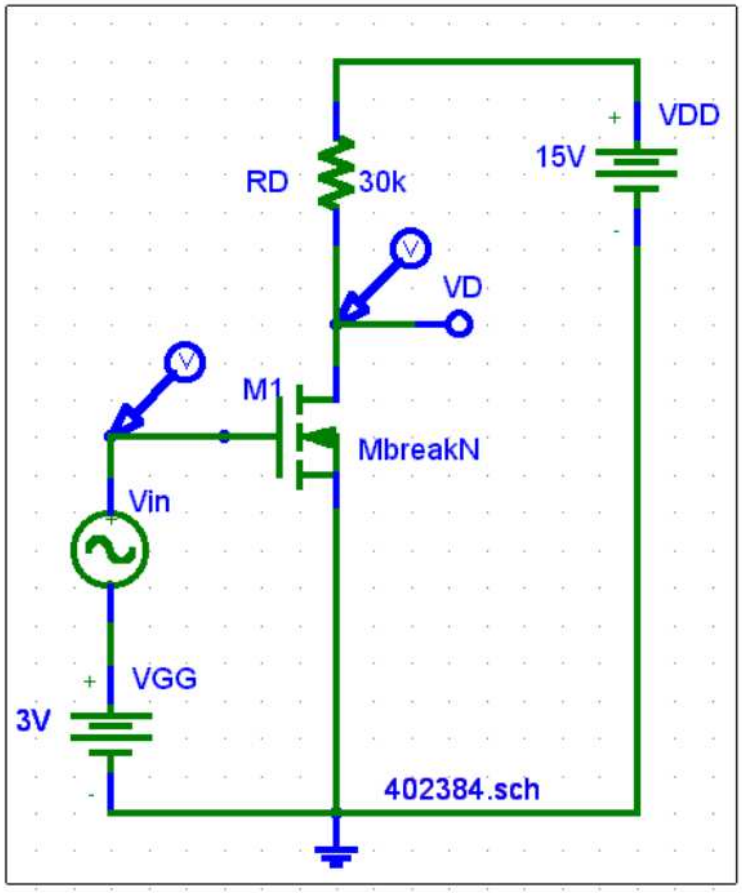
V_{GS}=3V

V_S=-3V

3 $R_S = \frac{\lfloor(-3)-(-5)\rfloor \text{V}}{0.4\text{mA}} = 5k\Omega$

4 $R_D = \frac{\lfloor 5-1 \rfloor \text{V}}{0.4\text{mA}} = 10k\Omega$

FET Amplifier Concept



This is not a good circuit, but we will use it for illustration

Assume Saturation:

$$I_D^{(DC)} = k'_n \frac{W}{L} \frac{\left(V_{GS}^{(DC)} - V_{thr}\right)^2}{2}$$

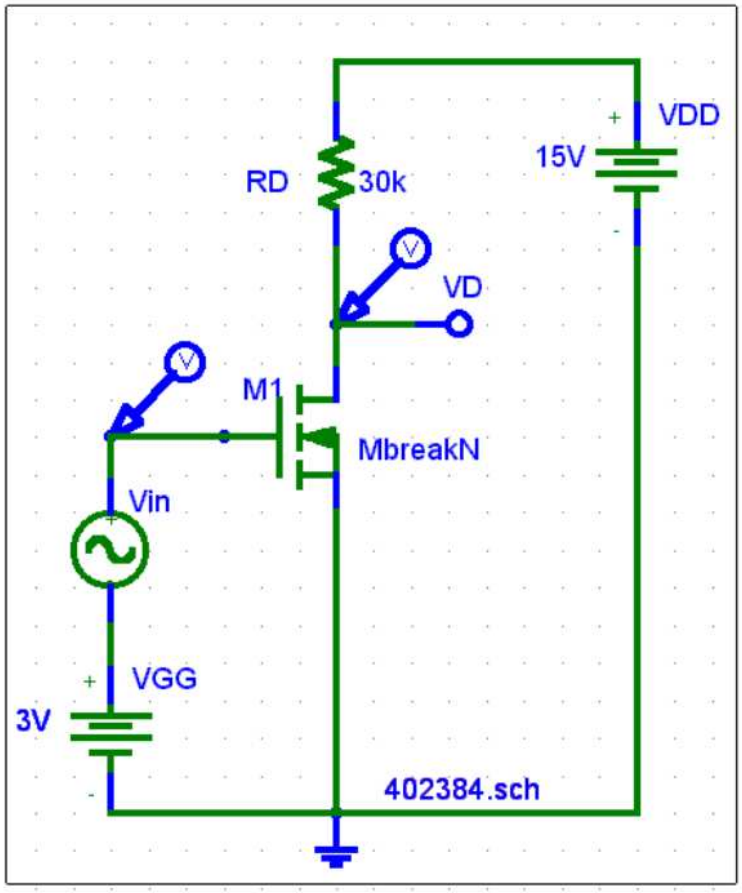
Circuit Equation

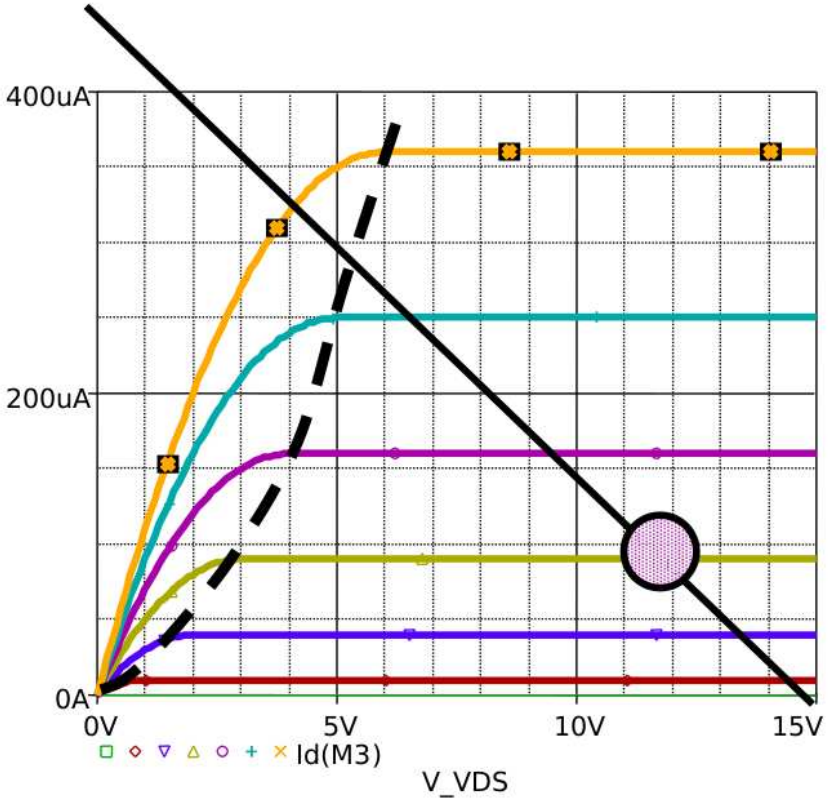
$$V_{DS}^{(DC)} = V_{DD} - R_D I_D^{(DC)}$$

Solve Simultaneously

Check $V_{DS}^{(DC)} > V_{GS}^{(DC)} - V_{thr}$

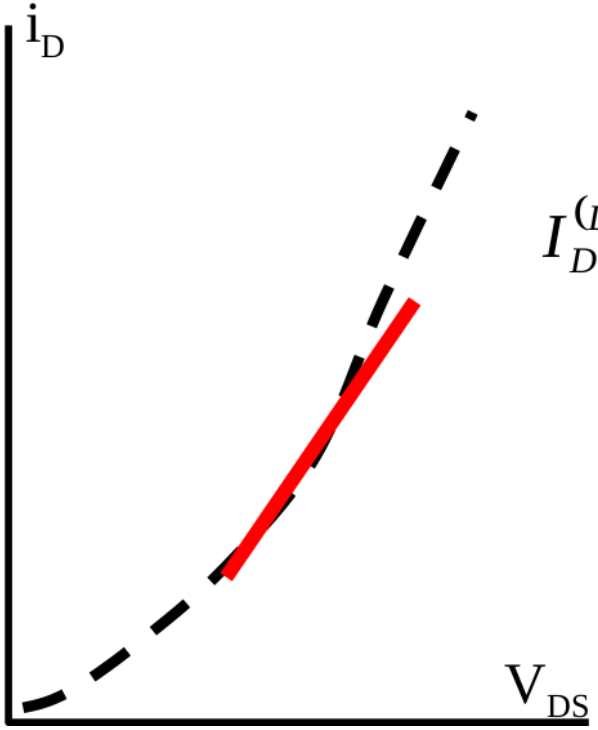
Operating Point Graphically





AC Performance (1)

$$i_D = k'_n \frac{W}{L} \frac{(v_{GS} - V_{thr})^2}{2}$$



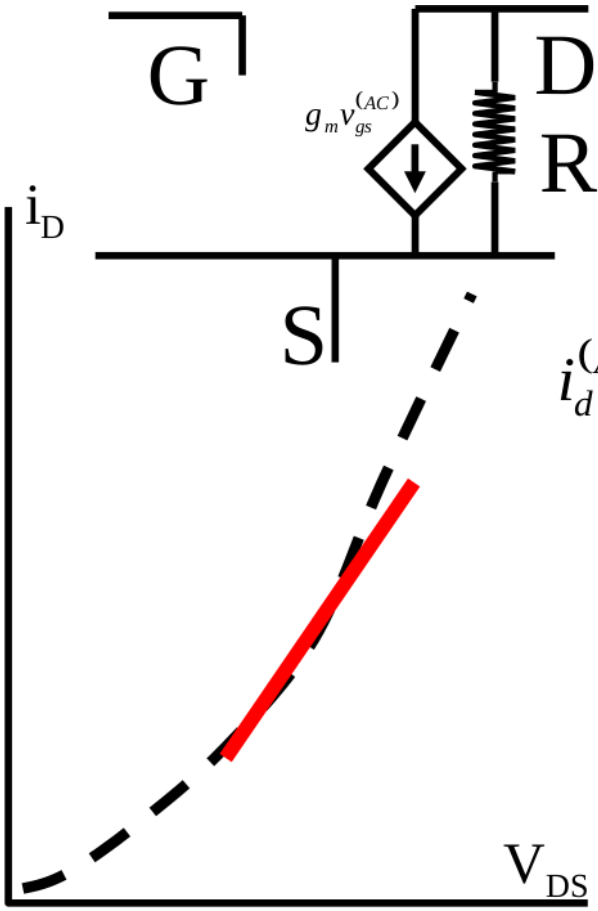
$$i_D = k'_n \frac{W}{L} \frac{(V_{GS}^{(DC)} - V_{thr})^2}{2} + k'_n \frac{W}{L}(V_{GS}^{(DC)} - V_{thr})v_{gs}^{(AC)}$$

$$I_D^{(DC)} + i_d^{(AC)} \approx k'_n \frac{W}{L} \frac{(V_{GS}^{(DC)} + v_{gs}^{(AC)} - V_{thr})^2}{2}$$

$$I_D^{(DC)} = k'_n \frac{W}{L} \frac{(V_{GS}^{(DC)} - V_{thr})^2}{2}$$

$$i_d^{(AC)} \approx k'_n \frac{W}{L}(V_{GS}^{(DC)} - V_{thr})v_{gs}^{(AC)}$$

AC Performance (2)



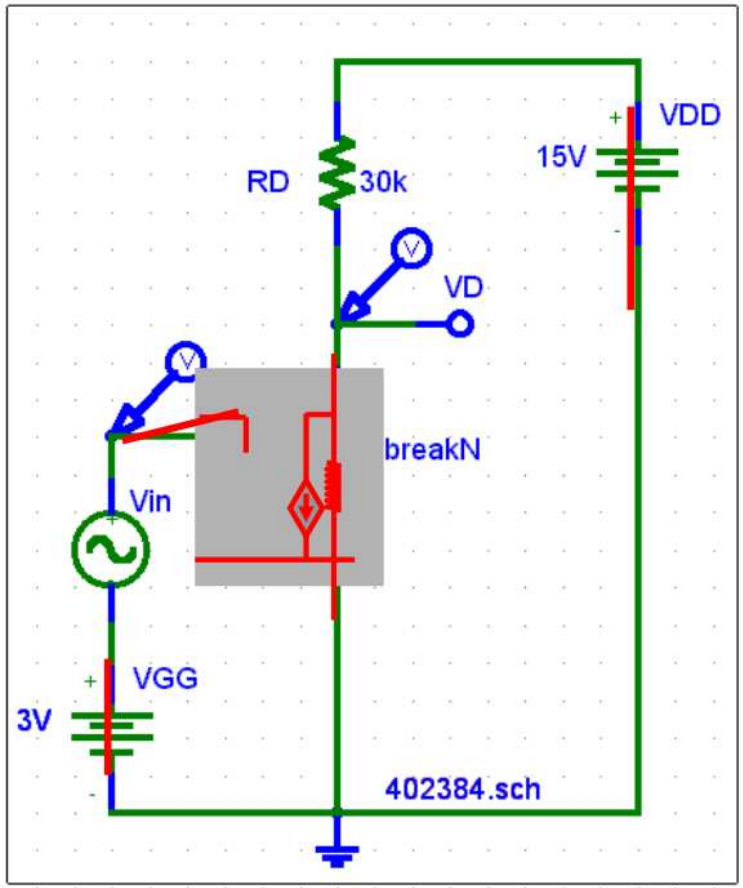
$$I_D^{(DC)} = k'_n \frac{W}{L} \frac{\left(V_{GS}^{(DC)} - V_{thr}\right)^2}{2}$$

$$i_d^{(AC)} \approx k'_n \frac{W}{L}\left(V_{GS}^{(DC)} - V_{thr}\right) v_{gs}^{(AC)} = g_m v_{gs}^{(AC)}$$

$$g_m = k'_n \frac{W}{L}\left(V_{GS}^{(DC)} - V_{thr}\right)$$

$$g_m = \frac{2I_D^{(DC)}}{\left(V_{GS}^{(DC)} - V_{thr}\right)}$$

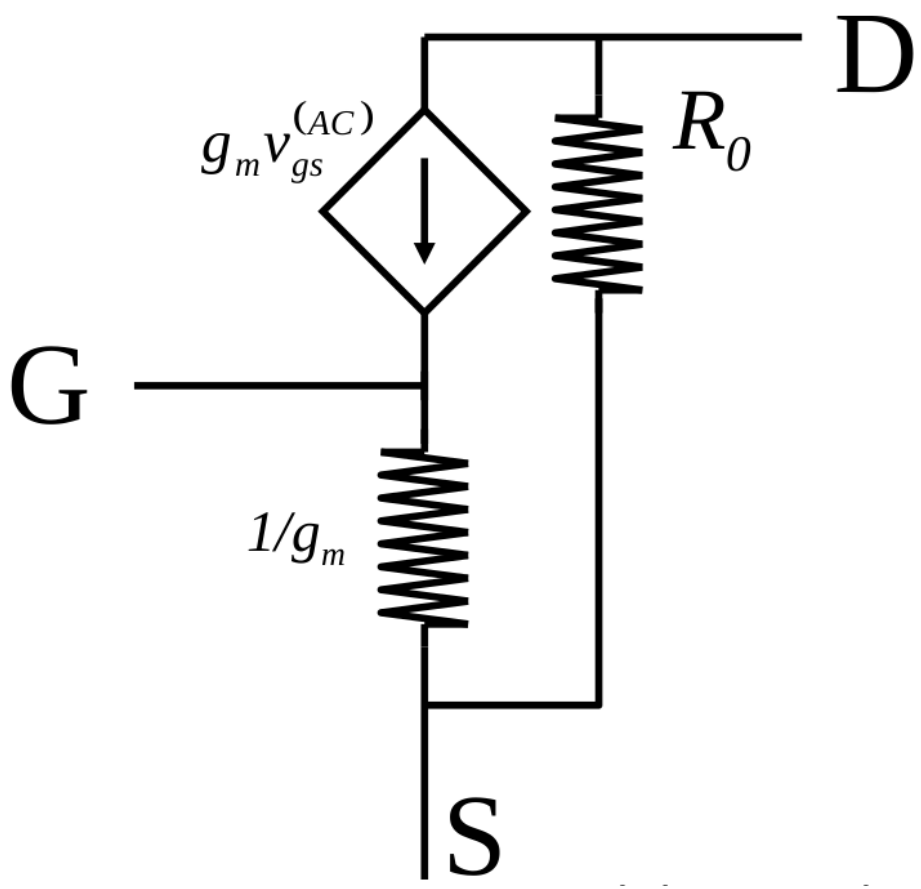
Small–Signal Pi Model



Voltage Gain

$$A_v = - g_m (R_D \parallel R_0)$$

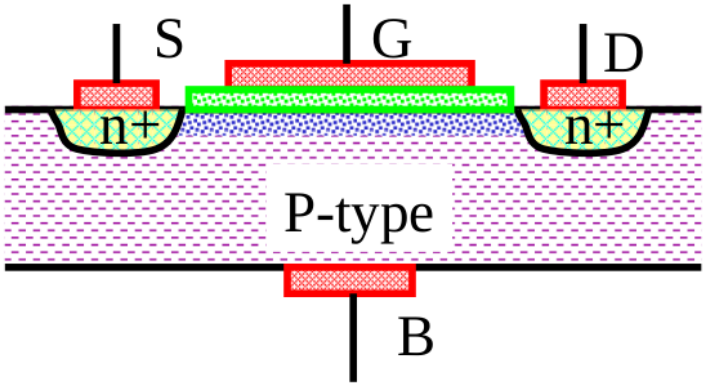
Small–Signal Tee Model



Because the gate current is zero, the source resistor must have the same current as the current source. Therefore it must have the value $1/g_m$.

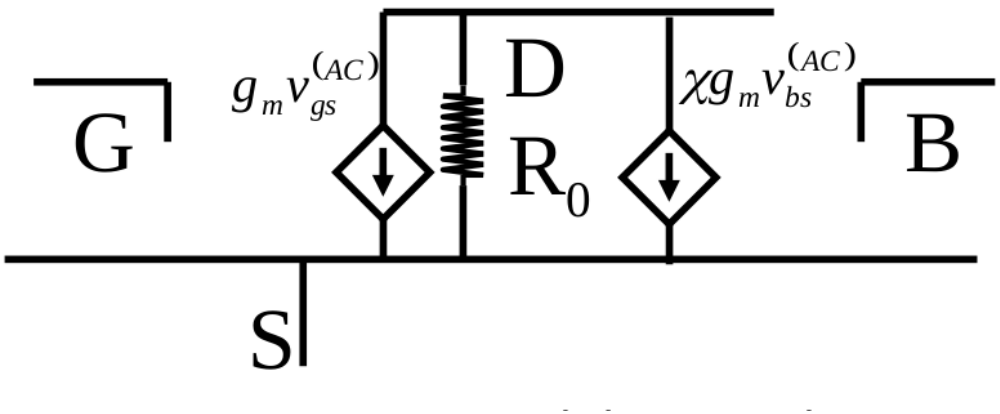
The current source can be described either by a current-controlled source with gain 1, or a voltage-controlled source with transconductance, g_m

Body Effect



Body acts like a second gate

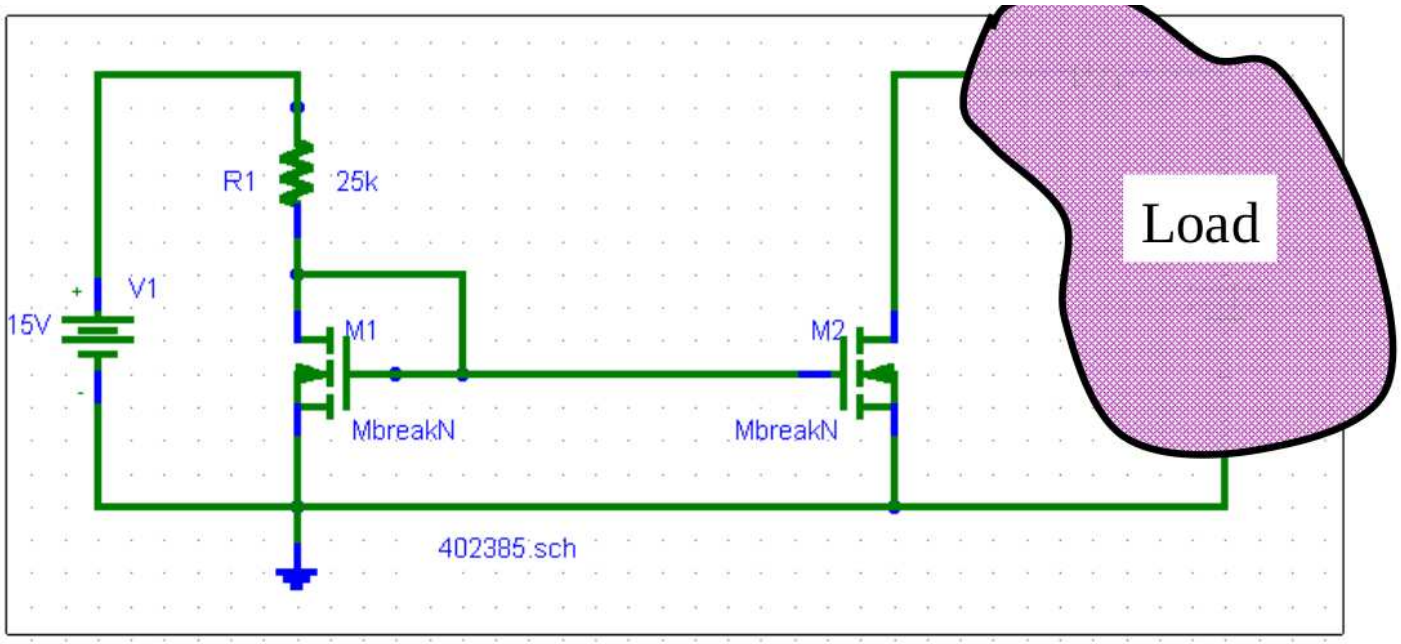
$$0.1 < \chi < 0.3$$



Pi Model

Note that in discrete FET circuits, the body is usually tied to the source. $v_{bs}^{(AC)} = 0$

Bias with a Current Source (1)



$$V_{GS1}^{(DC)} = V_{GD1}^{(DC)}$$

Ensures Saturation

Transistor M1 Establishes Reference Current. Transistor M2 Reflects it to the rest of the circuit (Load)

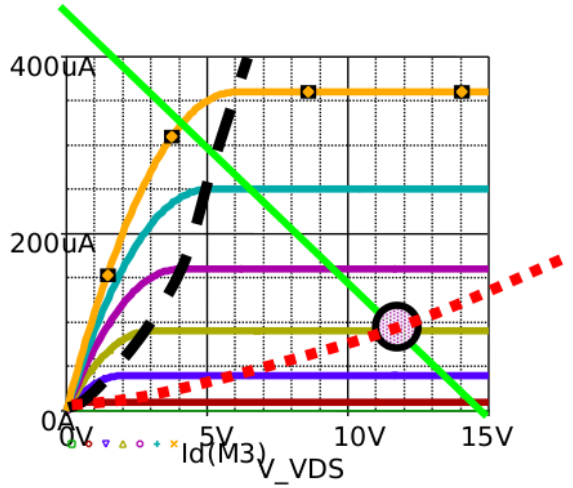
Bias with a Current Source (2)

Transistor Equation ..... Circuit Equation ——

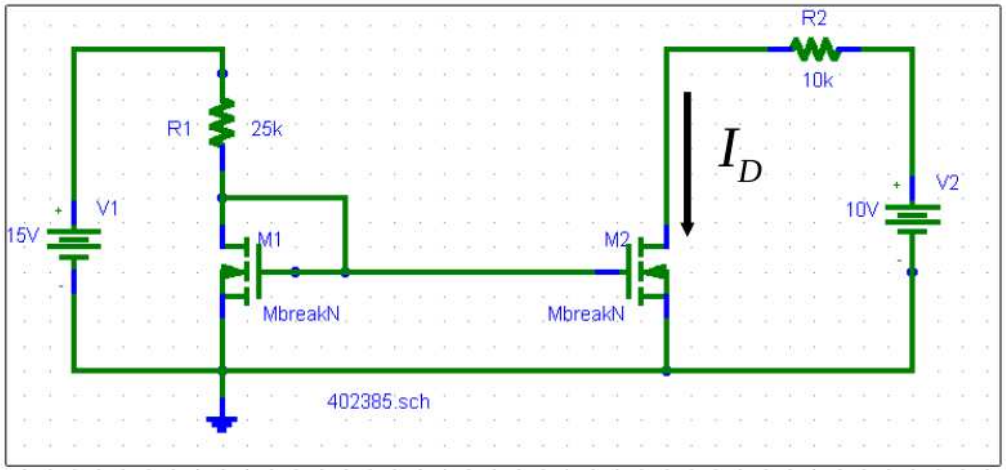
$$I_{D1}^{(DC)} = k'_n \frac{W}{L} \frac{\left(V_{GS}^{(DC)} - V_{thr}\right)^2}{2} \qquad I_{D1}^{(DC)} = \frac{V_{DD} - V_{DS}^{(DC)}}{R_D} = \frac{V_{DD} - V_{GS}^{(DC)}}{R_D}$$

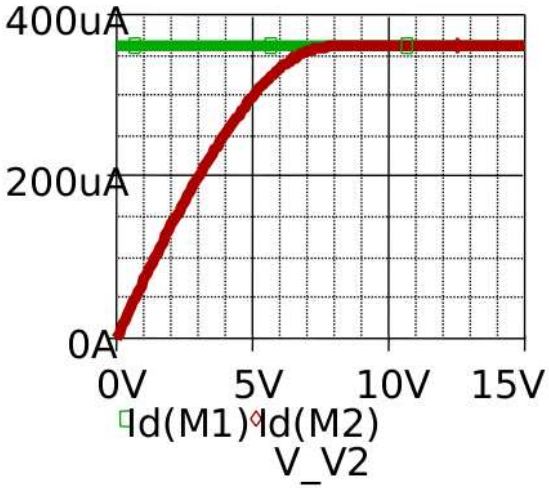
Pick $_{ID,}$ Solve for V_{GS} One Equation, Two Unknowns: V_{DD} and R_D

This sets the current through M1 and its gate voltage, and thus the gate voltage of M2. The current through M2 will be the same, provided that M2 remains in saturation.



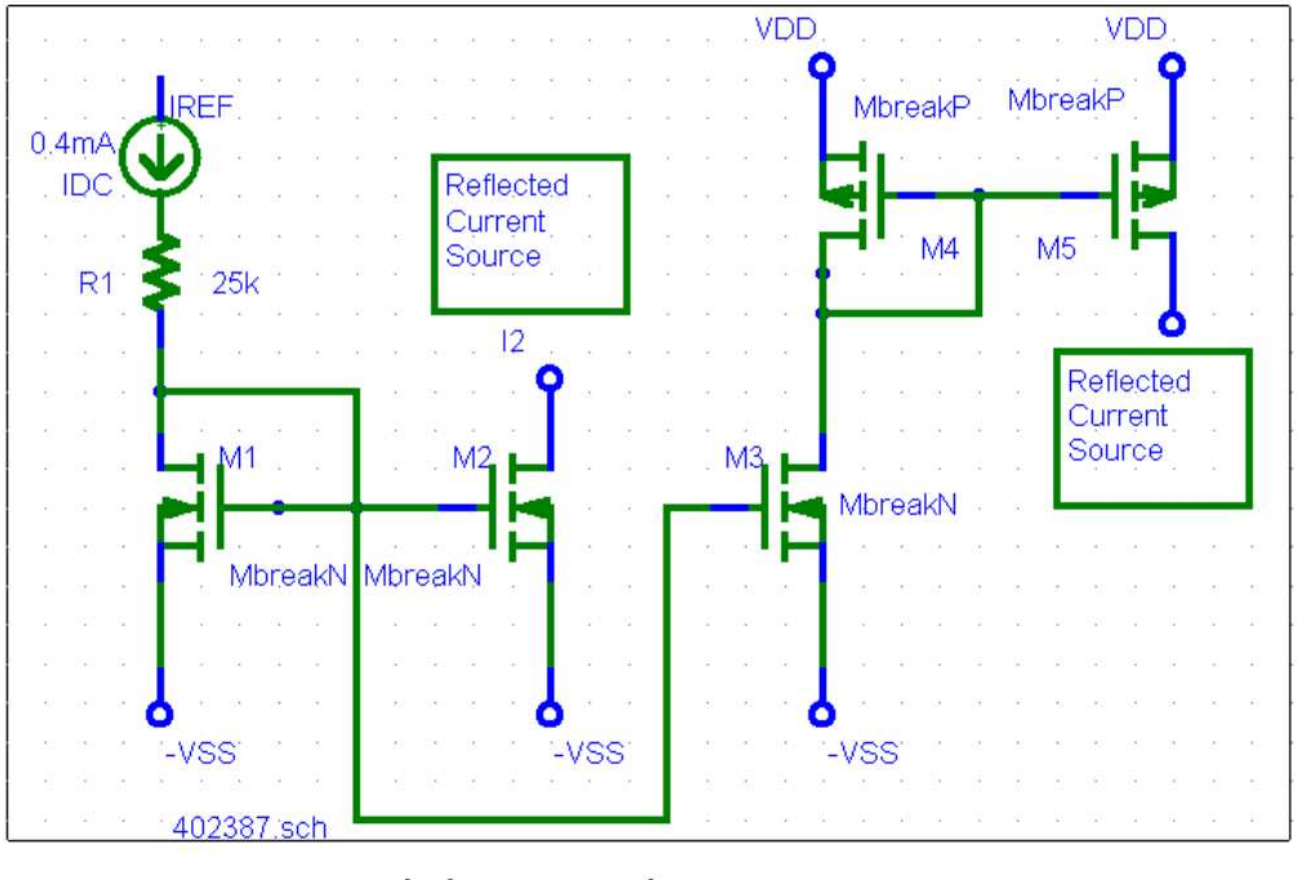
Current Mirror





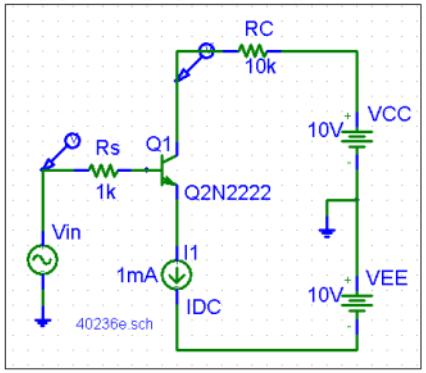
R2 and V2 represent some circuit, (the amplifier). Provided that it doesn't do anything too strange, I_D will remain constant. Thus, the circuit above, minus these two components, is a DC current source. In the AC model, it is a resistor of value R_0, which can serve as the load resistor for the amplifier.

Current Steering Circuit

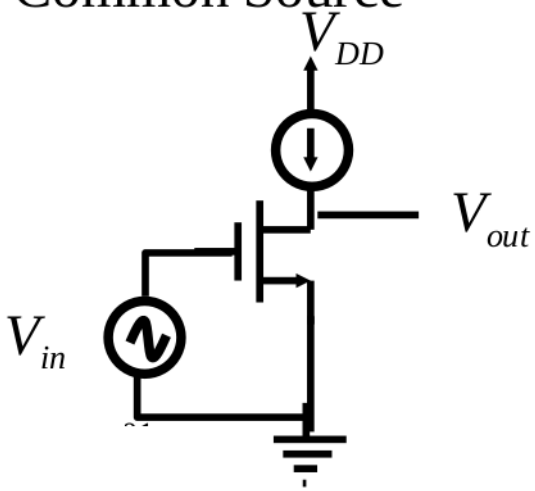


FET Amplifiers

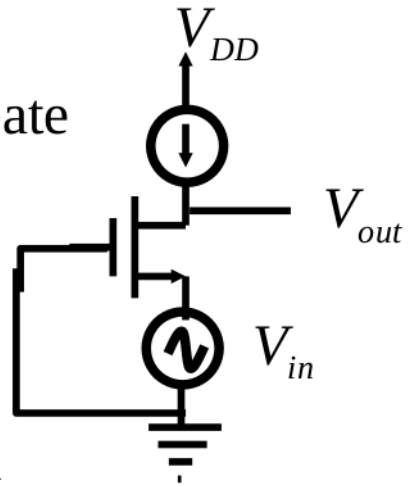
Recall Common Emitter



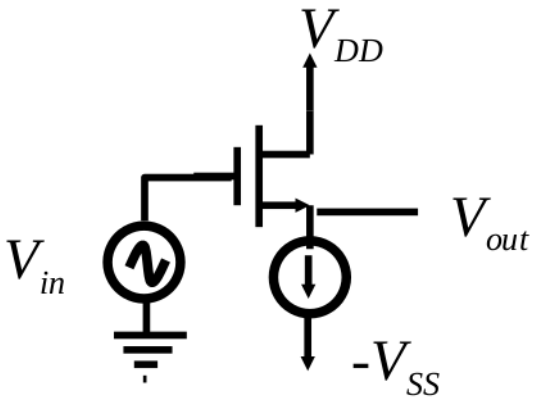
Common Source



Common Gate

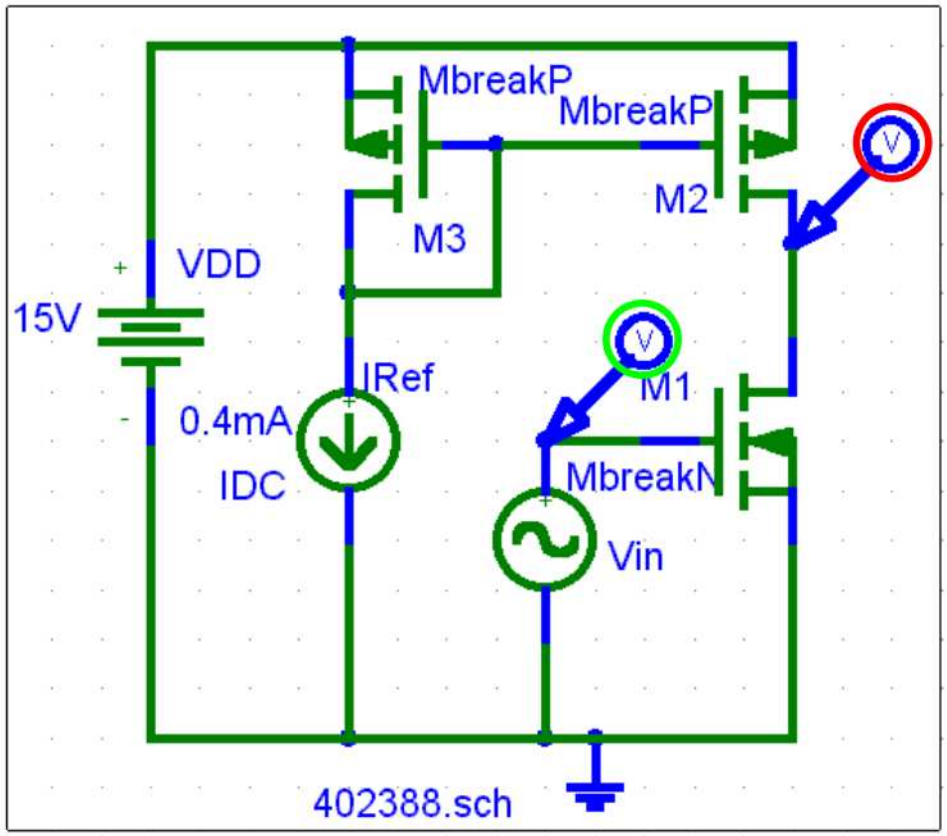


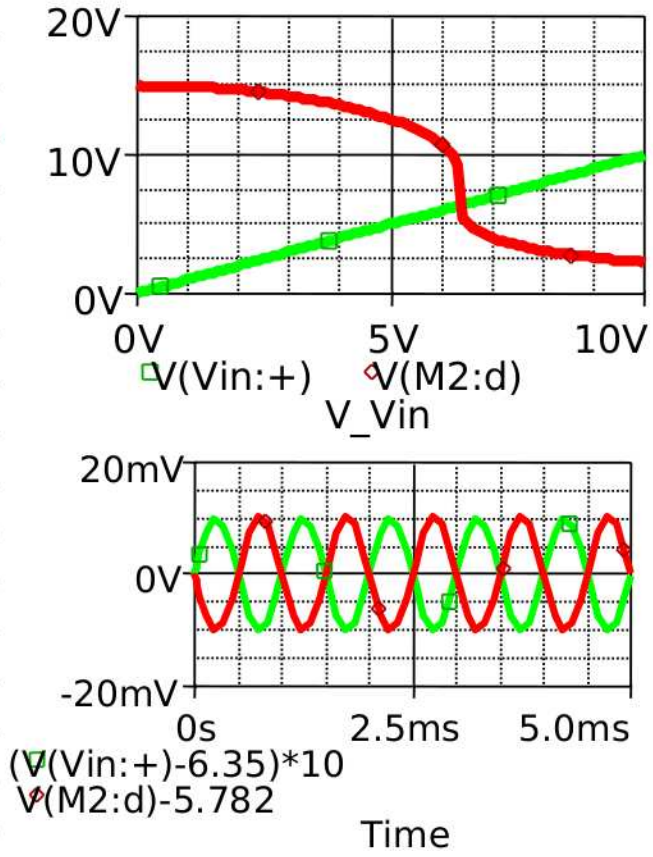
Common Drain



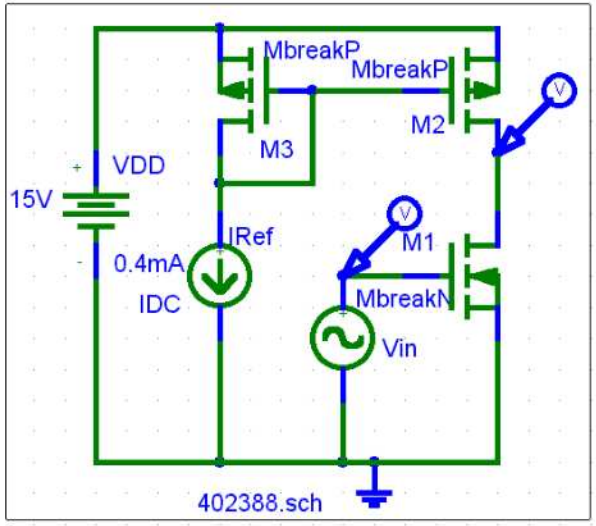
Note that "Current Source" Also serves as load

Common Source Amplifier



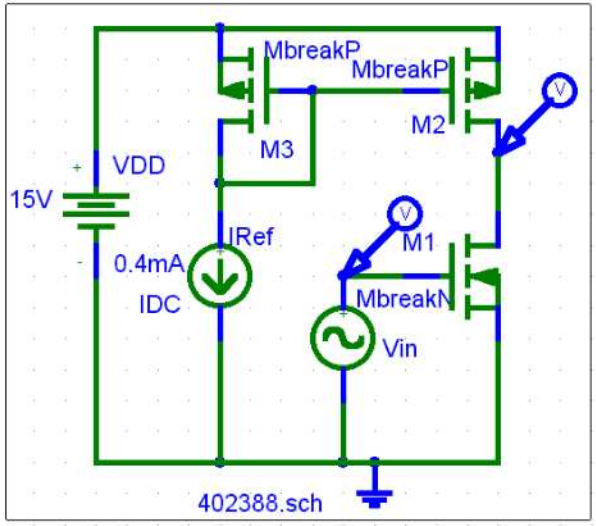


CS Amplifier Operation



- M1 is Amplifier
- M2 is Current Mirror
- Both Have Same V_{GS}
- Would Have Same Current if
  - Both in Saturation
  - No Early Effect
- Then no Amplification!

CS Circuit Analysis



Saturation

$$i_{D2} = k'_p \frac{W}{L} \frac{(V_{GS2} - V_{thr})^2}{2} \left(1 + \frac{V_{DS2}}{V_A}\right)$$

Triode

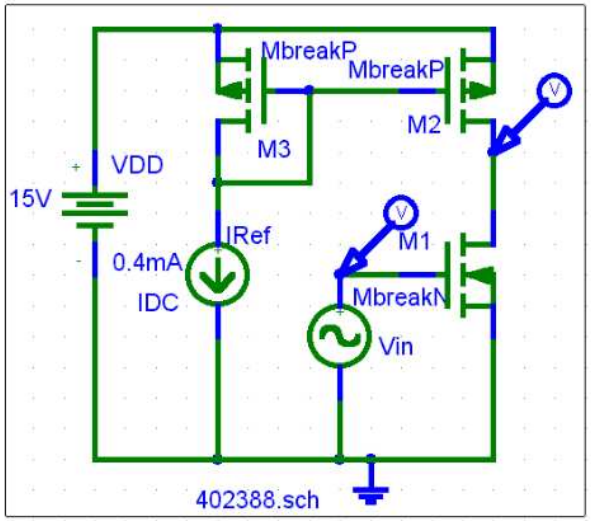
$$i_{D2} = k'_p \frac{W}{L} \left[(V_{GS} - V_{thr})V_{DS2} - \frac{1}{2}V_{DS2}^2\right]$$

Circuit

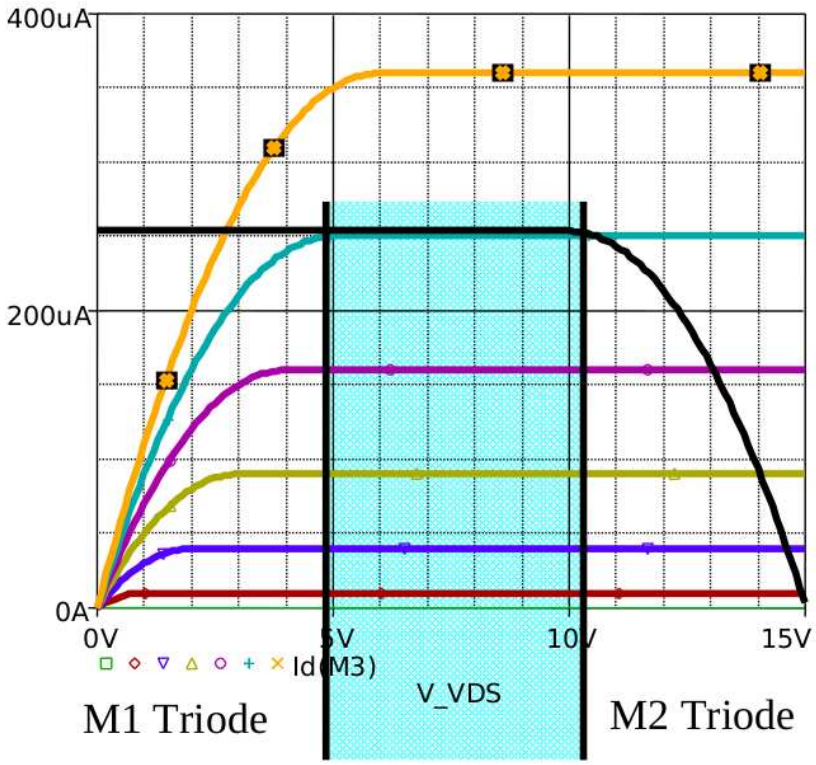
$$v_{DS1} + v_{SD2} = V_{DD}$$

$$v_{DS1} = V_{DD} + v_{DS2}$$

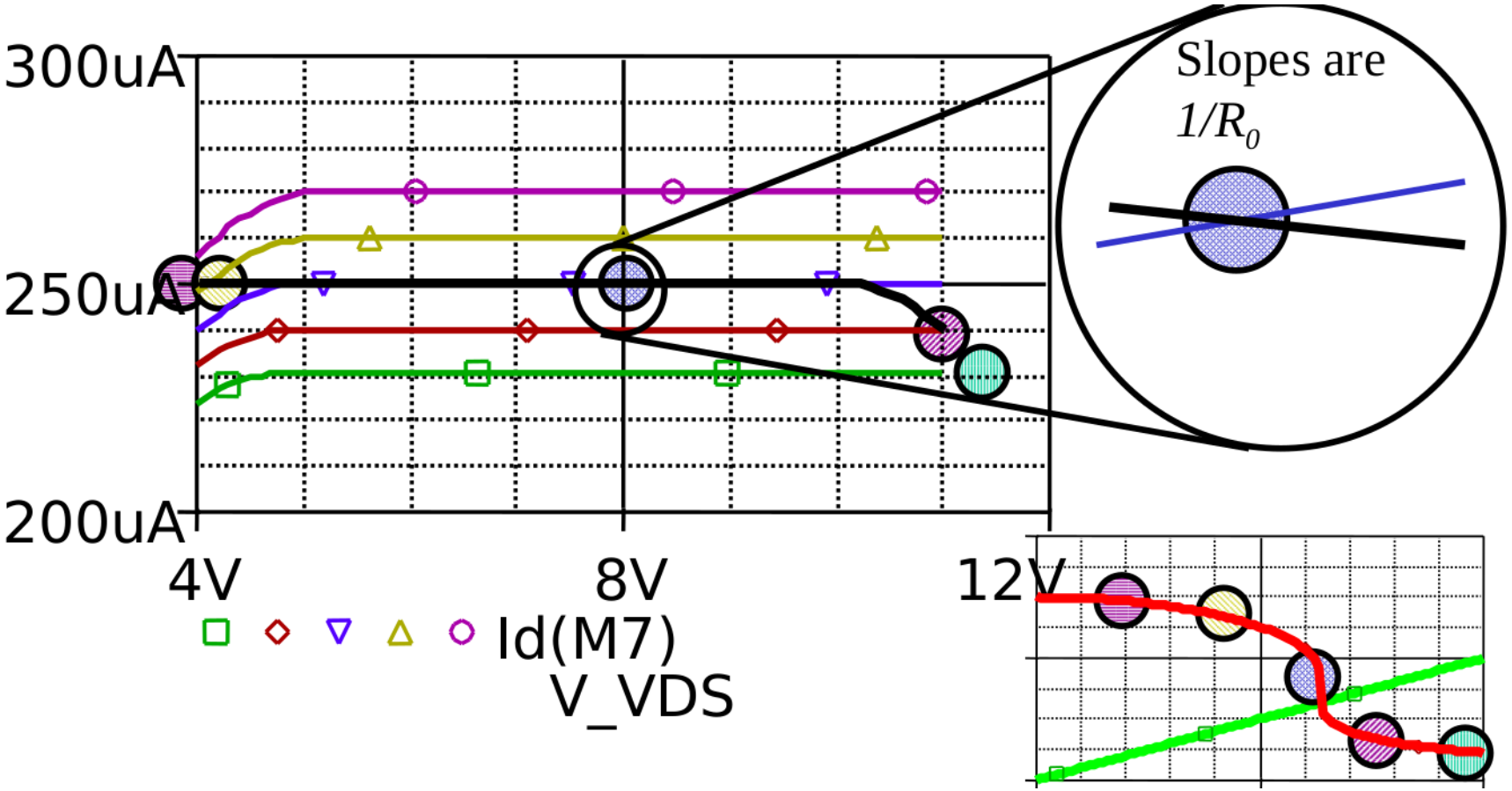
Graphical Analysis



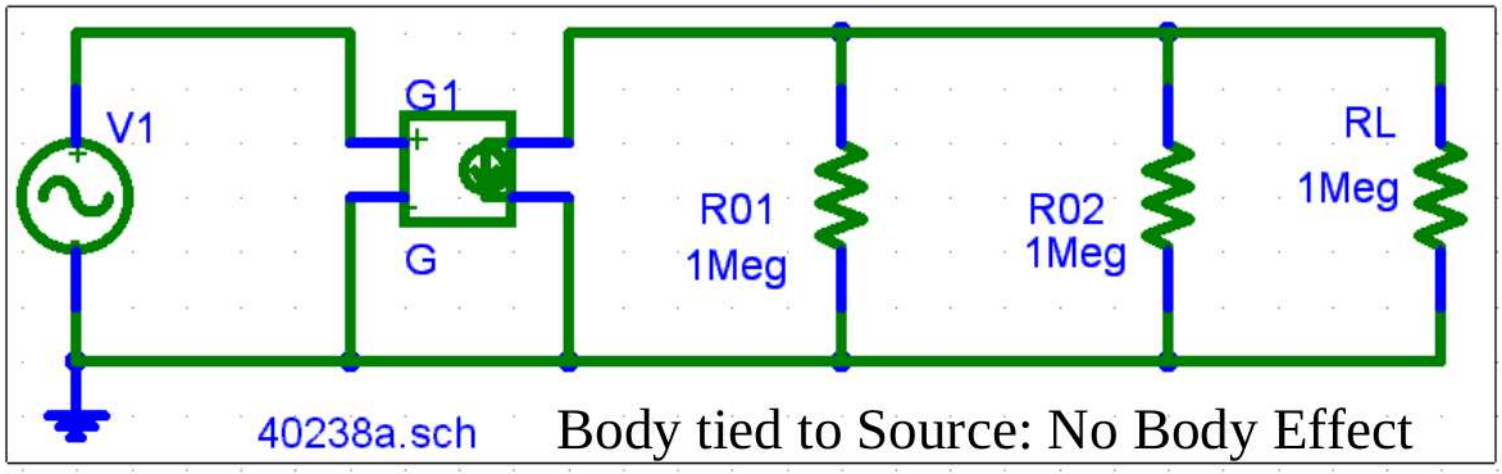
$$v_{DS1} = V_{DD} + v_{DS2}$$



Expanded Graphical Analysis



Small–Signal Model for CS Amp



$$I_D^{(DC)} = k'_n \frac{W}{L} \frac{\left(V_{GS}^{(DC)} - V_{thr}\right)^2}{2} = I_{REF} \qquad g_m = \frac{2I_D^{(DC)}}{\left(V_{GS}^{(DC)} - V_{thr}\right)}$$

Express in terms of Current $\qquad g_m = \sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}$

Small Signal Analysis

$$g_m = \sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}} \qquad R_0 = \frac{V_A}{I_D^{(DC)}}$$

$$A_V = - g_{m1} (R_{01} \| R_{02}) \qquad A_V = - \frac{\sqrt{2k'_n \frac{W_1}{L_1}}}{\frac{1}{V_{A1}} + \frac{1}{V_{A2}}} \frac{1}{\sqrt{I_{REF}^{(DC)}}}$$

$$R_{in} \rightarrow \infty \qquad R_{OUT} = R_{01} \| R_{02} = \frac{V_{A1}}{I_D^{(DC)}} \| \frac{V_{A2}}{I_D^{(DC)}}$$

(Nice!) (Unfortunate)

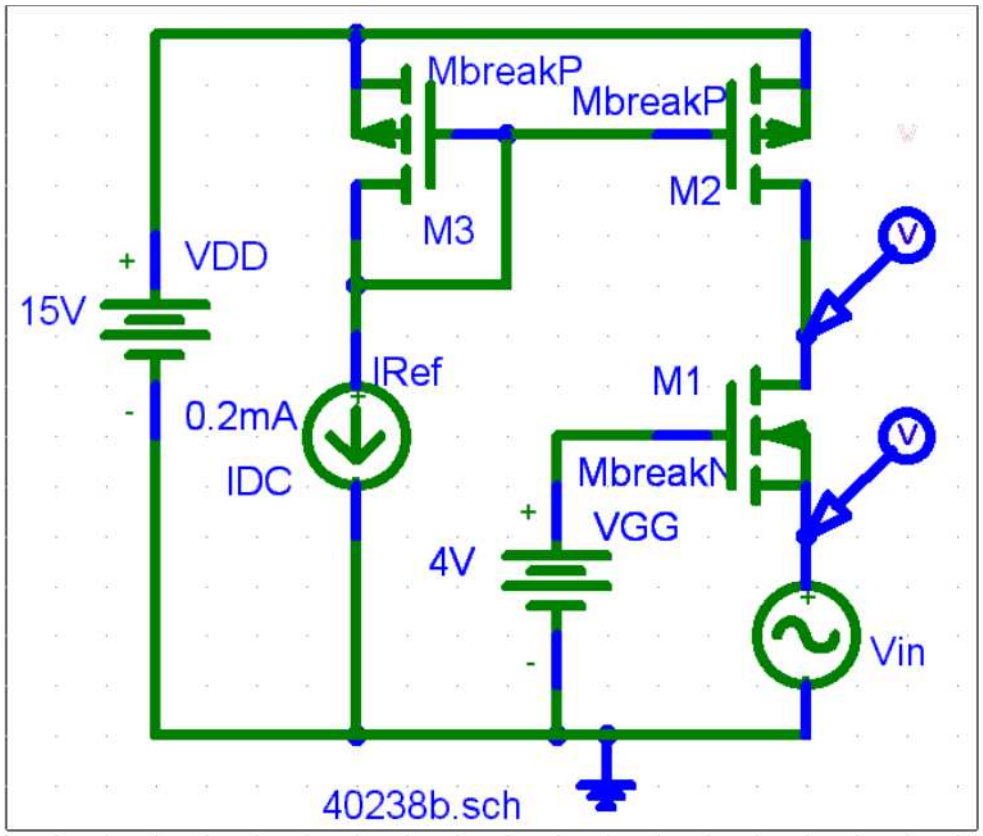
Some Numbers

$$A_V = - \frac{\sqrt{2k'_n \frac{W_1}{L_1}}}{\frac{1}{V_{A1}} + \frac{1}{V_{A2}}} \frac{1}{\sqrt{I_{REF}^{(DC)}}}$$

$$A_V = - \frac{\sqrt{2 \times 20 \times 10^{-6} \text{A/V}^2 \, 20}}{\frac{1}{100\text{V}} + \frac{1}{100\text{V}}} \frac{1}{\sqrt{4 \times 10^{-4} \text{A}}} = -70$$

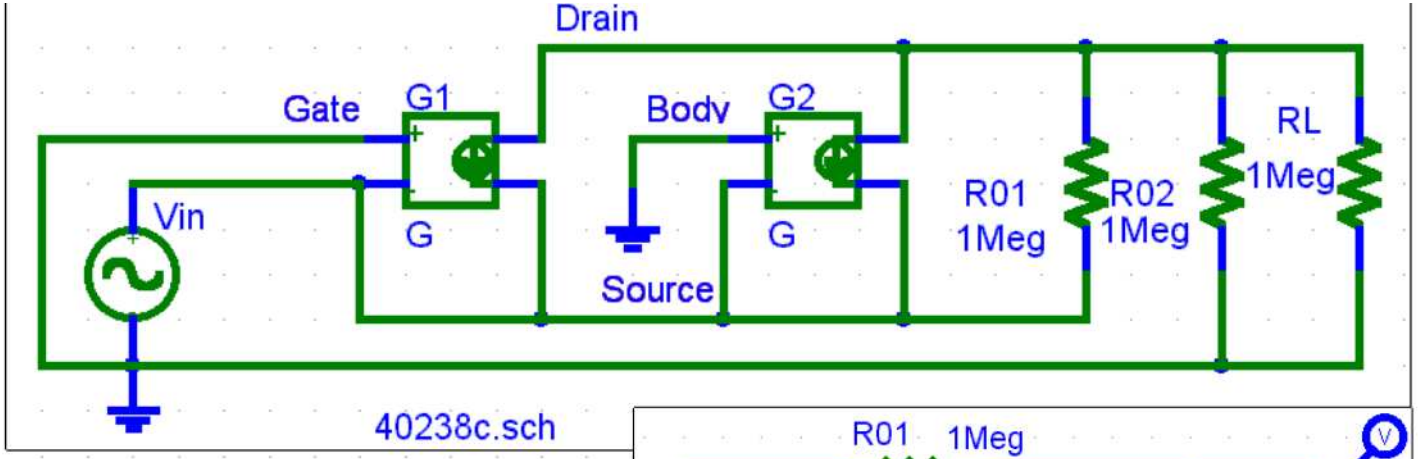
Typical Range is 20 to 100.

Common Gate Amplifier



- M1 is Amplifier
- M2 is Active Load and Current Mirror
- AC Models
  - M1
    - Small Signal Model with Body Effect
  - M2
    - R_{02}

CG Amp Small–Signal Model

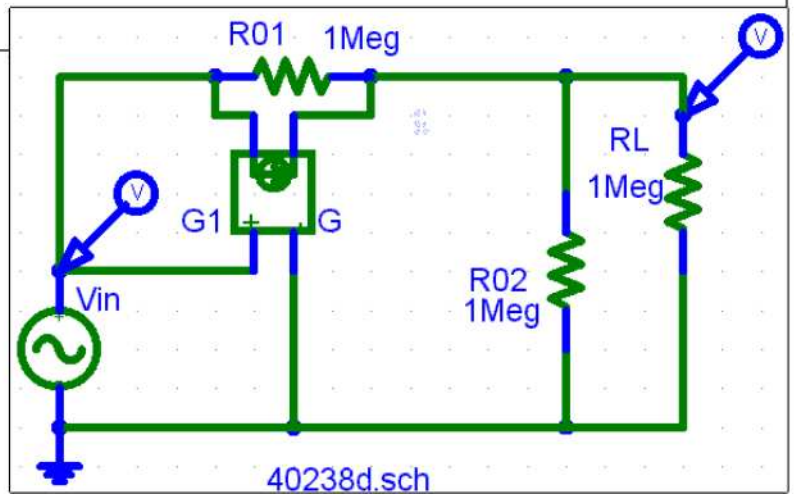


Above G1=g_{m1}

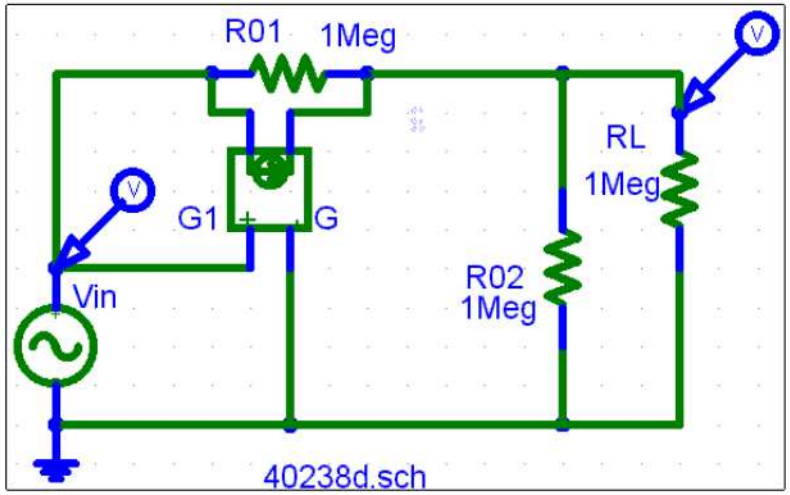
G2=χg_{m1}

Below

G1=$(1+\chi)g_{m1}$



CG Amp Voltage Gain



$$\frac{v_{in}^{(AC)} - v_{out}^{(AC)}}{R_{01}} + (1+\chi) g_{m1} v_{in}^{(AC)} = \frac{v_{out}^{(AC)}}{R_{02} \parallel R_L}$$

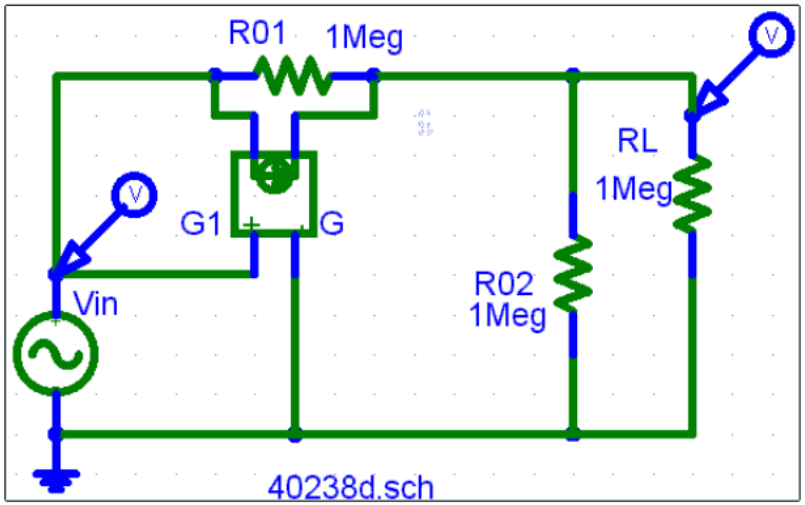
$$\left[\frac{1}{R_{01}} + (1+\chi) g_{m1} \right] v_{in}^{(AC)} = \frac{v_{out}^{(AC)}}{R_{01} \parallel R_{02} \parallel R_L}$$

$$v_{out}^{(AC)} = \left[\frac{1}{R_{01}} + (1+\chi) g_{m1} \right] (R_{01} \parallel R_{02} \parallel R_L) v_{in}^{(AC)}$$

$$A_V = \left[\frac{1}{R_{01}} + (1+\chi) g_{m1} \right] (R_{01} \parallel R_{02} \parallel R_L)$$

$$A_V = \left[\frac{1}{R_{01}} + (1+\chi) \sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}} \right] (R_{01} \parallel R_{02} \parallel R_L)$$

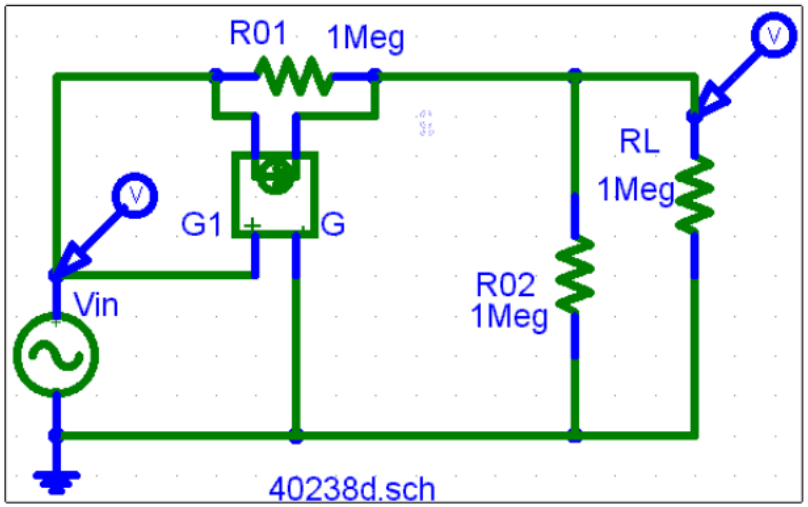
CG Amp Current Gain



Current from Input Splits Between two Resistors

$$A_i = 1 + \frac{R_L}{R_{02}} \approx 1$$

CG Amp Input Resistance



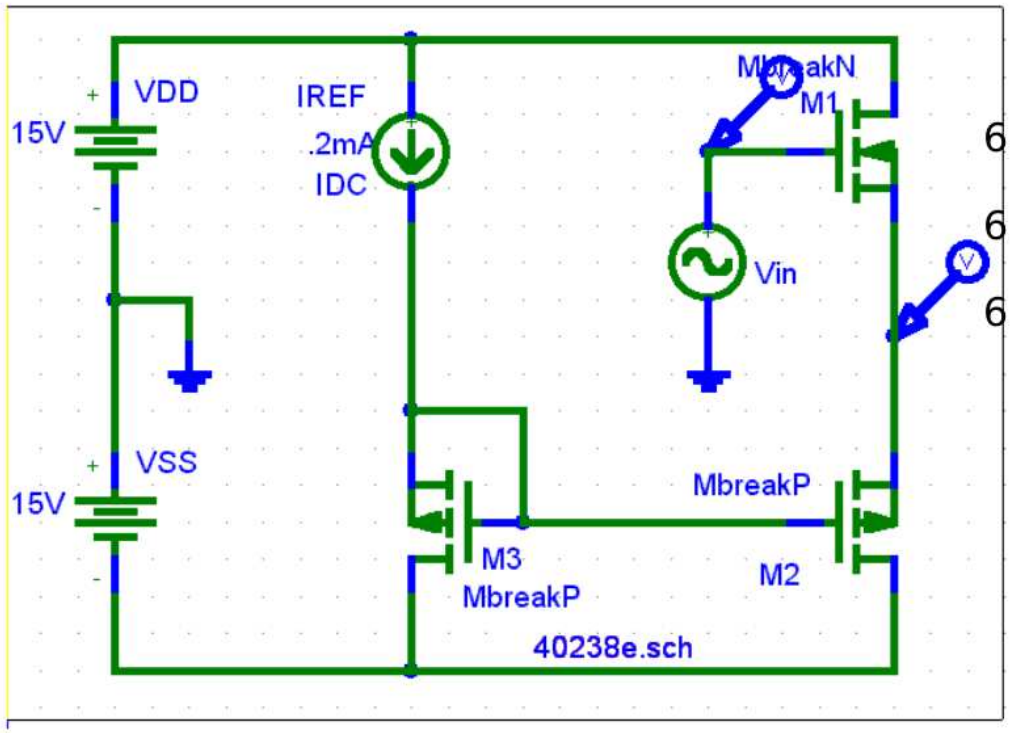
$$i_{in}^{(AC)} = \frac{v_{in}^{(AC)} - v_{out}^{(AC)}}{R_{01}} + (1+\chi) g_{m1} v_{in}^{(AC)} = \frac{v_{out}^{(AC)}}{R_{02} \parallel R_L}$$

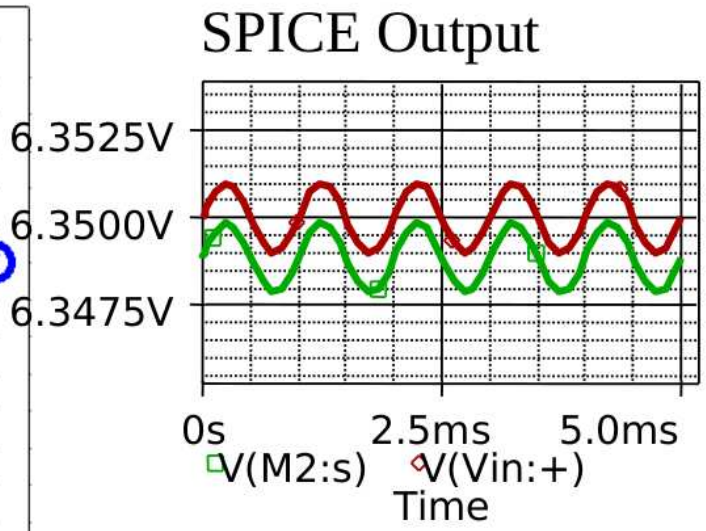
$$i_{in}^{(AC)} = \frac{\left[\frac{1}{R_{01}} + (1+\chi) g_{m1} \right] (R_{01} \parallel R_{02} \parallel R_L) v_{in}^{(AC)}}{R_{02} \parallel R_L}$$

$$\frac{v_{in}^{(AC)}}{i_{in}^{(AC)}} = \frac{R_{02} \parallel R_L}{\left[\frac{1}{R_{01}} + (1+\chi) g_{m1} \right] (R_{01} \parallel R_{02} \parallel R_L)}$$

$$R_{in} = \frac{v_{in}^{(AC)}}{i_{in}^{(AC)}} = \frac{1}{(1+\chi) g_{m1}} \left(1 + \frac{R_{02} \parallel R_L}{R_{01}} \right)$$

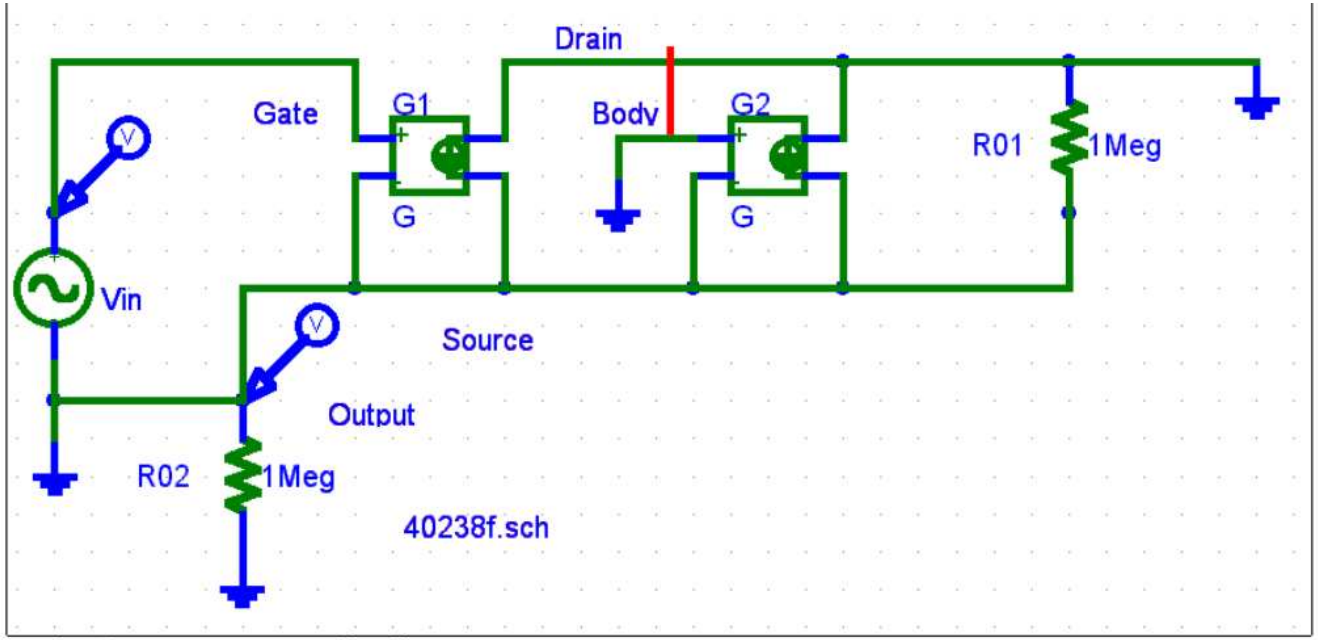
Common Drain Amplifier





M1 is Amplifier
M2 is Active Load and
Current Source

CD Amp Small–Signal Model



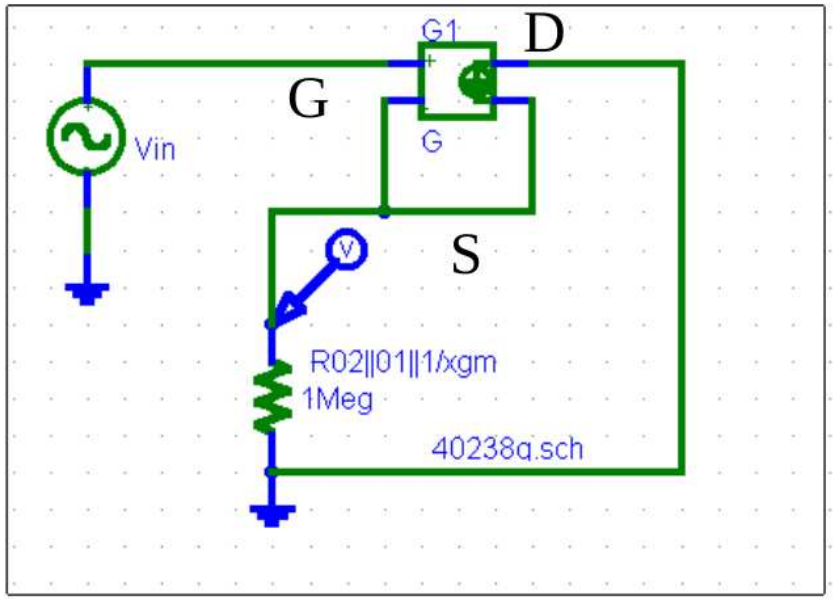
$$\chi g_{m1} V_{bs1}^{(AC)} = - \chi g_{m1} V_{s1}^{(AC)}$$

Current source acts like a resistor from source to ground (*ie*. source to drain)

Note also R01 is in parallel with R02.

Replace all 3 with a Single Resistor

Simplified CD Amp AC Model



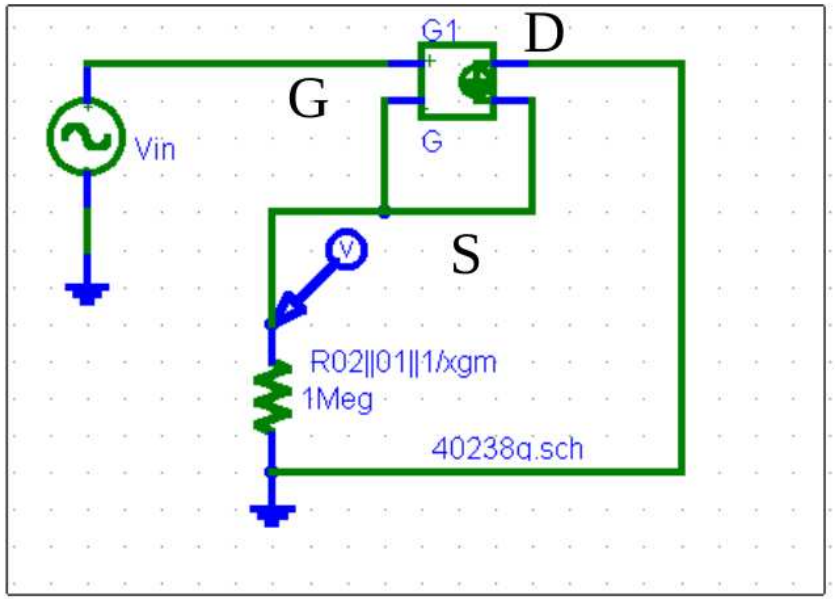
$$v_{out}^{(AC)} = \left(\frac{1}{\chi_1 g_{m1}} \| R_{01} \| R_{02} \right) g_{m1} v_{gs1}^{(AC)}$$

$$v_{in}^{(AC)} = v_{gs1}^{(AC)} + v_{s1}^{(AC)} =$$

$$v_{gs1}^{(AC)} + v_{out}^{(AC)}$$

$$v_{in}^{(AC)} = v_{gs1}^{(AC)} + \left(\frac{1}{\chi_1 g_{m1}} \| R_{01} \| R_{02} \right) g_{m1} v_{gs1}^{(AC)}$$

CD Amp Voltage Gain (1)



$$v_{out}^{(AC)} = \left(\frac{1}{\chi_1 g_{m1}} \| R_{01} \| R_{02} \right) g_{m1} v_{gs1}^{(AC)}$$

$$v_{in}^{(AC)} = v_{gs1}^{(AC)} + \left(\frac{1}{\chi_1 g_{m1}} \| R_{01} \| R_{02} \right) g_{m1} v_{gs1}^{(AC}$$

$$A_V = \frac{v_{out}^{(AC)}}{v_{in}^{(AC)}} = \frac{\left(\frac{1}{\chi_1 g_{m1}} \| R_{01} \| R_{02} \right) g_{m1}}{1 + \left(\frac{1}{\chi_1 g_{m1}} \| R_{01} \| R_{02} \right) g_{m1}}$$

CD Amp Voltage Gain (2)

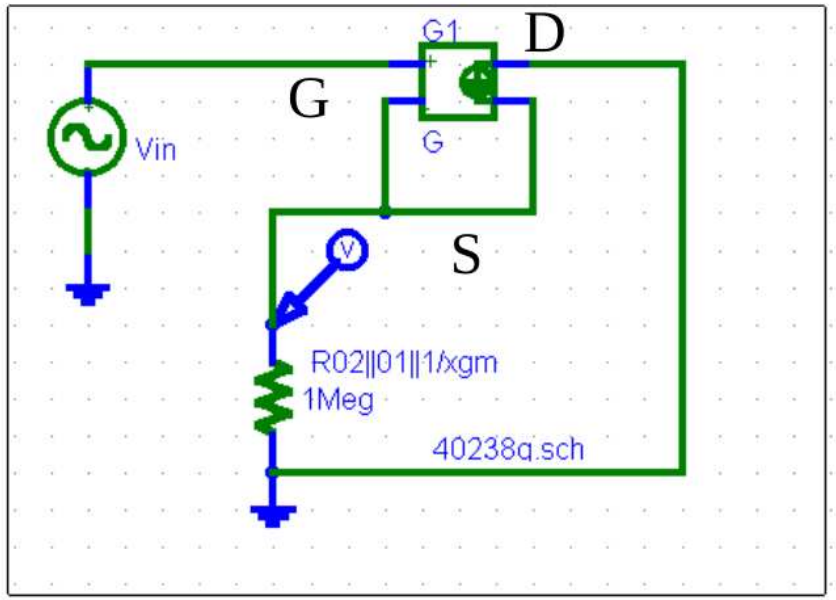
$$A_V = \frac{v_{out}^{(AC)}}{v_{in}^{(AC)}} = \frac{\left(\frac{1}{\chi_1 g_{m1}} \parallel R_{01} \parallel R_{02} \right) g_{m1}}{1 + \left(\frac{1}{\chi_1 g_{m1}} \parallel R_{01} \parallel R_{02} \right) g_{m1}} = \frac{g_{m1}}{\frac{1}{\left(\frac{1}{\chi_1 g_{m1}} \parallel R_{01} \parallel R_{02} \right)} + g_{m1}}$$

$$A_V = \frac{g_{m1}}{g_{m1} + \chi_1 g_{m1} + \frac{1}{R_{01}} + \frac{1}{R_{02}}} \approx \frac{1}{1 + \chi}$$

Voltage Buffer

CD Amp Output Resistance

$$R_{out} = \frac{1}{g_{m1} + \chi_1 g_{m1} + \frac{1}{R_{01}} + \frac{1}{R_{02}}} \approx \frac{1}{g_{m1}(1+\chi)}$$



(Current Source and all Resistor Appear in Parallel)

$$R_{out} \approx \frac{1}{\sqrt{k'_n \frac{W}{L} I_{D1}^{(DC)}}(1+\chi)}$$

FET Amplifier Summary

	Voltage Gain	Current Gain	Input Resistance	Output Resistance
CS	$-\sqrt{2k'_n \frac{W_1}{L_1}} \frac{V_A}{\sqrt{I_{REF}^{(DC)}}}$		Infinite	$\frac{V_{A1}}{I_D^{(DC)}} \parallel \frac{V_{A2}}{I_D^{(DC)}}$
CG	$\left[\frac{1}{R_{01}} + (1+\chi)\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}\right](R_{01} \parallel R_{02} \parallel R_L)$	$1 + \frac{R_L}{R_{02}} \approx 1$	$\frac{1}{(1+\chi)\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}}\left(1 + \frac{R_{02} \parallel R_L}{R_{01}}\right)$	$\frac{V_{A1}}{I_D^{(DC)}} \parallel \frac{V_{A2}}{I_D^{(DC)}}$
CD	$\frac{\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}}{\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}(1+\chi_1) + \frac{1}{R_{01}} + \frac{1}{R_{02}}} \approx 1$		Infinite	$\approx \frac{1}{\sqrt{k'_n \frac{W}{L} I_{D1}^{(DC)}(1+\chi)}}$