Fundamentals of Electronics
Week 12

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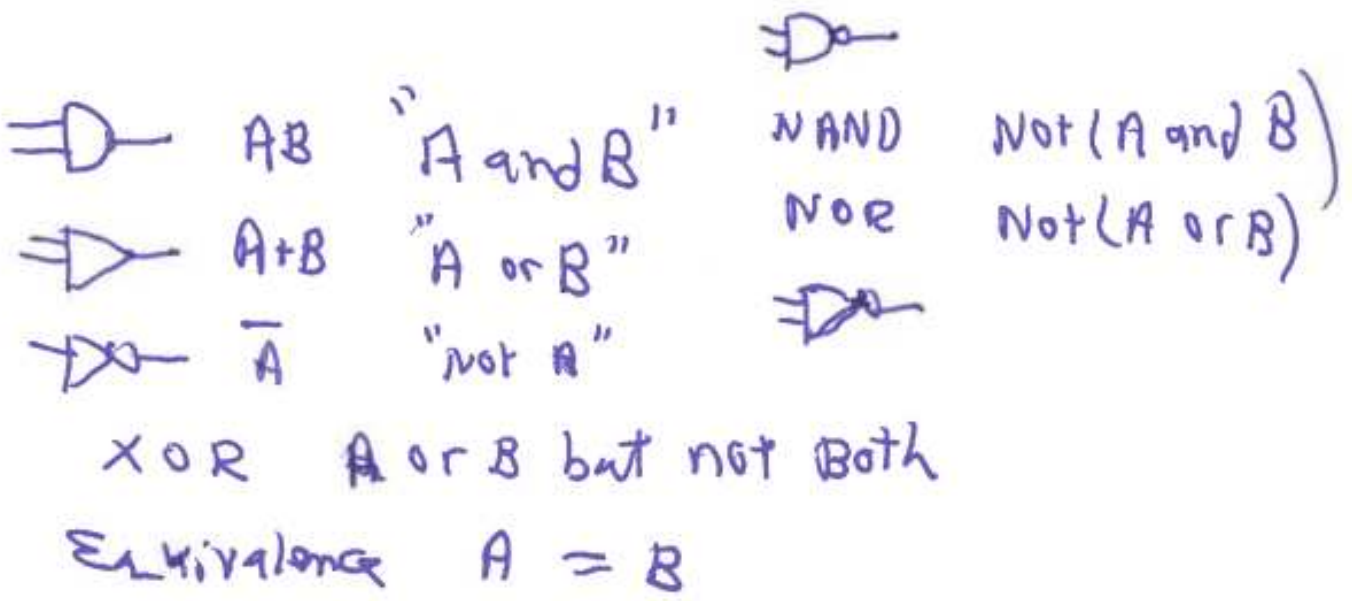
Agenda

- Overview
- Logic Inverter
  - Graphical Analysis
  - Calculations
  - Sample Circuits
  - CMOS Advantages
- NOR Gate
- NAND Gate

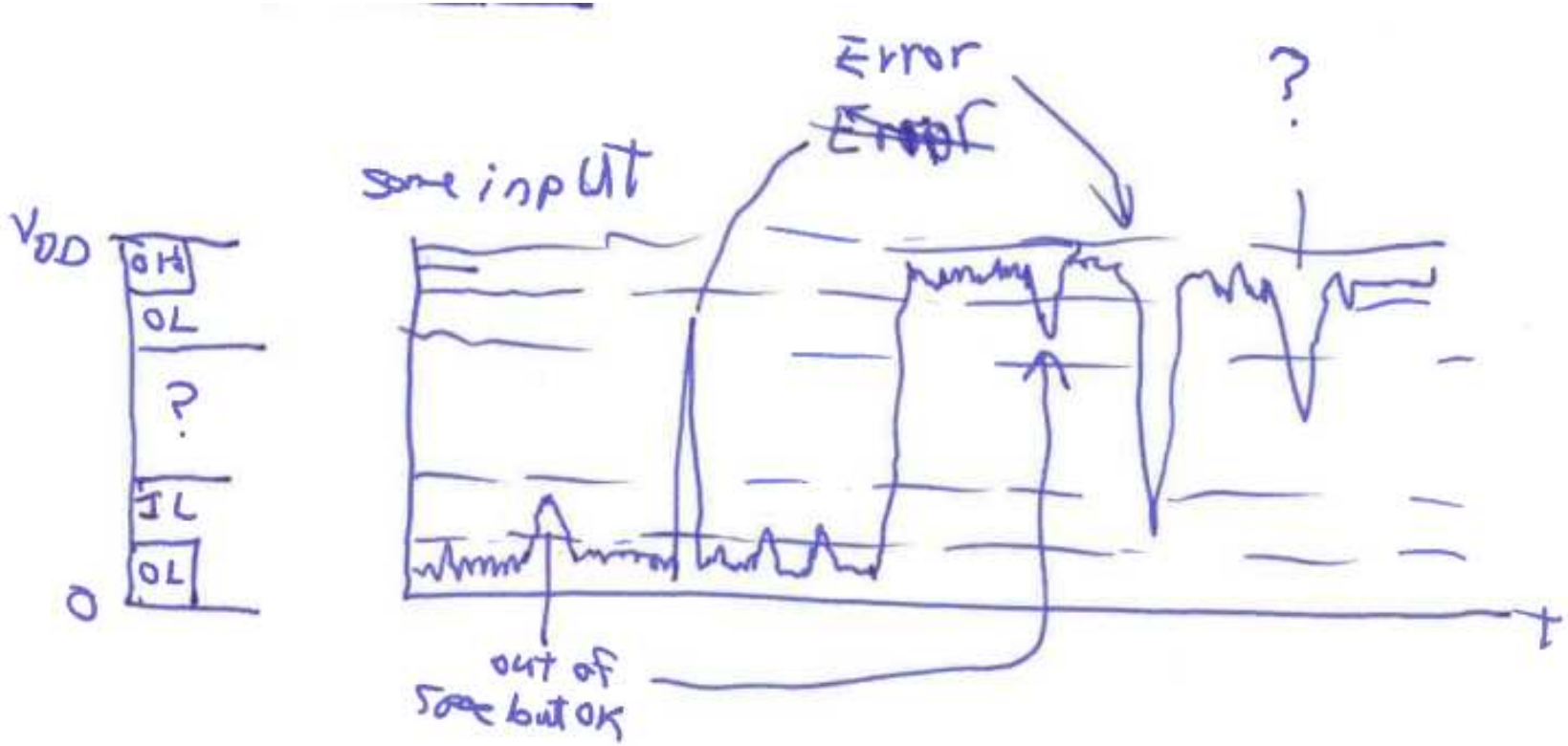
Logic Goals

- Complete: Implement all logic functions
- Simple: As few different devices as possible
- Fanout
- Noise Tolerance
- Low Power Consumption
- Small Size
- High Speed

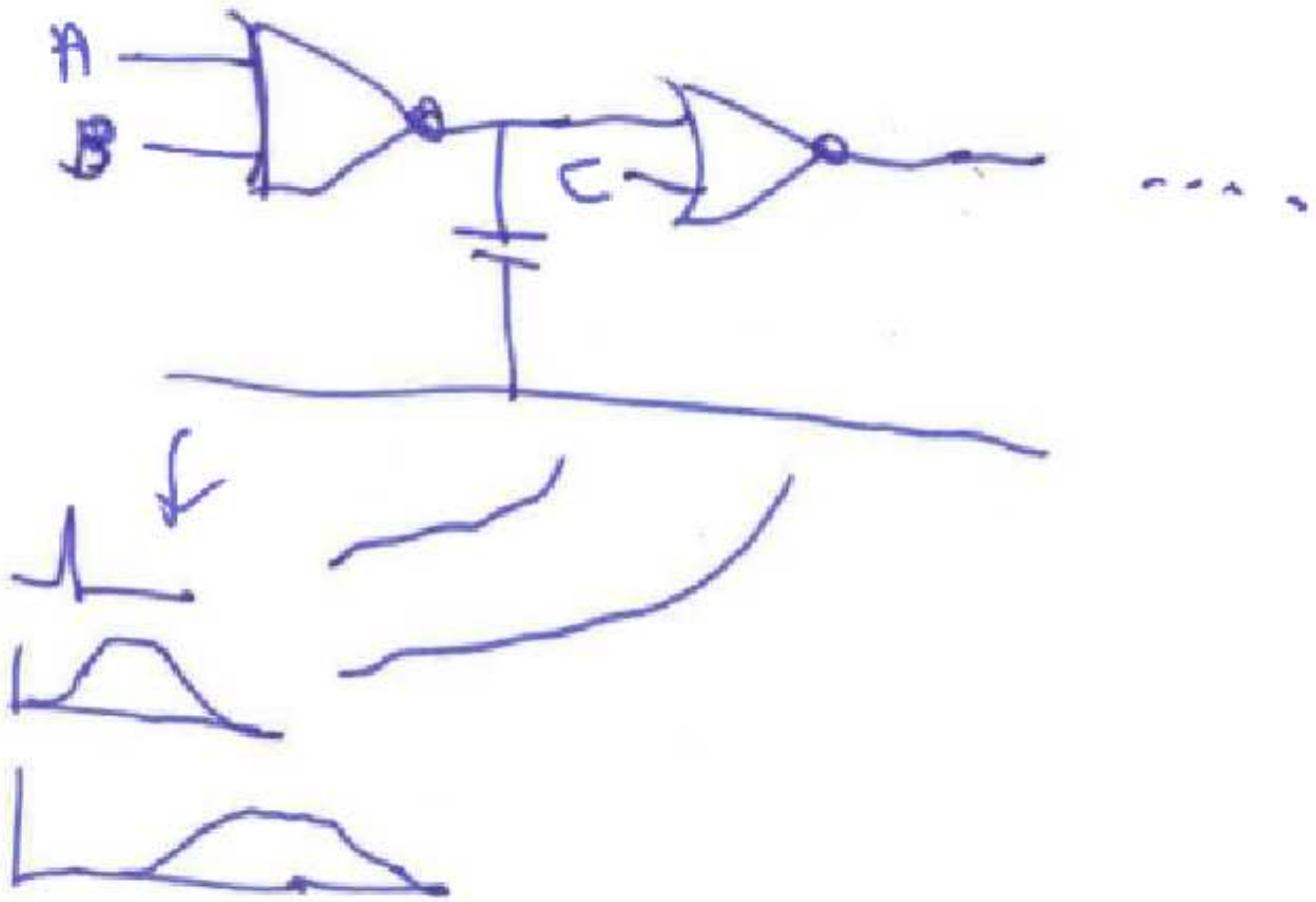
Logic Functions



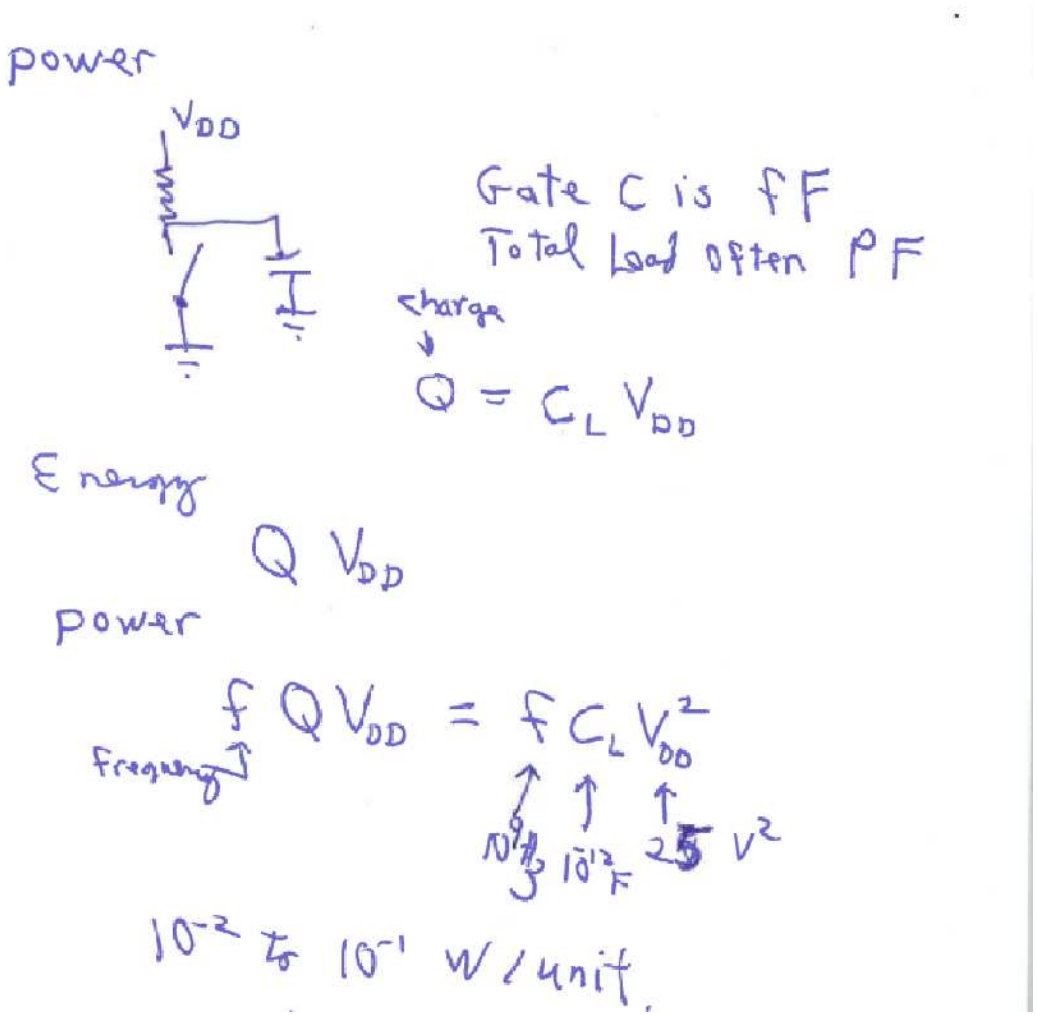
Noise in Logic



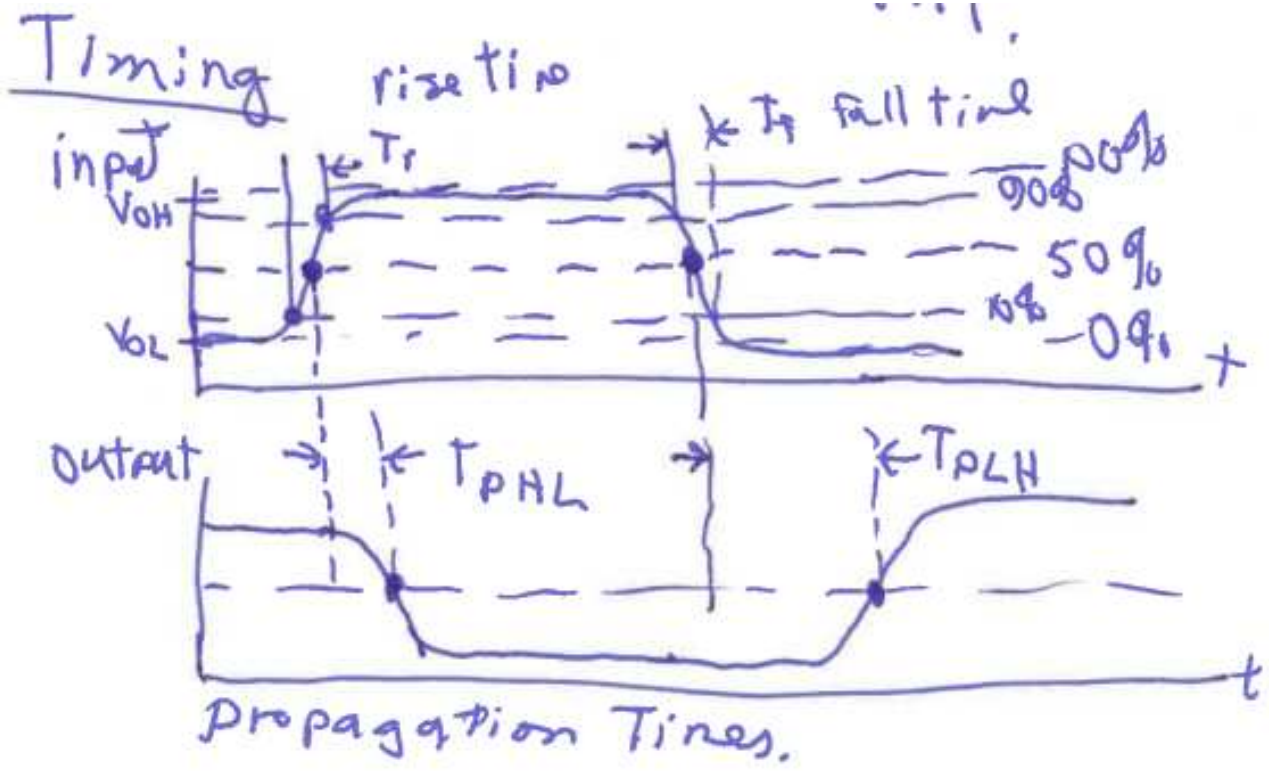
Speed in Logic



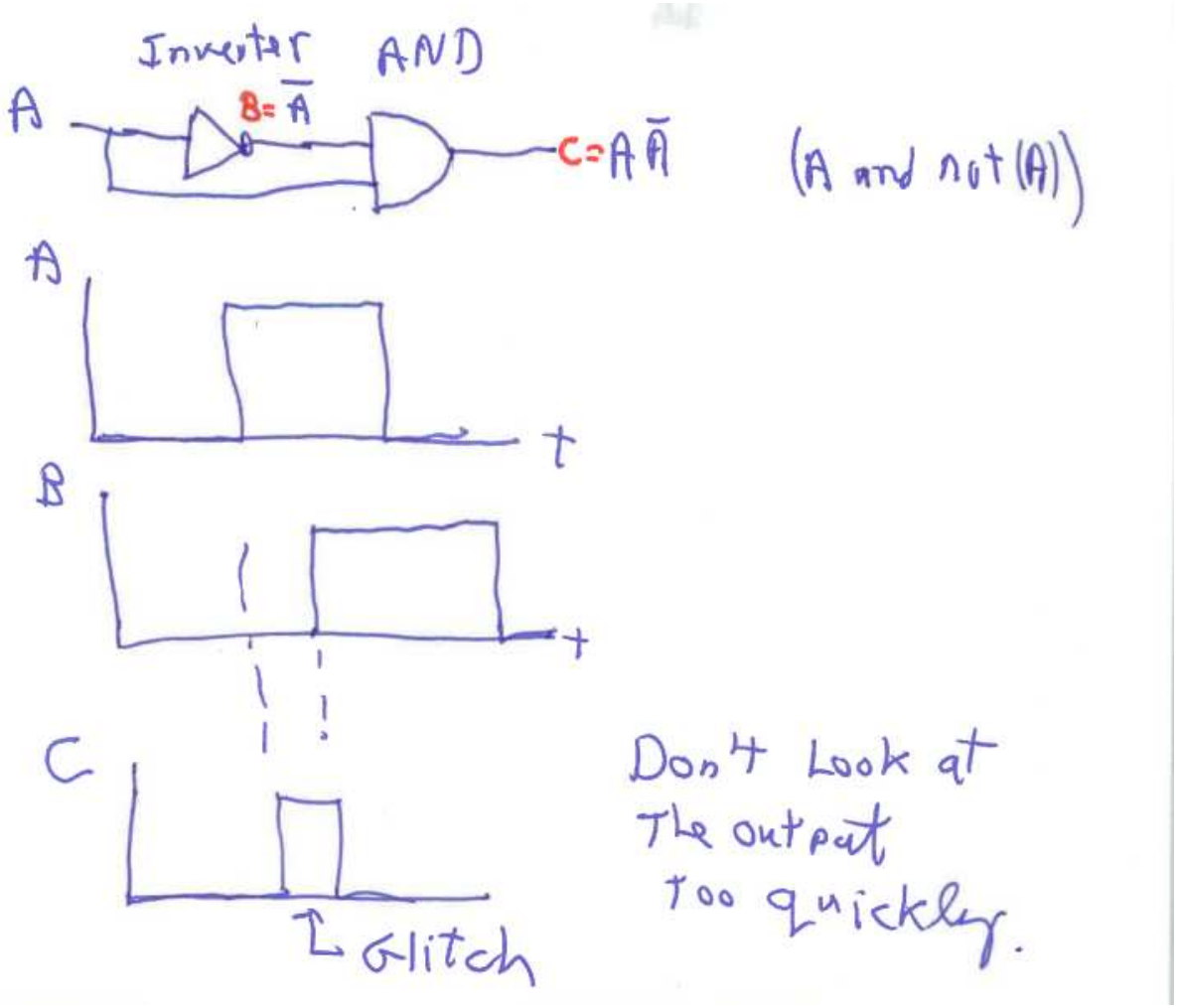
Power in Logic



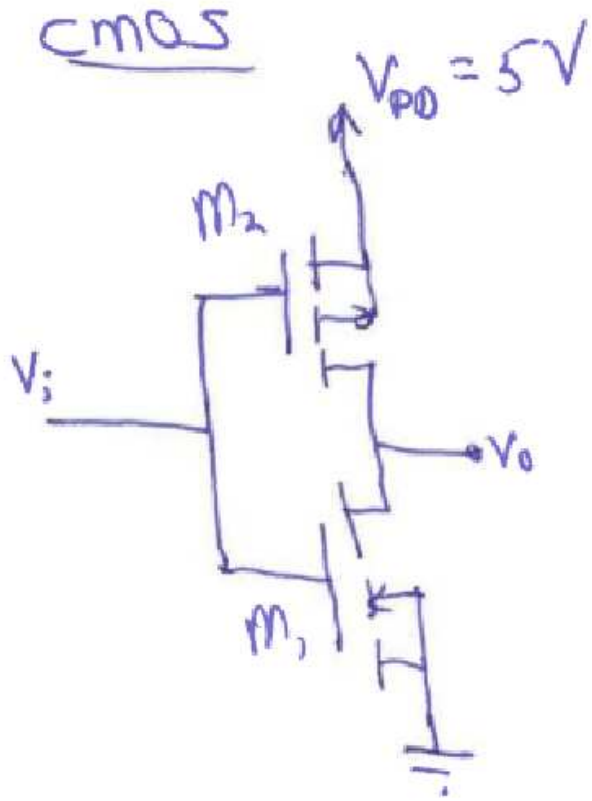
Timing in Logic



Glitch


Inverter
AND
A
B = Ā
C = A Ā
(A and not (A))
A
t
B
t
C
Glitch
Don't Look at
The output
too quickly.

CMOS Logic Inverter



input	0	5
V_{GS1}	0	5
V_{SG2}	5	0
V_o	5	0

cutoff

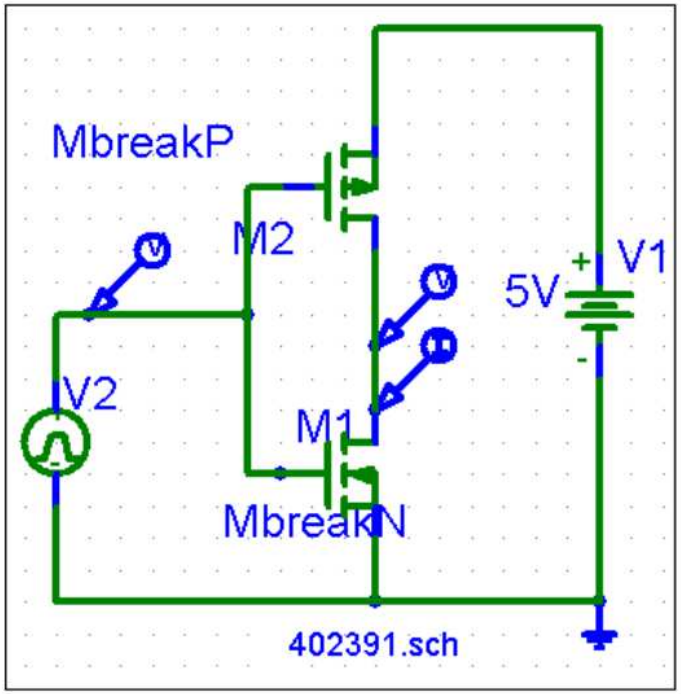
little detail

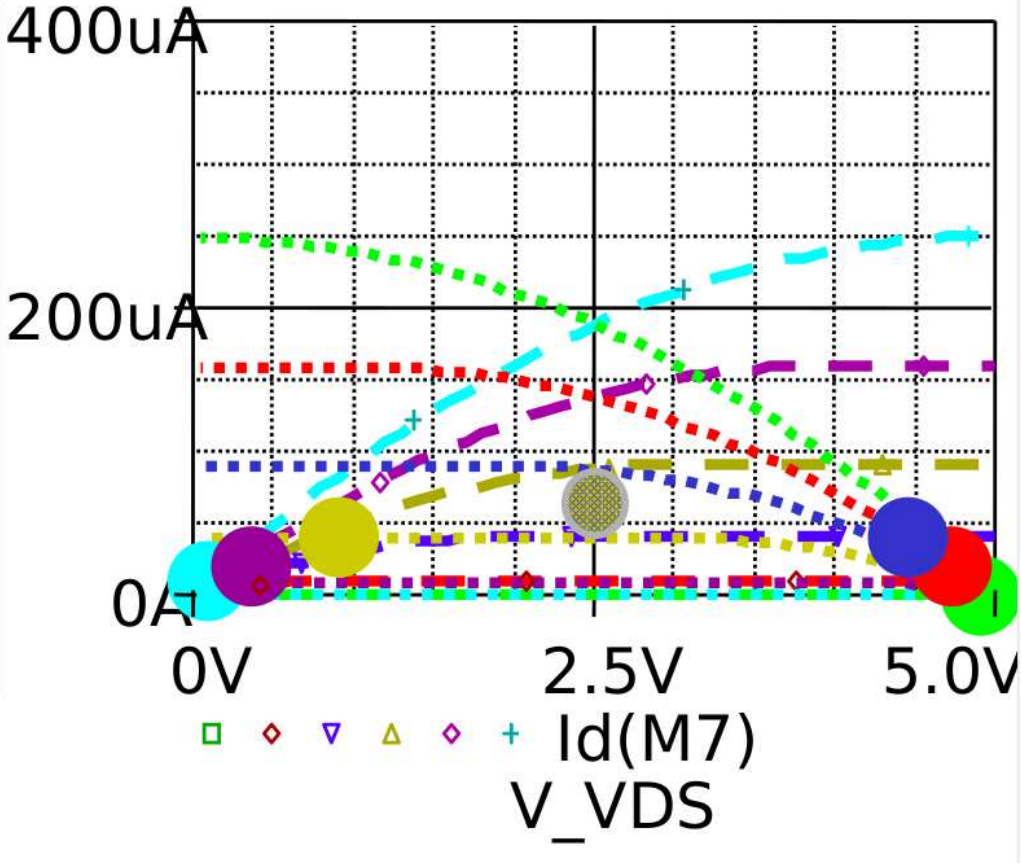
$$K_{P(P)} = \frac{K_{P(n)}}{2}$$

$$\left(\frac{W}{L}\right)_P = 2\left(\frac{W}{L}\right)_n$$

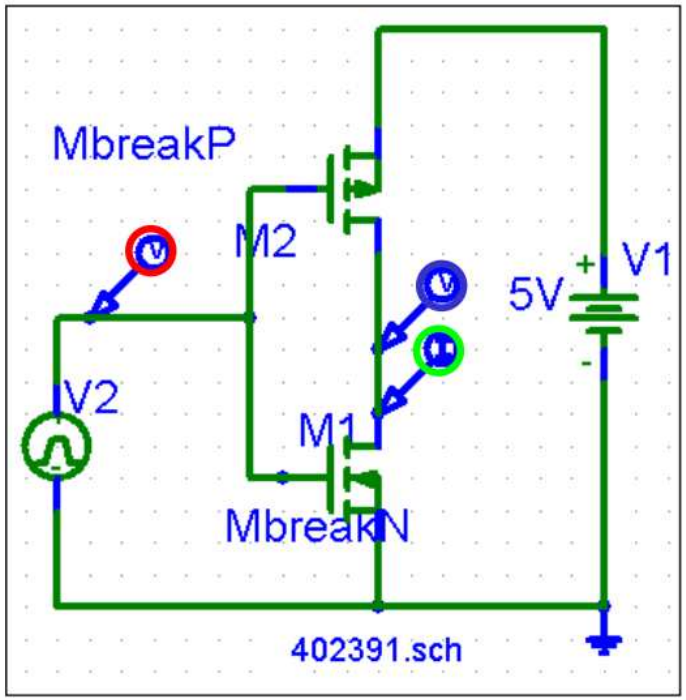
$$K_{(P)} = K_{(n)}$$

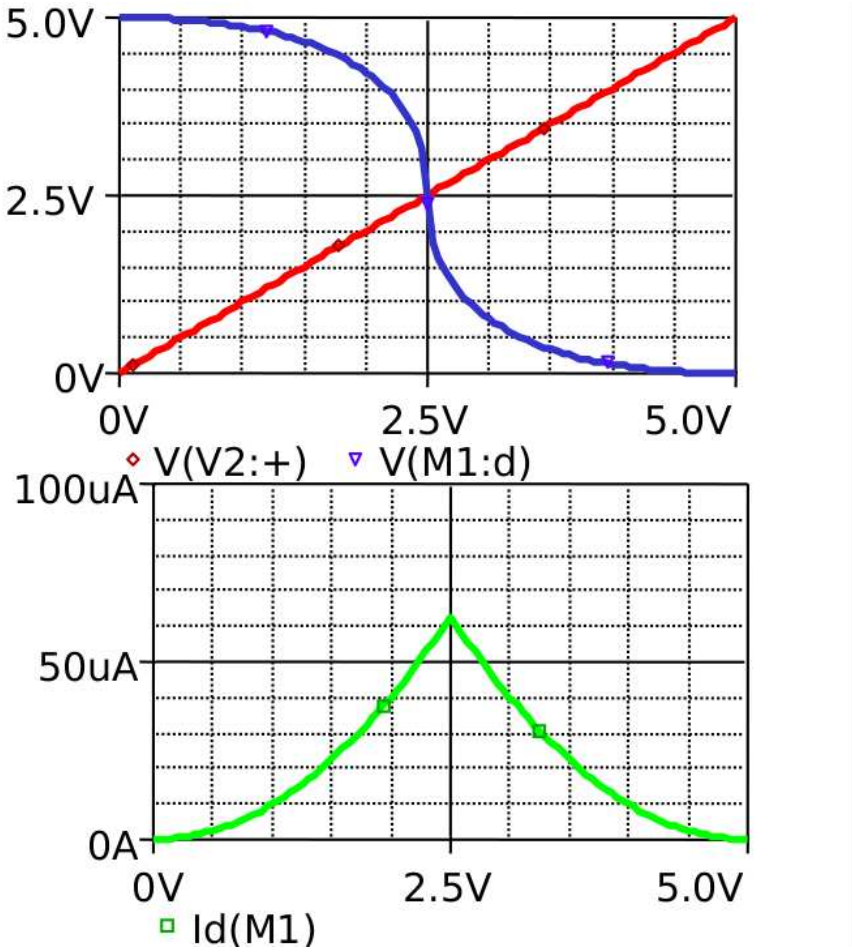
Inverter Operation



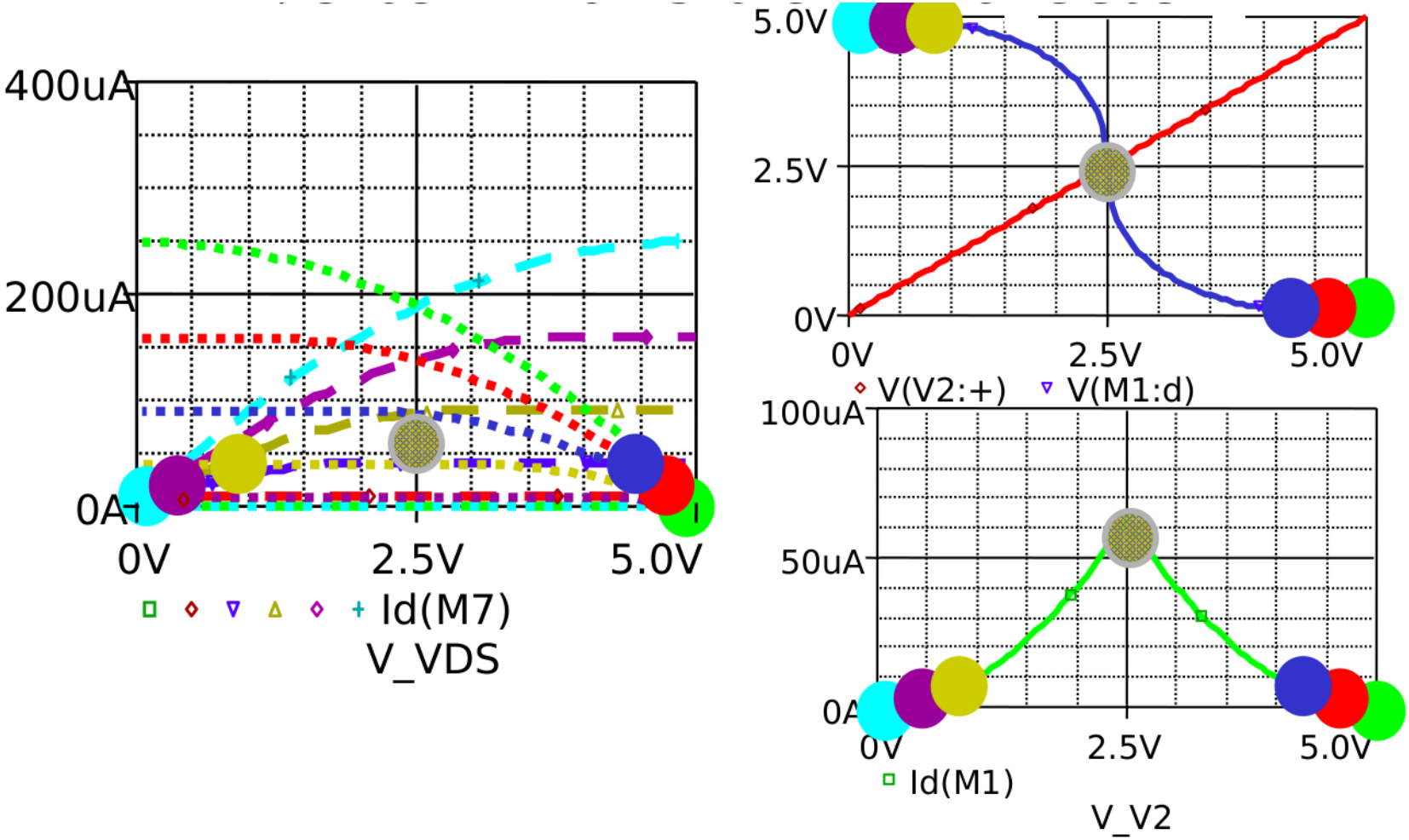


CMOS Inverter Behavior





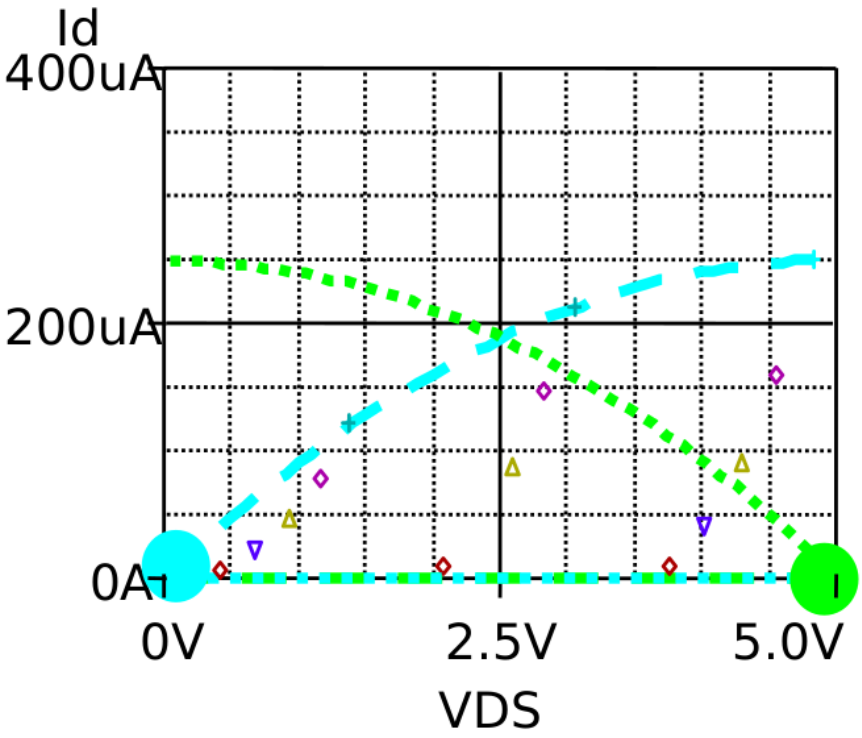
Inverter Transition Trajectory



FET Logic Characteristics

- Wide Voltage Swing (0 to 5 V)
  - Good noise margins
- Near Zero Power Consumption (static)
- Low Output Resistance
  - Can Drive Large Loads
  - Low Noise
- High Input Resistance

Output Resistance



- Transistor with High v_{GS} $(=v_{DD})$is in Triode
  - Steep IV Slope=Low R

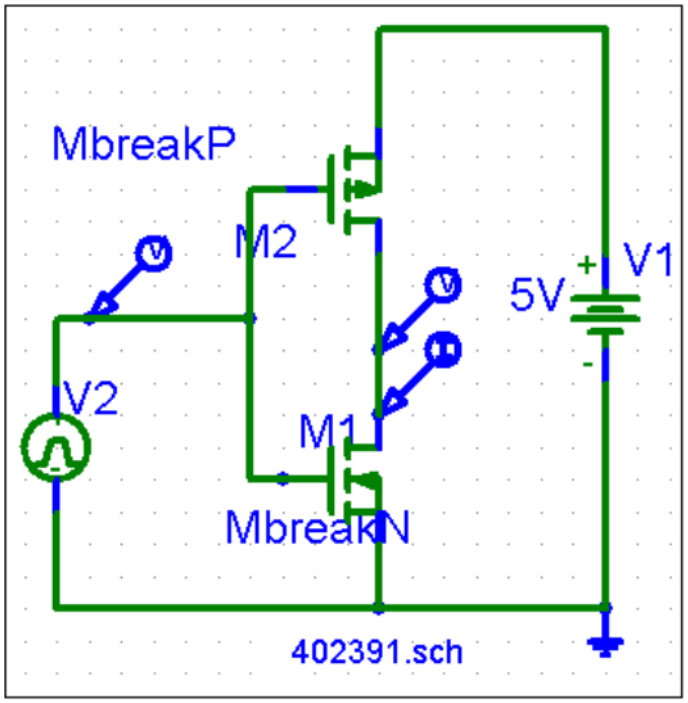
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_{thr})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$$\frac{di_D}{dv_{DS}} = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - V_{thr}) - v_{DS}\right]$$

$$\frac{di_D}{dv_{DS}} \approx \mu_n C_{ox} \frac{W}{L}\left[(v_{DD} - V_{thr}) - 0\right]$$

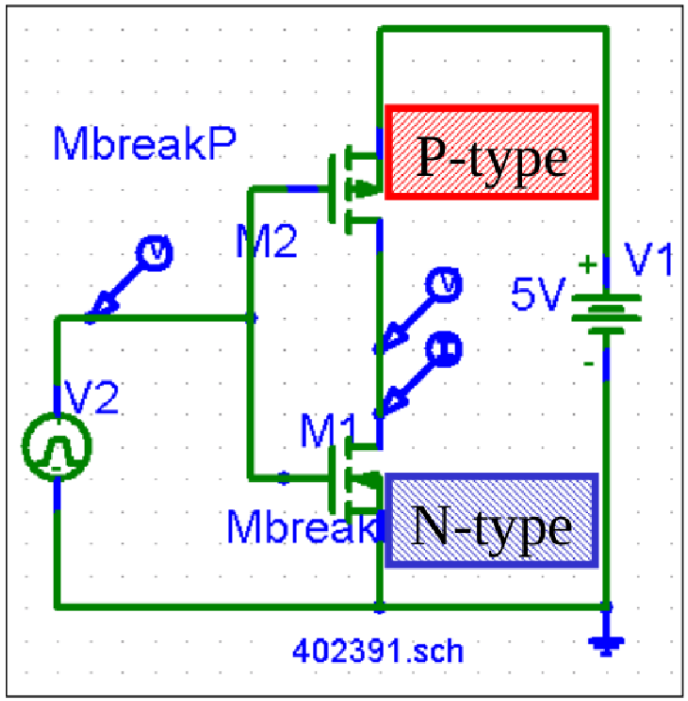
$$R_{DS} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(v_{DD} - V_{thr})} \approx \frac{1}{20\times10^{-6}(\mathrm{A/V^2})\times50\times5\mathrm{V}} = 200\Omega$$

Input Resistance



- Input to Gates Only
  - Infinite Resistance

FET Logic Equations (1)



Triode $v_{out} < v_{in} - V_{thr}$

$$i_{DP} = \mu_p C_{ox} \frac{W}{L}\left[(V_{DD} - v_{in} - |v_{thr}|)(V_{DD} - v_{out}) - \frac{1}{2}(V_{DD} - v_{out})^2\right]$$

Saturation

$$i_{DP} = \mu_p C_{ox} \frac{W}{L} \frac{(V_{DD} - v_{in} - |V_{thr}|)^2}{2}\left(1 + \frac{V_{DD} - v_{out}}{V_A}\right)$$

Triode $v_{out} > v_{in} + |V_{thr}|$

$$i_{DN} = \mu_n C_{ox} \frac{W}{L}\left[(v_{in} - v_{thr})v_{out} - \frac{1}{2}v_{out}^2\right]$$

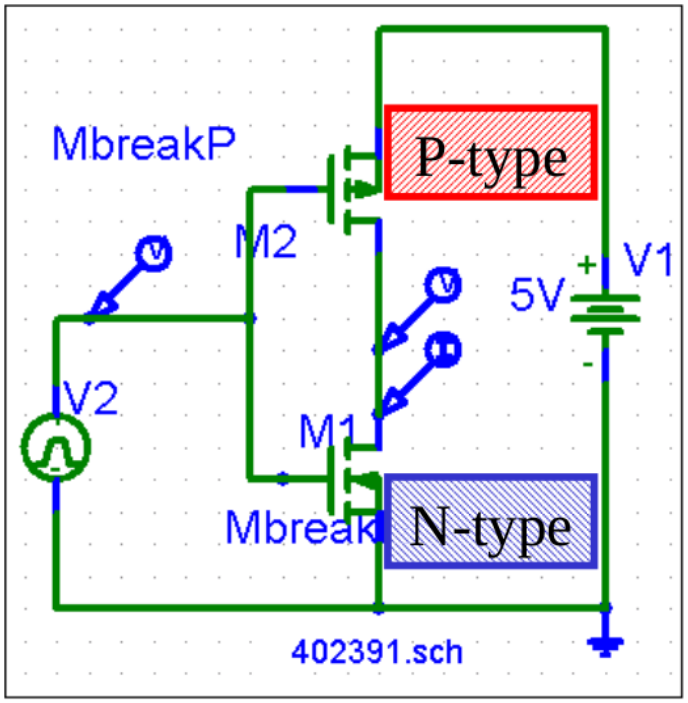
Saturation

$$i_{DN} = \mu_n C_{ox} \frac{W}{L} \frac{(v_{in} - V_{thr})^2}{2}\left(1 + \frac{v_{out}}{V_A}\right)$$

Assume

$\mu_p W_p/L_p = \mu_n W_n/L_n$

FET Logic Equations (2)



Both in Saturation

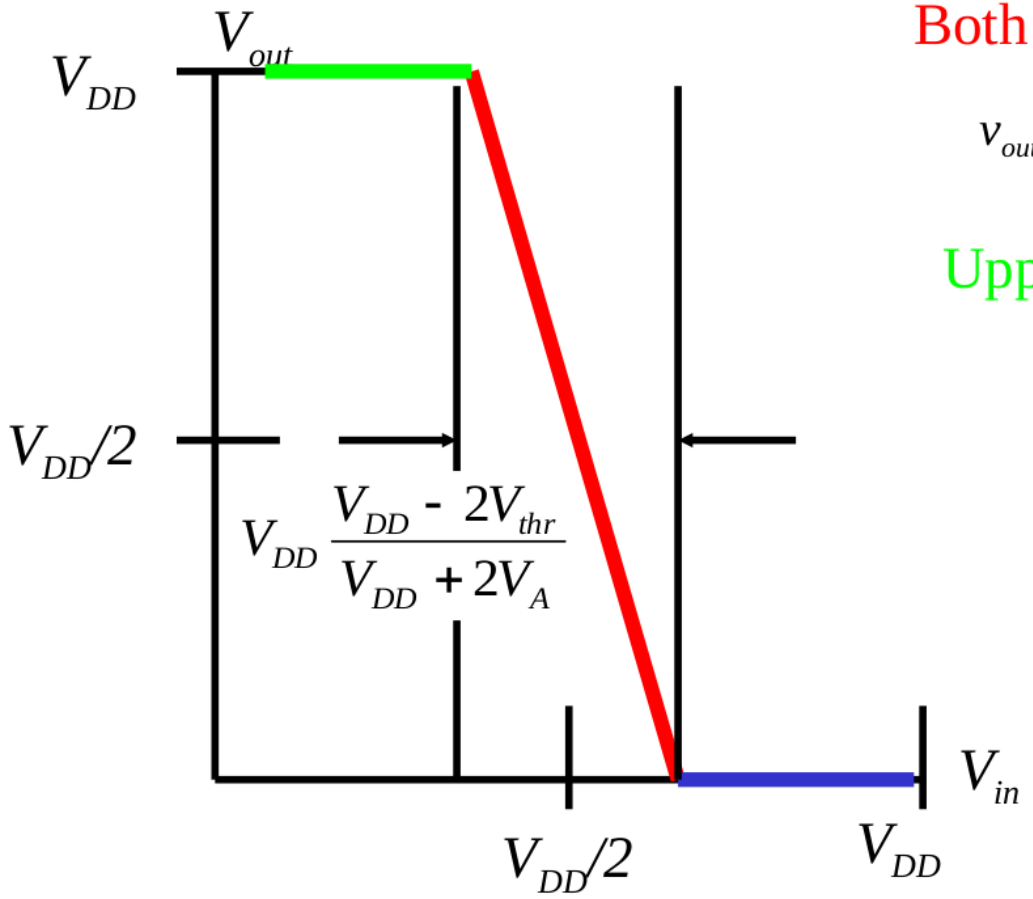
$$i_D = \mu C_{ox} \frac{W}{L} \frac{(V_{DD} - v_{in} - |V_{thr}|)^2}{2} \left(1 + \frac{V_{DD} - v_{out}}{V_A}\right)$$

$$i_D = \mu C_{ox} \frac{W}{L} \frac{(v_{in} - V_{thr})^2}{2} \left(1 + \frac{v_{out}}{V_A}\right)$$

$$\frac{(V_{DD} - v_{in} - |V_{thr}|)^2}{2} \left(1 + \frac{V_{DD} - v_{out}}{V_A}\right) = \frac{(v_{in} - V_{thr})^2}{2} \left(1 + \frac{v_{out}}{V_A}\right)$$

Trust Me $$v_{out} = \frac{V_{DD}}{2} - \frac{V_{DD} + 2V_A}{V_{DD} - 2V_{thr}} \left(v_{in} - \frac{V_{DD}}{2}\right)$$

FET Logic Equations (3)



Both in Saturation

$$v_{out} = \frac{V_{DD}}{2} - \frac{V_{DD} + 2V_A}{V_{DD} - 2V_{thr}} \left(v_{in} - \frac{V_{DD}}{2} \right)$$

Upper Limit $v_{out} = V_{DD}$

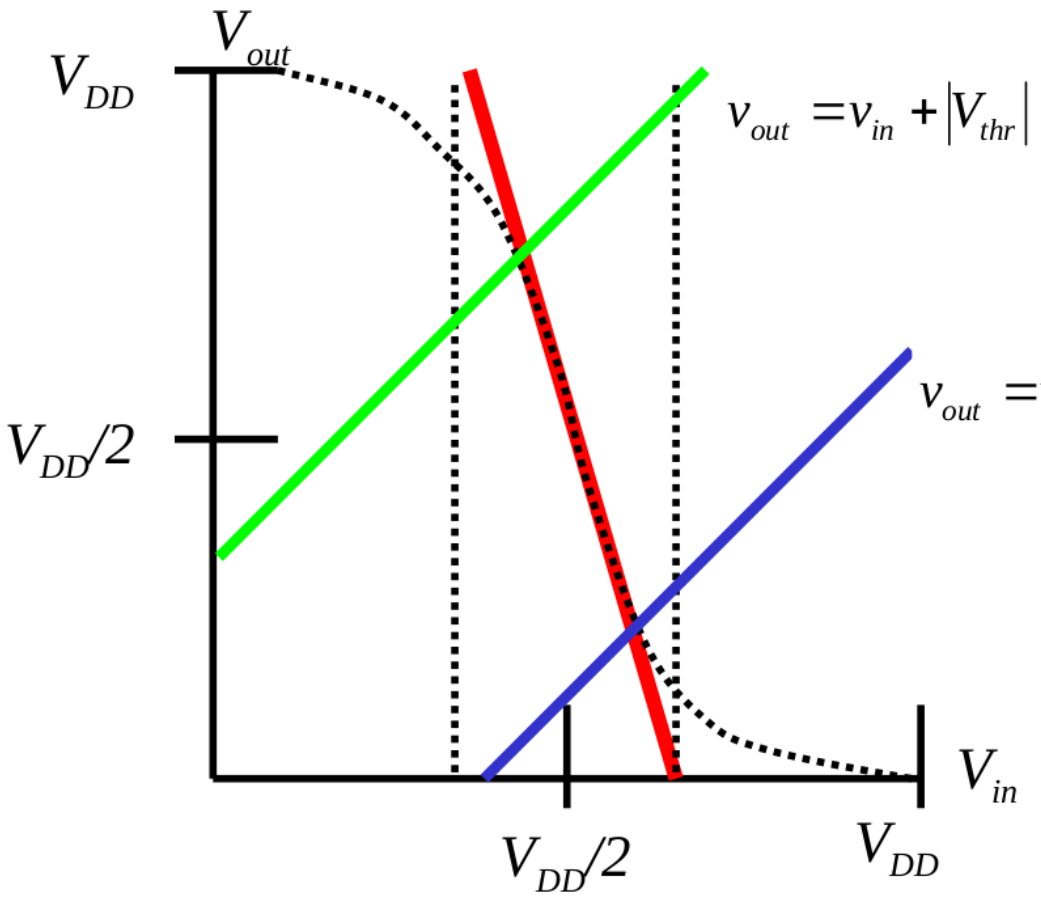
$$\frac{V_{DD}}{2} = - \frac{V_{DD} + 2V_A}{V_{DD} - 2V_{thr}} \left(v_{in} - \frac{V_{DD}}{2} \right)$$

$$v_{in} = \frac{V_{DD}}{2} - \frac{V_{DD}}{2} \frac{V_{DD} - 2V_{thr}}{V_{DD} + 2V_A}$$

Lower Limit $v_{out} = 0$

$$v_{in} = \frac{V_{DD}}{2} + \frac{V_{DD}}{2} \frac{V_{DD} - 2V_{thr}}{V_{DD} + 2V_A}$$

Regions of Operation



It is left as an exercise for the student to calculate the curve in the other two regions.

Inverter Power Consumption

Midpoint of Switching Operation (Peak Current)

$$v_{in} = v_{out} \frac{V_{DD}}{2} \qquad i_D = \mu C_{ox} \frac{W}{L} \frac{\left(\frac{V_{DD}}{2} - V_{thr} \right)^2}{2} \left(1 + \frac{V_{DD}}{2V_A} \right)$$

Peak Power in Two Transistors

$$P = 2 \frac{V_{DD}}{2} \mu C_{ox} \frac{W}{L} \frac{\left(\frac{V_{DD}}{2} - V_{thr} \right)^2}{2} \left(1 + \frac{V_{DD}}{2V_A} \right) \approx V_{DD} \mu C_{ox} \frac{W}{L} \frac{\left(\frac{V_{DD}}{2} - V_{thr} \right)^2}{2}$$

Average Power is Hundreds of Microwatts

$$P_{Average} < V_{DD} \mu C_{ox} \frac{W}{L} \frac{\left(\frac{V_{DD}}{2} - V_{thr} \right)^2}{2} \approx 200 \times 10^{-6} \text{A/V}^2 (\text{few Volts})$$

Inverter Speed

Assume load is the capacitance of the next gate

$$\tau \approx RC \approx \frac{C_{ox}WL}{\mu C_{ox}\frac{W}{L}V_{DD}} = \frac{L^2}{\mu V_{DD}}$$

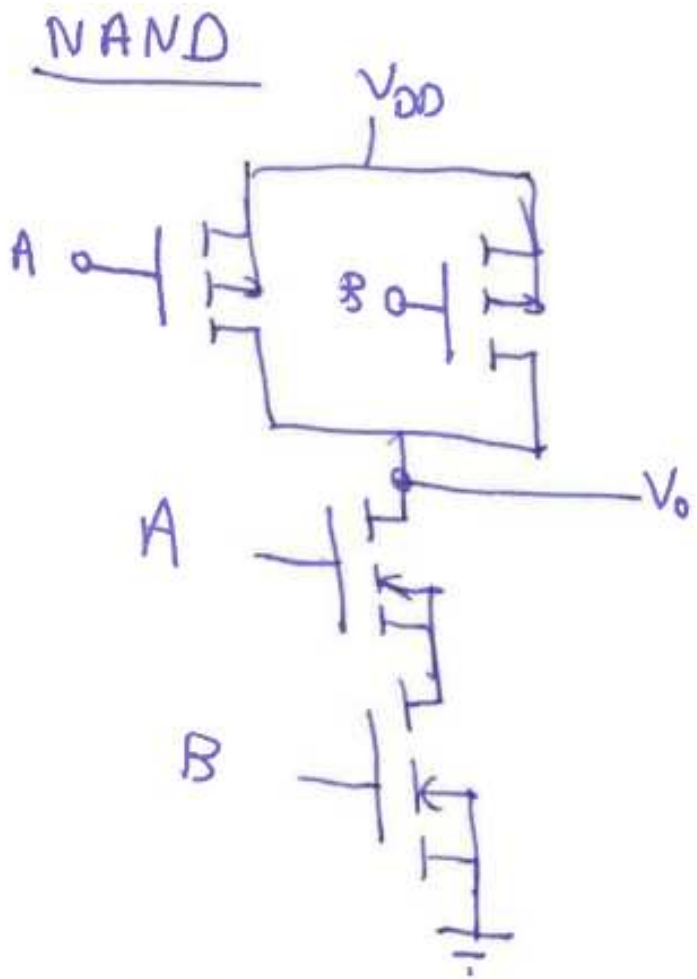
$$\tau \approx \frac{(10\times10^{-4}\text{cm})^2}{(480\text{cm}^2/\text{V/s})\times 5\text{V}} = 4\times10^{-10}\text{s}$$

Switching Time is nanoseconds

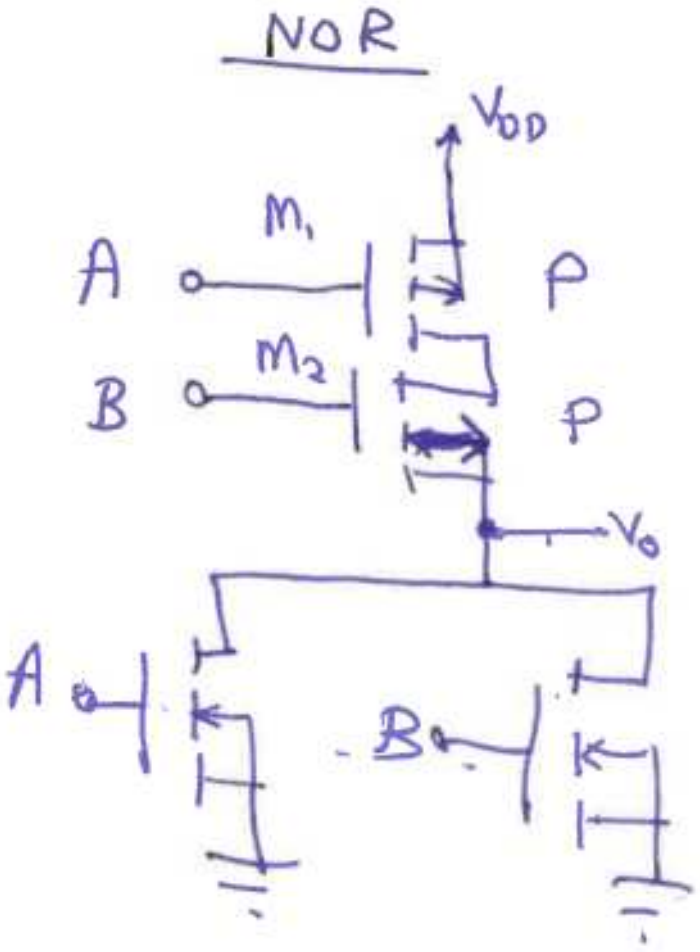
Energy to Switch is $J = P\tau \approx 10^{-4}\text{W}\times10^{-9}\text{s} = 10^{-13}\text{Joules}$

10^6 Electrons!

CMOS NAND



CMOS NOR



A	B	OUT
H	H	L
H	L	L
L	H	L
L	L	H

Not (A or B)

Some Thoughts on Limits

$$\frac{\left(10^6 \pm \sqrt{10^6}\right)\text{Electrons}}{10^{-9}\text{seconds}} \times \text{Number of Units} \times \text{Duty Cycle}$$

$$10^{-4}\,\text{Watts} \times \text{Number of Units} \times \text{Duty Cycle}$$

- Where do we go from here?
  - Speed?
  - Parallel Computing?
  - Something totally new?