Fundamentals of Electronics
Week 13 — Review

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Nov 2024

Field–Effect Transistor (1)

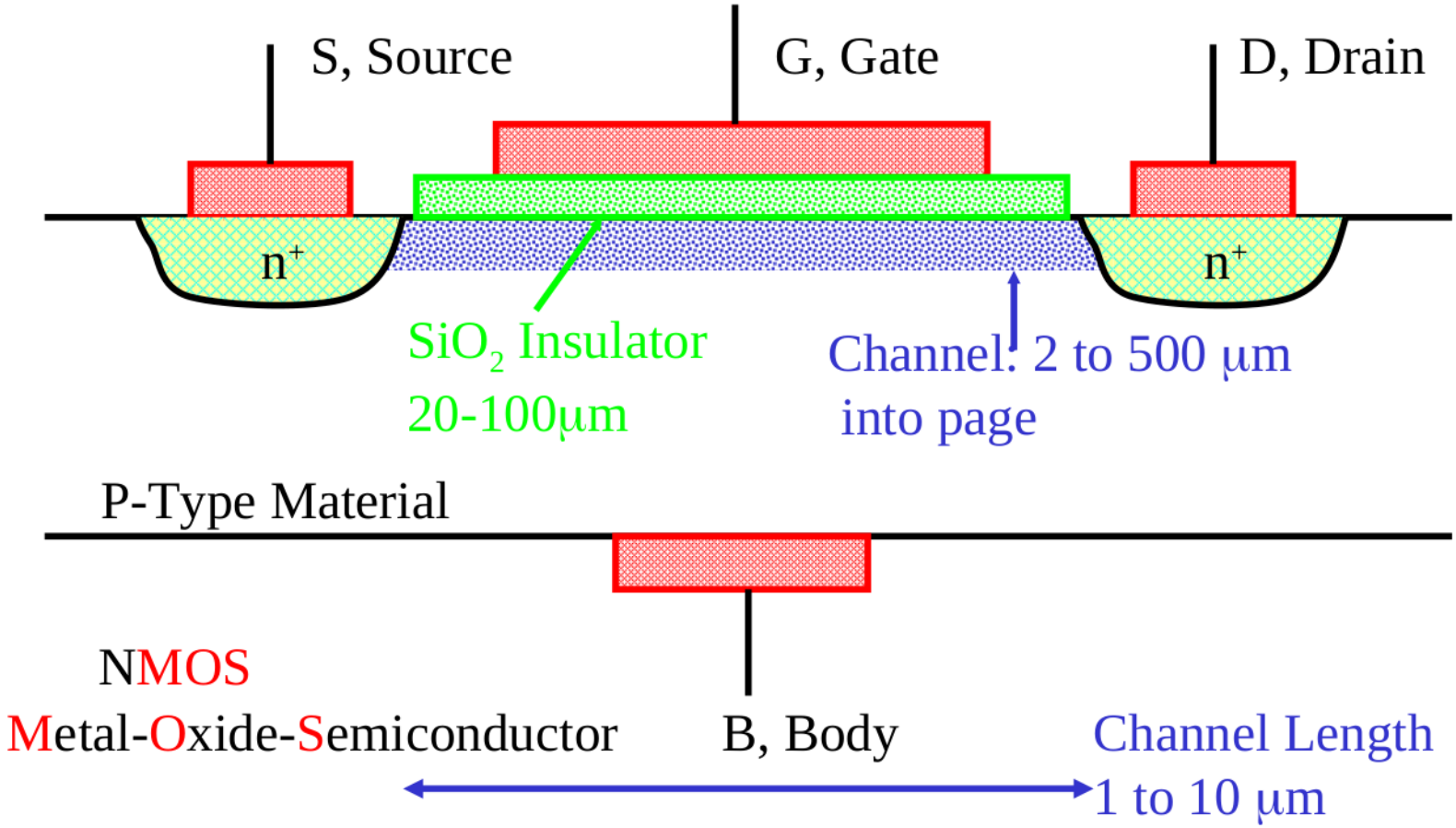
- Different Physics, Some Different Equations. . .
- . . . but Many Similarities
- Similar Materials
  - Silicon
  - P– and N–Doped
- 3 Terminals
  - Emitter $\longleftrightarrow$ Source
  - Base $\longleftrightarrow$ Gate
  - Collector $\longleftrightarrow$ Drain

Field–Effect Transistor (2)

- 3 Operating Regions
  - Active $\longleftrightarrow$ Saturation (Amplifiers)
  - Saturation $\longleftrightarrow$ Triode (Logic)
  - Cutoff $\longleftrightarrow$ Cutoff (Logic)

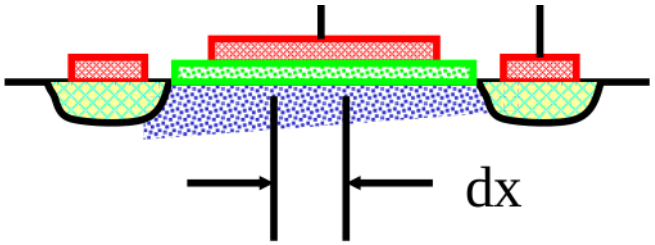
- 3 Amplifers
  - Common Emitter $\longleftrightarrow$ Common Source (Large A_v)
  - Common Base $\longleftrightarrow$ Common Gate ($A_i = 1$)
  - Common Collector $\longleftrightarrow$ Common Drain ($A_v = 1$)

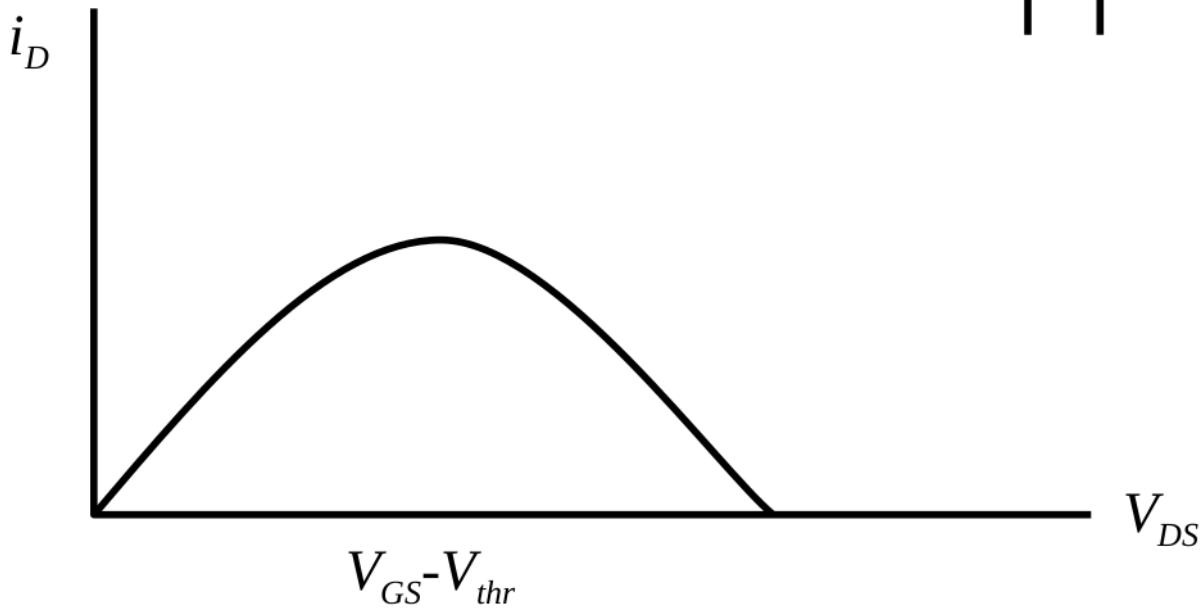
N–FET Structure



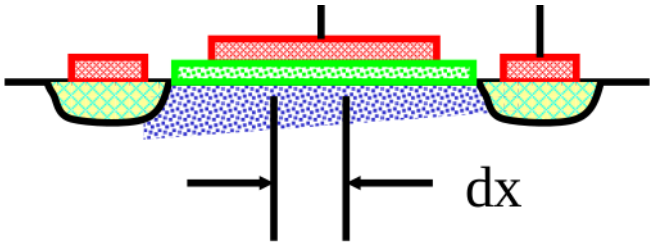
N–FET Equations (4)

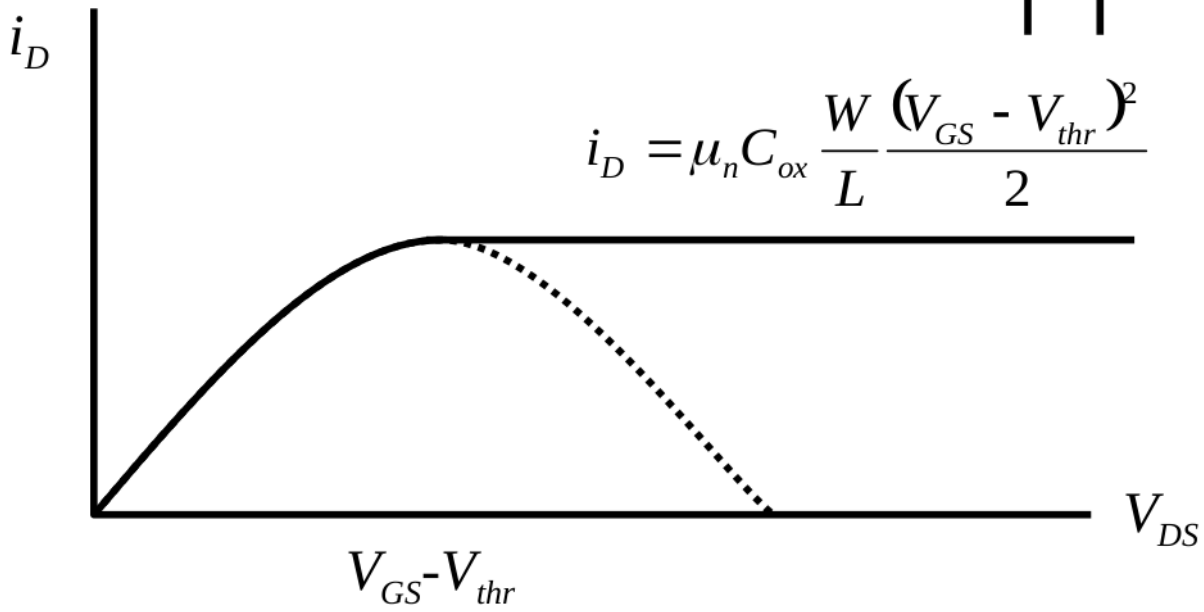
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{thr})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$





Saturation Region





Triode–Saturation Boundary

Triode

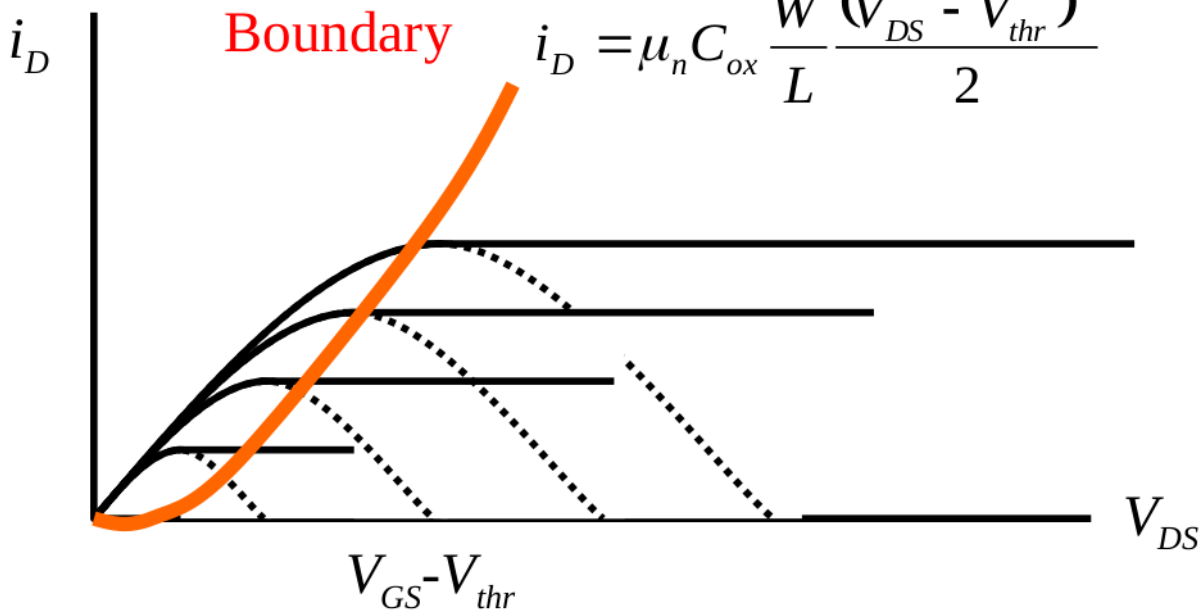
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{thr})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Saturation

$$i_D = \mu_n C_{ox} \frac{W}{L}\frac{(V_{GS} - V_{thr})^2}{2}$$

Boundary

$$i_D = \mu_n C_{ox} \frac{W}{L}\frac{(V_{DS} - V_{thr})^2}{2}$$



The Early Voltage

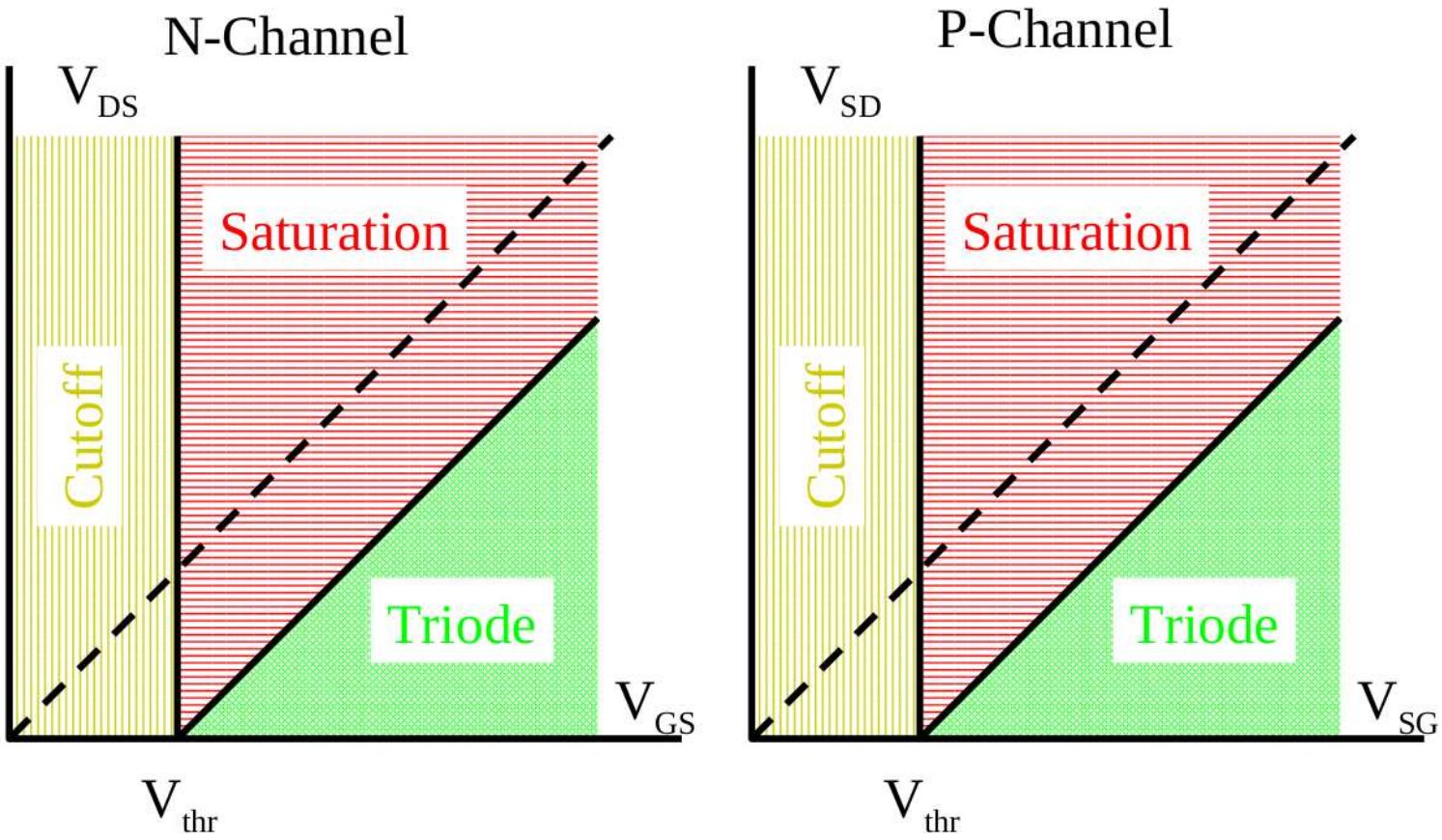
- Effect of Pinch Off as Resistance
  - Increasing Current with Voltage

Previous Eqn. for Saturation $$i_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2}$$

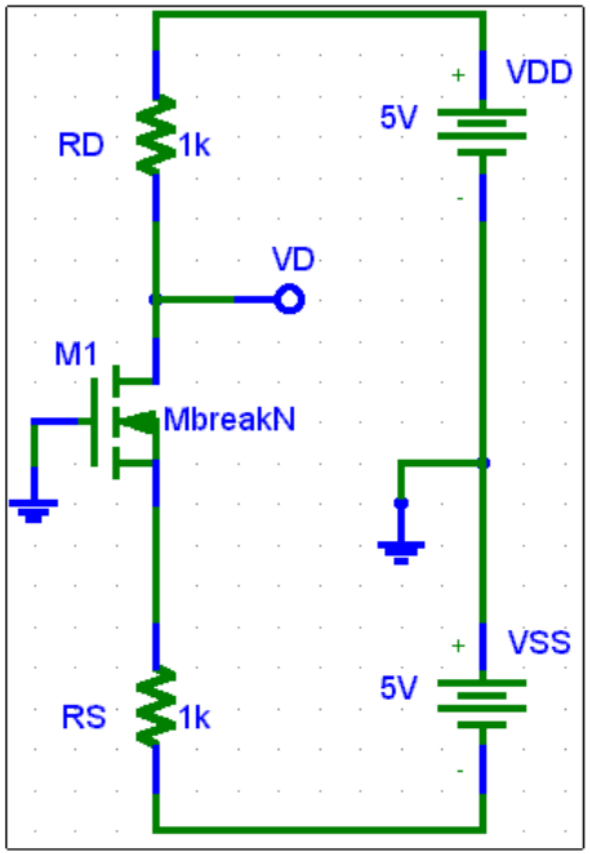
Modified $$i_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{thr})^2}{2} (1 + \lambda V_{DS})$$

$$\lambda = \frac{1}{V_A}$$

Regions of FET Operation



DC FET Circuit Example (5.1)



Given:

L=10 μm, W =400 μm

k'_n=20 μA/V^2, λ=0

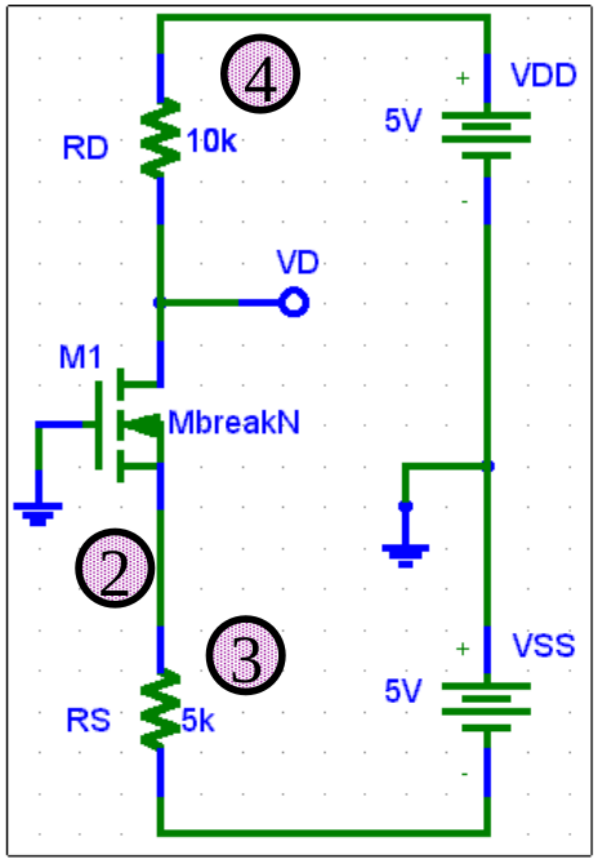
V_{thr}=2V

Goal:

I_D=0.4mA

V_D=1V

Solve Problems Like This: 5.1



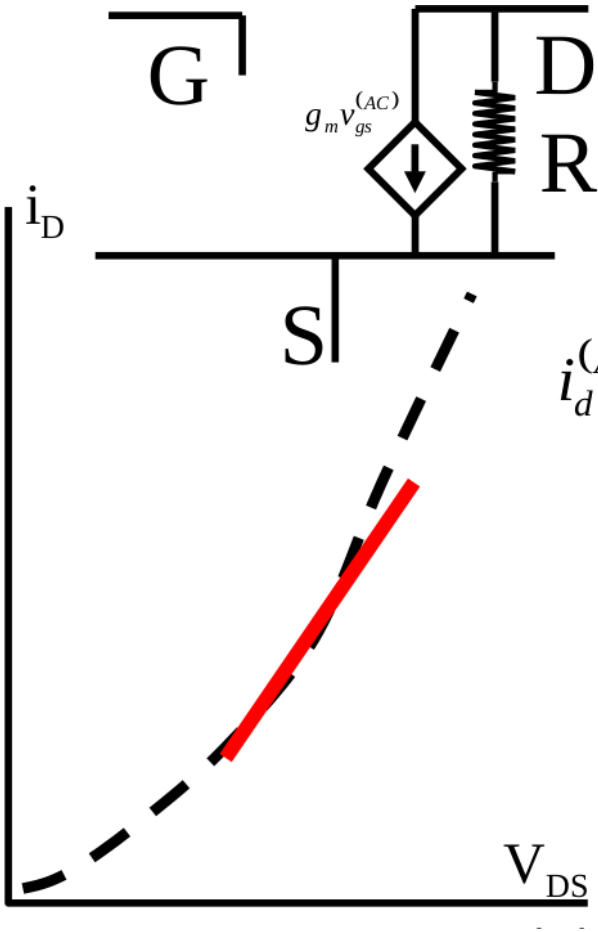
V_{GS}=3V

V_S=-3V

3 $R_S = \frac{|(-3)-(-5)|\text{V}}{0.4\text{mA}} = 5k\Omega$

4 $R_D = \frac{|5-1|\text{V}}{0.4\text{mA}} = 10k\Omega$

AC Performance (2)



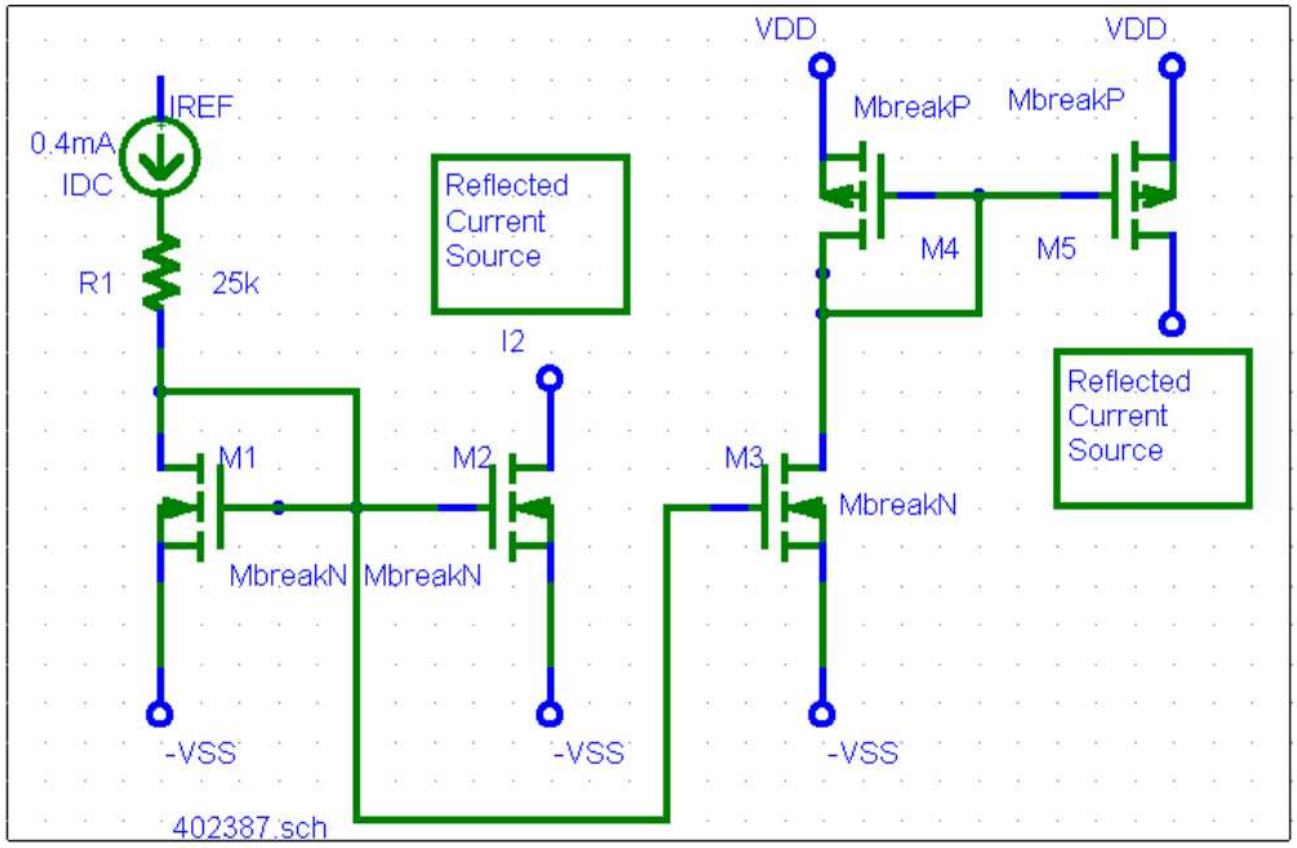
$$I_D^{(DC)} = k'_n \frac{W}{L} \frac{\left(V_{GS}^{(DC)} - V_{thr}\right)^2}{2}$$

$$i_d^{(AC)} \approx k'_n \frac{W}{L}\left(V_{GS}^{(DC)} - V_{thr}\right) v_{gs}^{(AC)} = g_m v_{gs}^{(AC)}$$

$$g_m = k'_n \frac{W}{L}\left(V_{GS}^{(DC)} - V_{thr}\right)$$

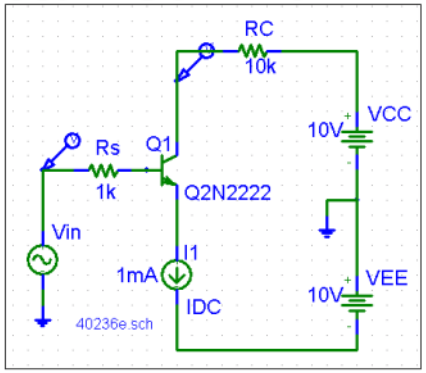
$$g_m = \frac{2I_D^{(DC)}}{\left(V_{GS}^{(DC)} - V_{thr}\right)}$$

Current Steering Circuit

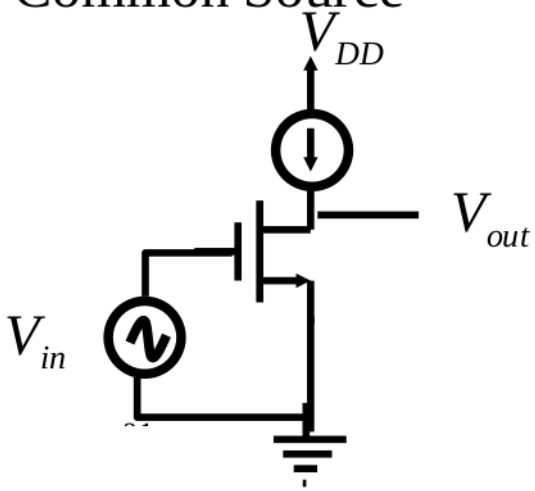


FET Amplifiers

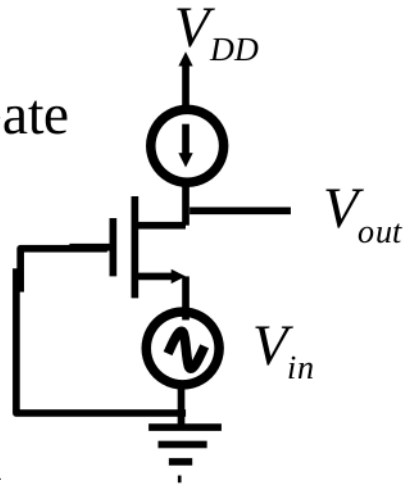
Recall Common Emitter



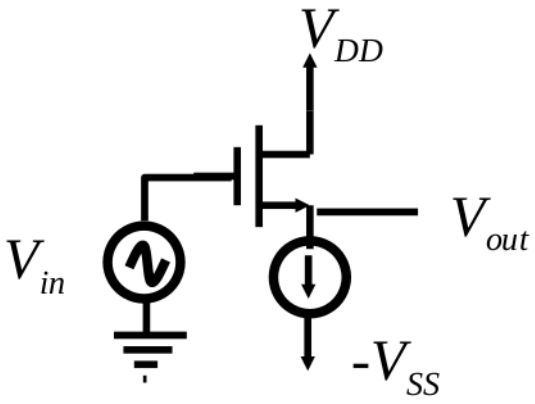
Common Source



Common Gate



Common Drain

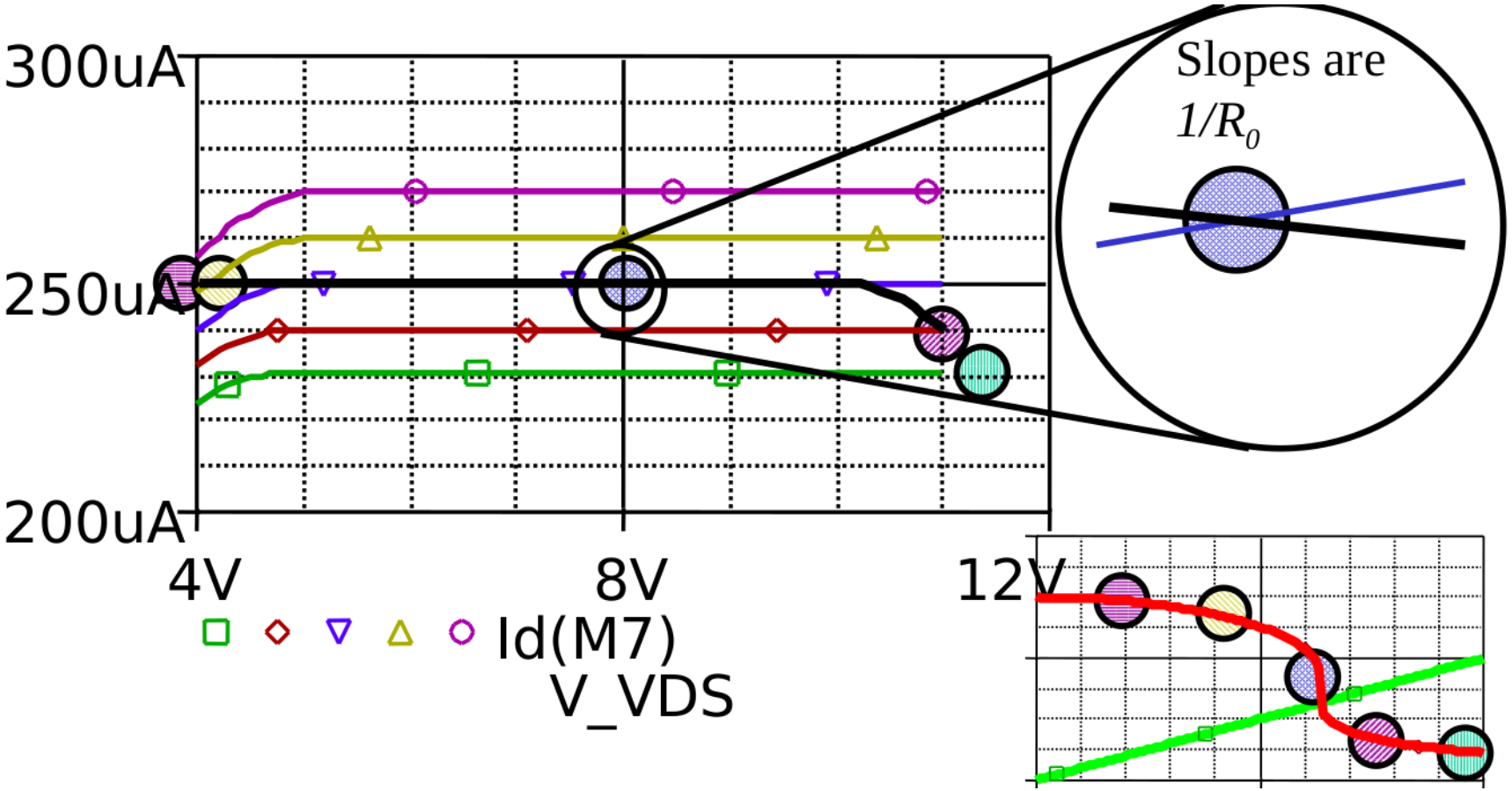


Note that "Current Source" Also serves as load

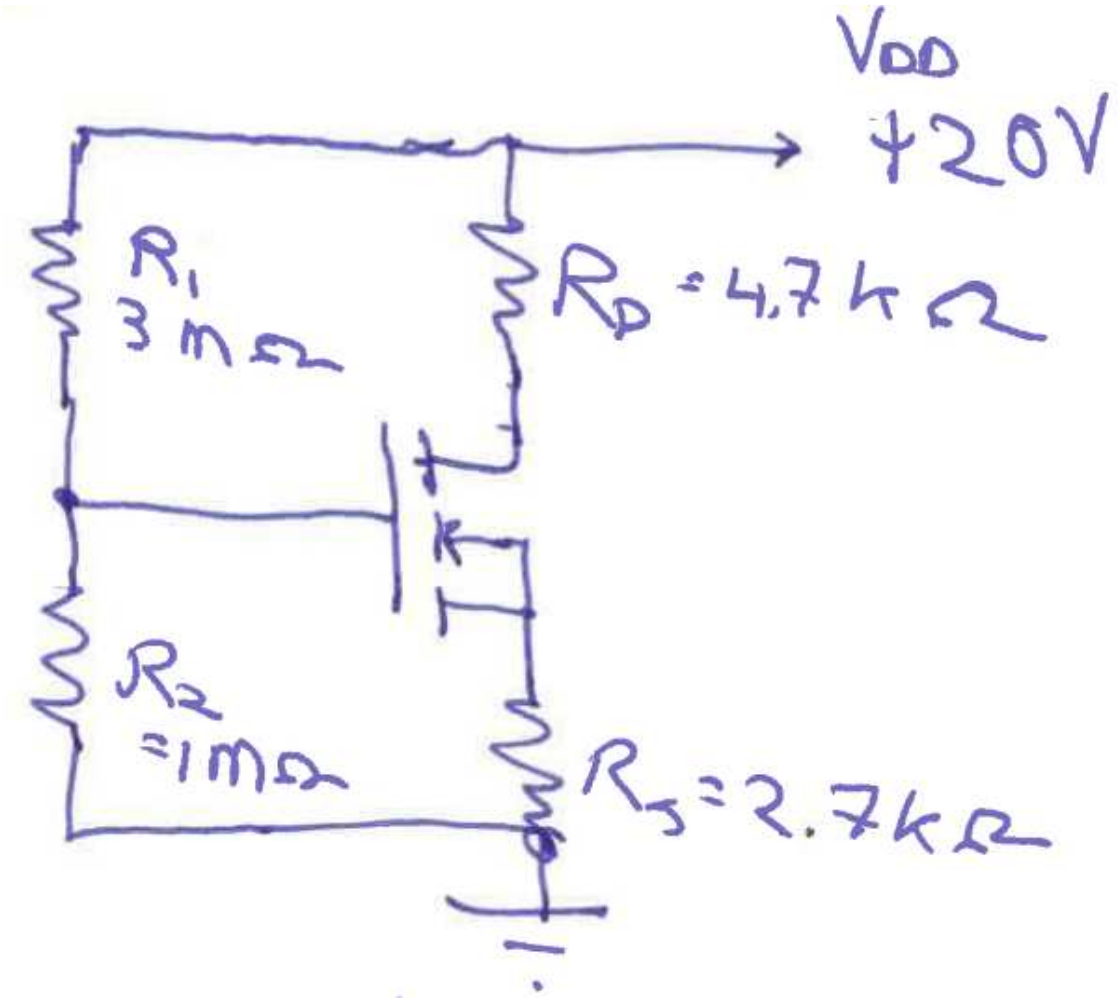
FET Amplifier Summary

	Voltage Gain	Current Gain	Input Resistance	Output Resistance
CS	$-\sqrt{2k'_n \frac{W_1}{L_1}} \frac{V_A}{\sqrt{I_{REF}^{(DC)}}}$		Infinite	$\frac{V_{A1}}{I_D^{(DC)}} \parallel \frac{V_{A2}}{I_D^{(DC)}}$
CG	$\left[\frac{1}{R_{01}} + (1+\chi)\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}\right](R_{01} \parallel R_{02} \parallel R_L)$	$1 + \frac{R_L}{R_{02}} \approx 1$	$\frac{1}{(1+\chi)\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}}\left(1 + \frac{R_{02} \parallel R_L}{R_{01}}\right)$	$\frac{V_{A1}}{I_D^{(DC)}} \parallel \frac{V_{A2}}{I_D^{(DC)}}$
CD	$\frac{\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}}{\sqrt{2k'_n \frac{W_1}{L_1} I_{REF}^{(DC)}}(1+\chi_1) + \frac{1}{R_{01}} + \frac{1}{R_{02}}} \approx 1$		Infinite	$\approx \frac{1}{\sqrt{k'_n \frac{W}{L} I_{D1}^{(DC)}(1+\chi)}}$

Expanded Graphical Analysis: Active Load



DC FET Solutions (1)



Remember:

$k'_n = \mu_n C_{ox}$

NFET Parameters:

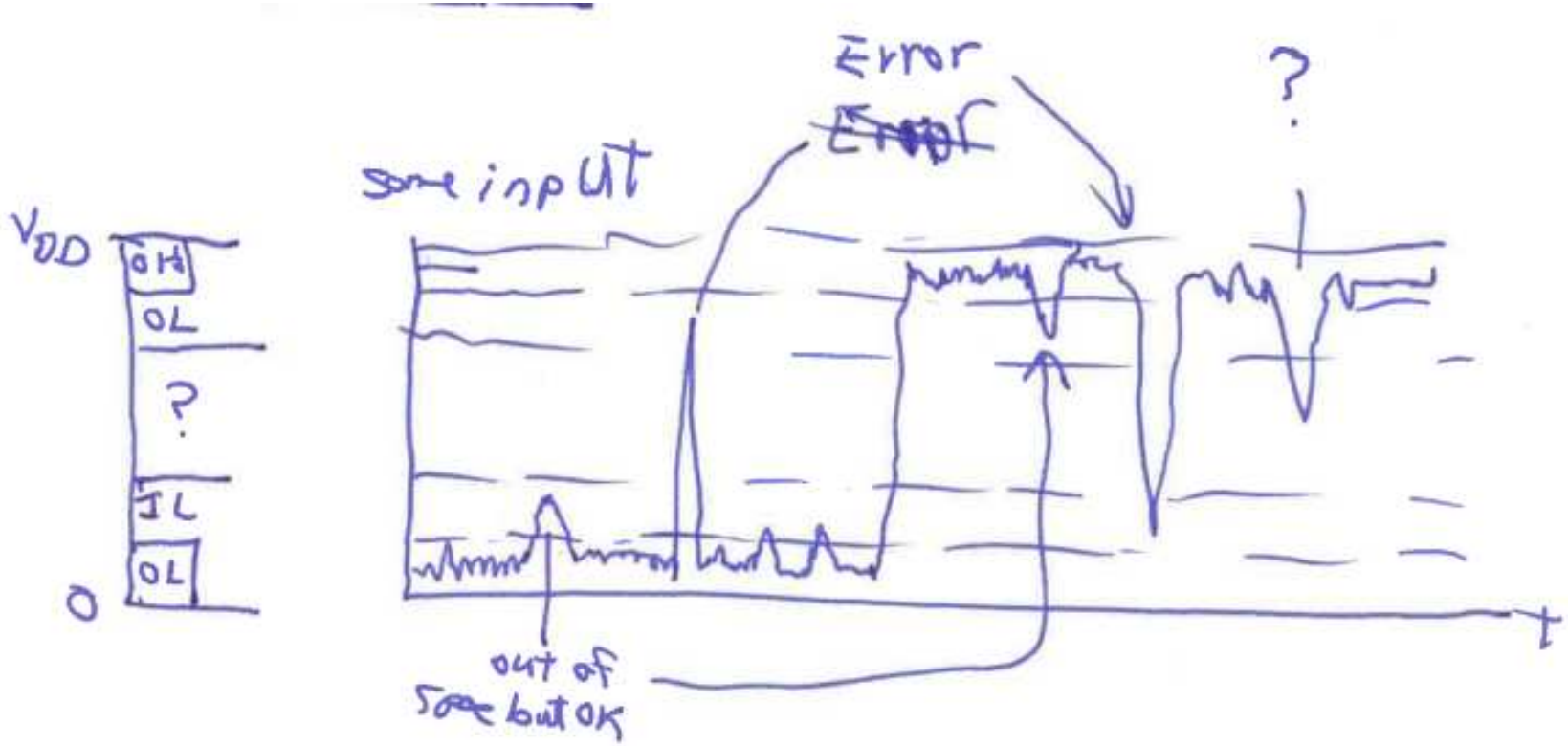
$k'_n = 50\mu\text{A/V}^2$,

$W = 400\mu\text{m}$,

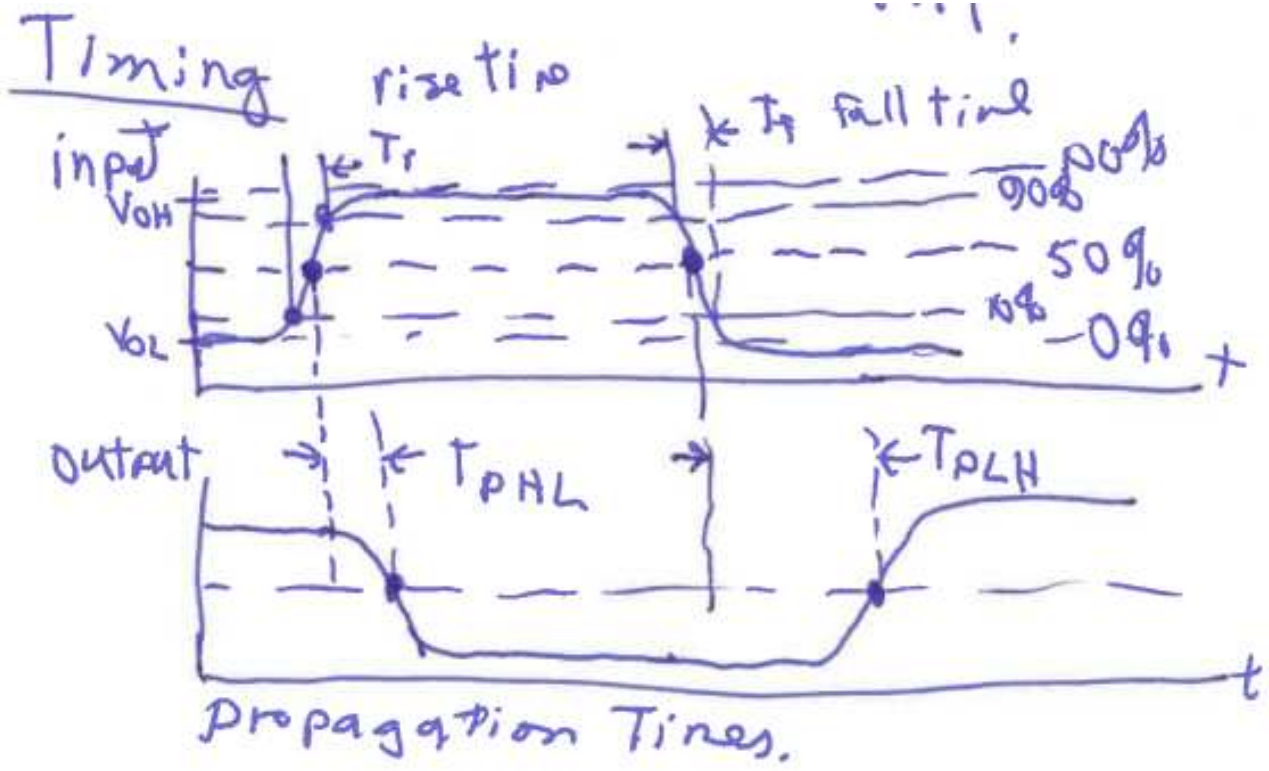
$L = 10\mu\text{m}$,

$V_T = 2\text{V}$.

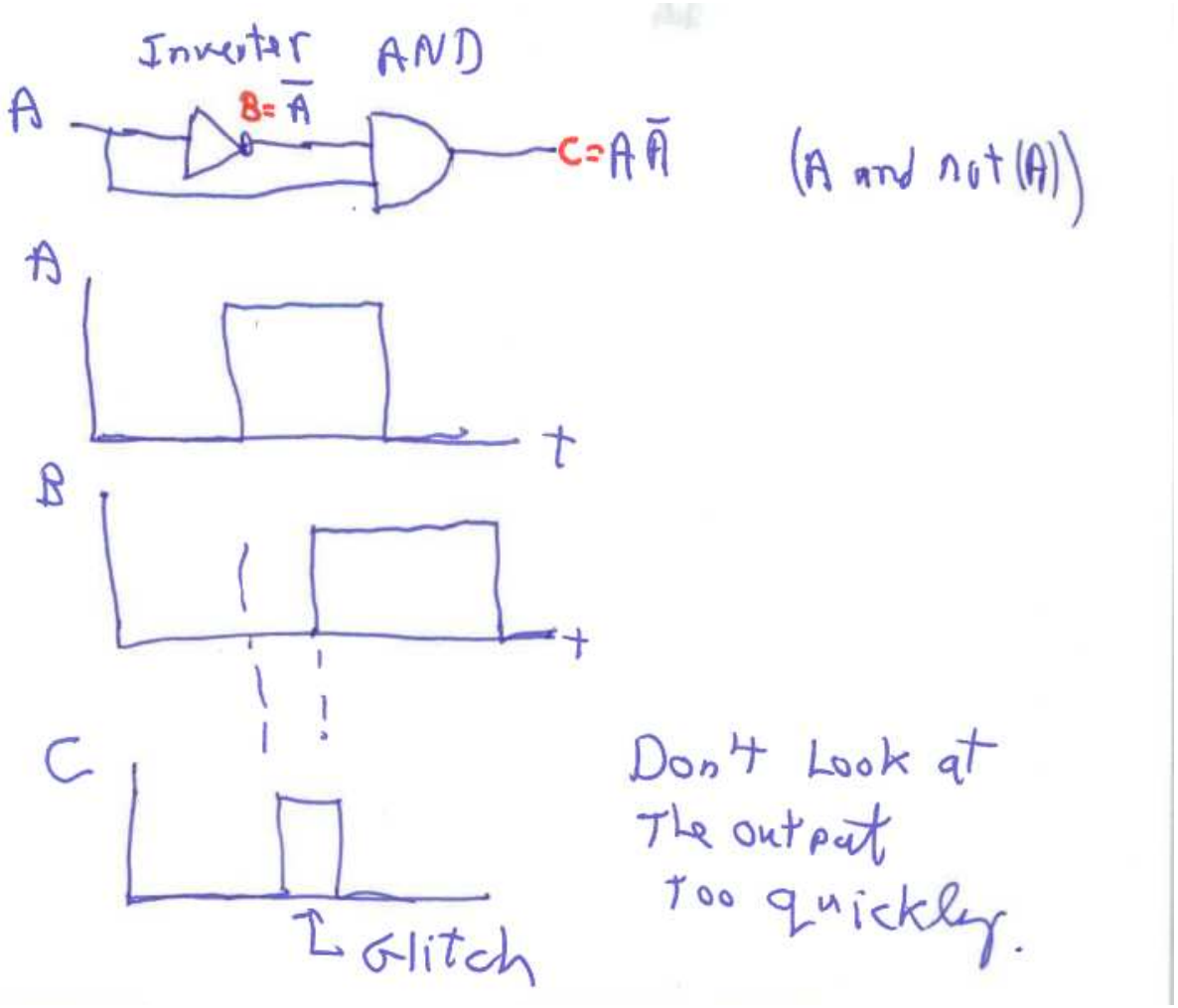
Noise in Logic



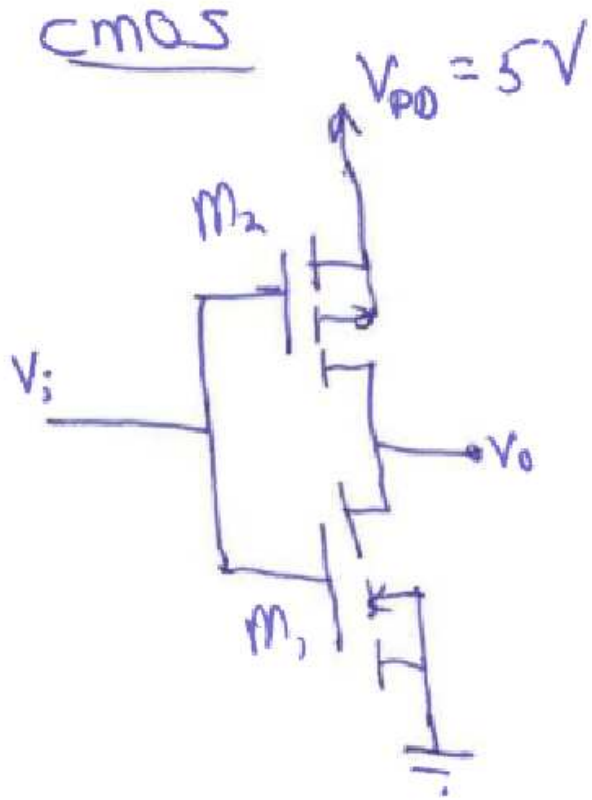
Timing in Logic



Glitch


Inverter
AND
A
B = $\bar{A}$
C = A $\bar{A}$
(A and not (A))
A
t
B
t
C
Glitch
Don't Look at
The output
too quickly.

CMOS Logic Inverter



input	0	5
V_{GS1}	0	5
V_{SG2}	5	6 — cutoff
V_o	5	0

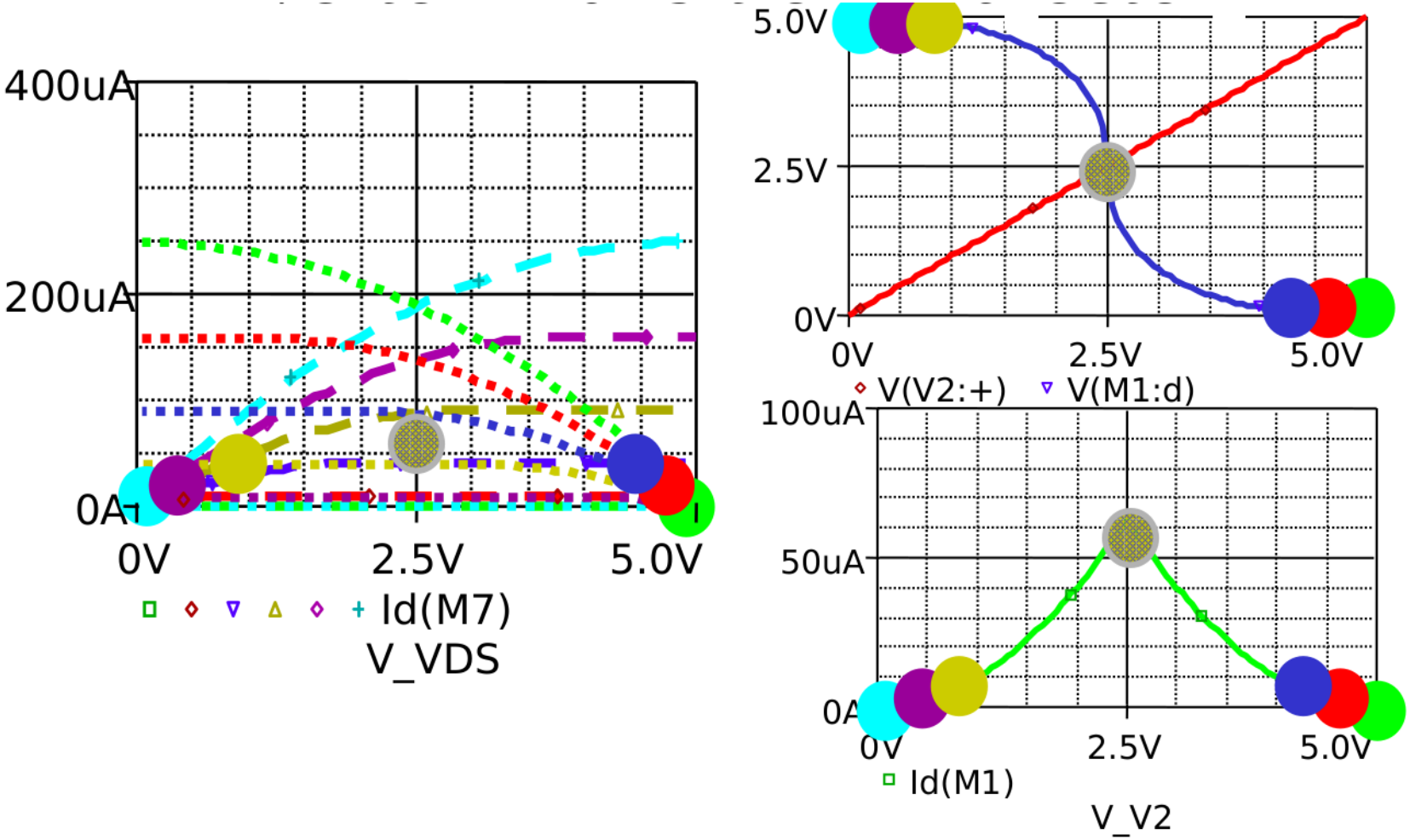
Little detail

$$K_{P(P)} = \frac{K_{P(n)}}{2}$$

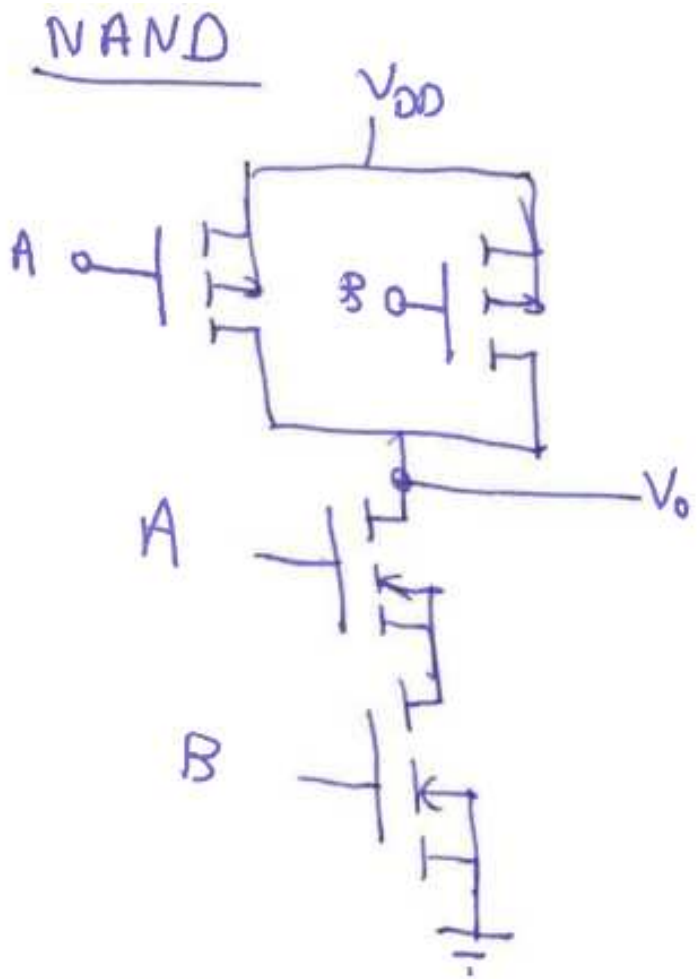
$$\left(\frac{W}{L}\right)_P = 2\left(\frac{W}{L}\right)_n$$

$$K_{(P)} = K_{(n)}$$

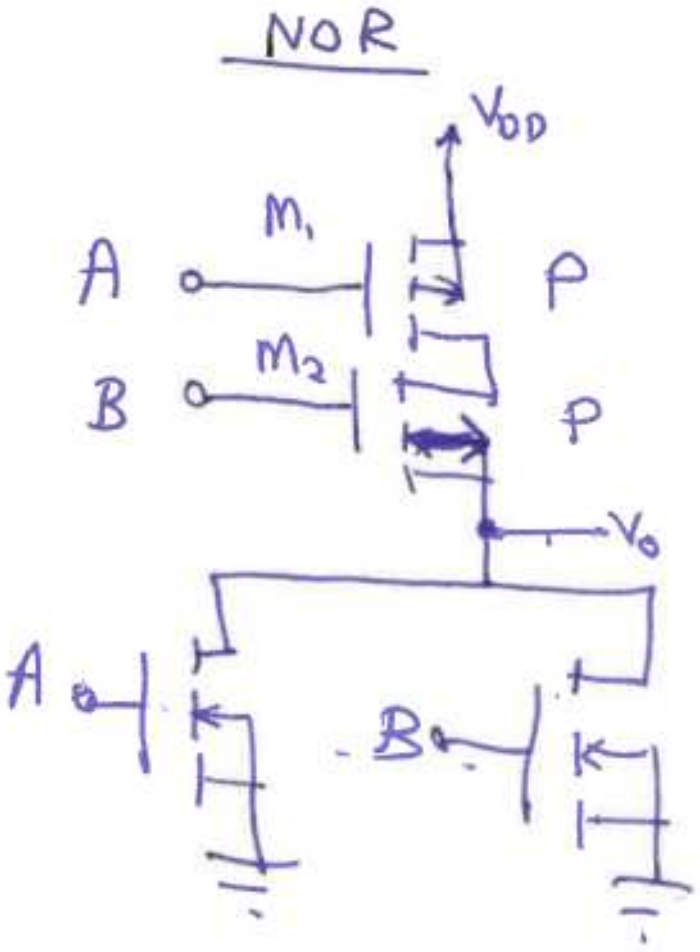
Inverter Transition Trajectory



CMOS NAND



CMOS NOR



A	B	OUT
H	H	L
H	L	L
L	H	L
L	L	H

Not (A or B)