Fundamentals of Electronics
Week 9 Continued

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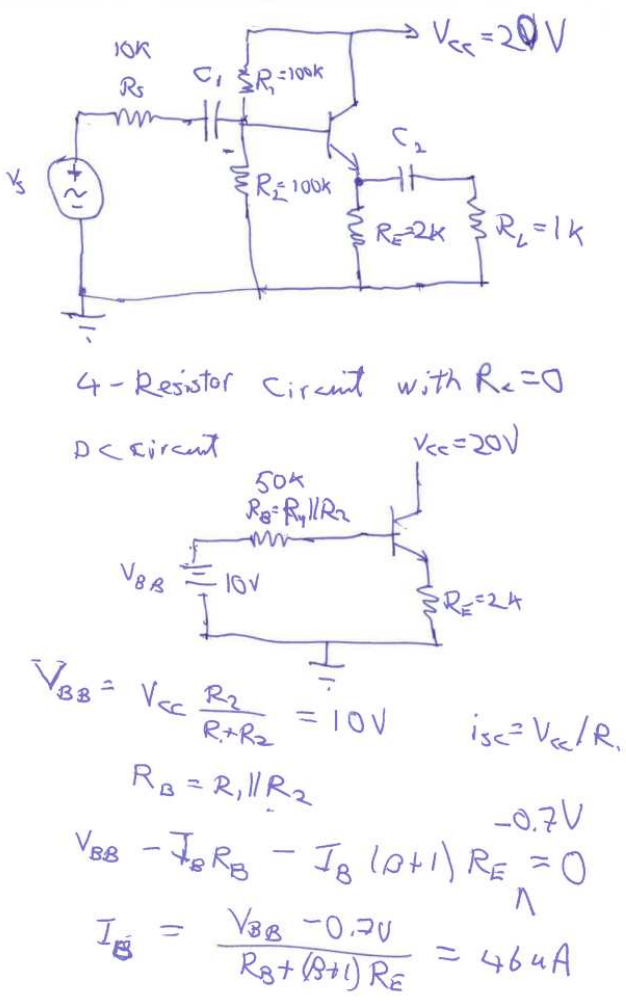
Nov 2024

Agenda

- Amplifier In–Class Exercise
- Cutoff and Sauturation
  - Graphical Analysis
  - Saturation Models
- 3 Regions of Operation
- Logic
  - Inverter
  - NOR (Not OR)
  - NAND (Not AND)

Common Collector Example (1)

- Goal: $A_V = 1$ for AC
- Solve DC
- AC Parameters: r_π
- Solve AC "Midband"
- Solve AC vs. Frequency

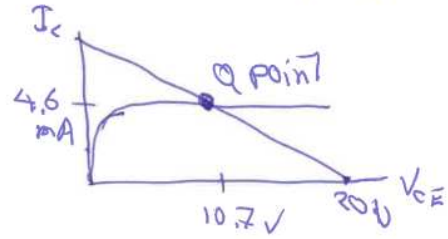


Common Collector Example (2)

- Finish DC
- AC Parameters: r_π
- Start AC Solution

$I_C = \beta I_B = 4.6\,mA$ (Good!)

$V_{CE} = V_C - (\beta+1) I_B R_E = 10.7\,V$

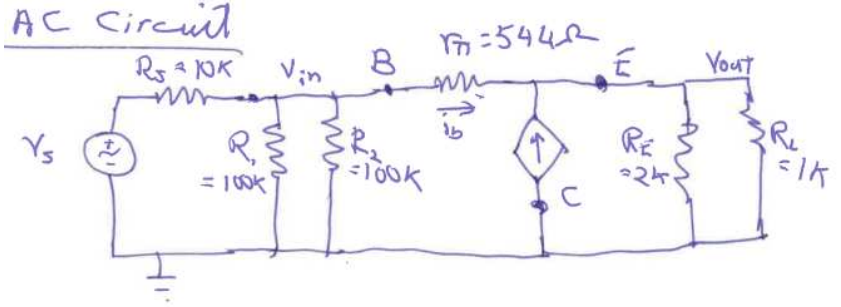


Small signal model

$r_\pi = \frac{\beta V_t}{I_C} = \frac{100 \times 25mV}{4.6\,mA} = 544\,\Omega$

$\beta = 100$

AC circuit



Common Collector Example (3)

- Midband AC Analysis
- Then vs. Frequency

$$Z_S = R_S + \frac{1}{j\omega C_1}$$

$$Z_L = R_L + \frac{1}{j\omega C_2}$$

New $A + v$ multiplied by . . .

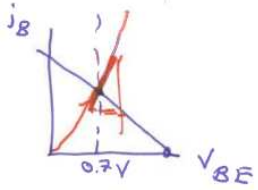
$$\frac{R_L}{Z_L}$$

$V_{in} = i_b r_\pi + (\beta+1) i_b (R_E \| R_L)$

$V_{out} = (\beta+1) i_b (R_E \| R_L)$

$A_v = \frac{V_{out}}{V_{in}} = \frac{R_E \| R_L}{R_E \| R_L + \frac{r_\pi}{\beta+1}} = \frac{666\,\Omega}{666\,\Omega \; \frac{544}{101}}$

$A_v = 0.992$



input impedance

$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{V_{in}}{i_b} = r_\pi + (\beta+1)(R_E \| R_L)$

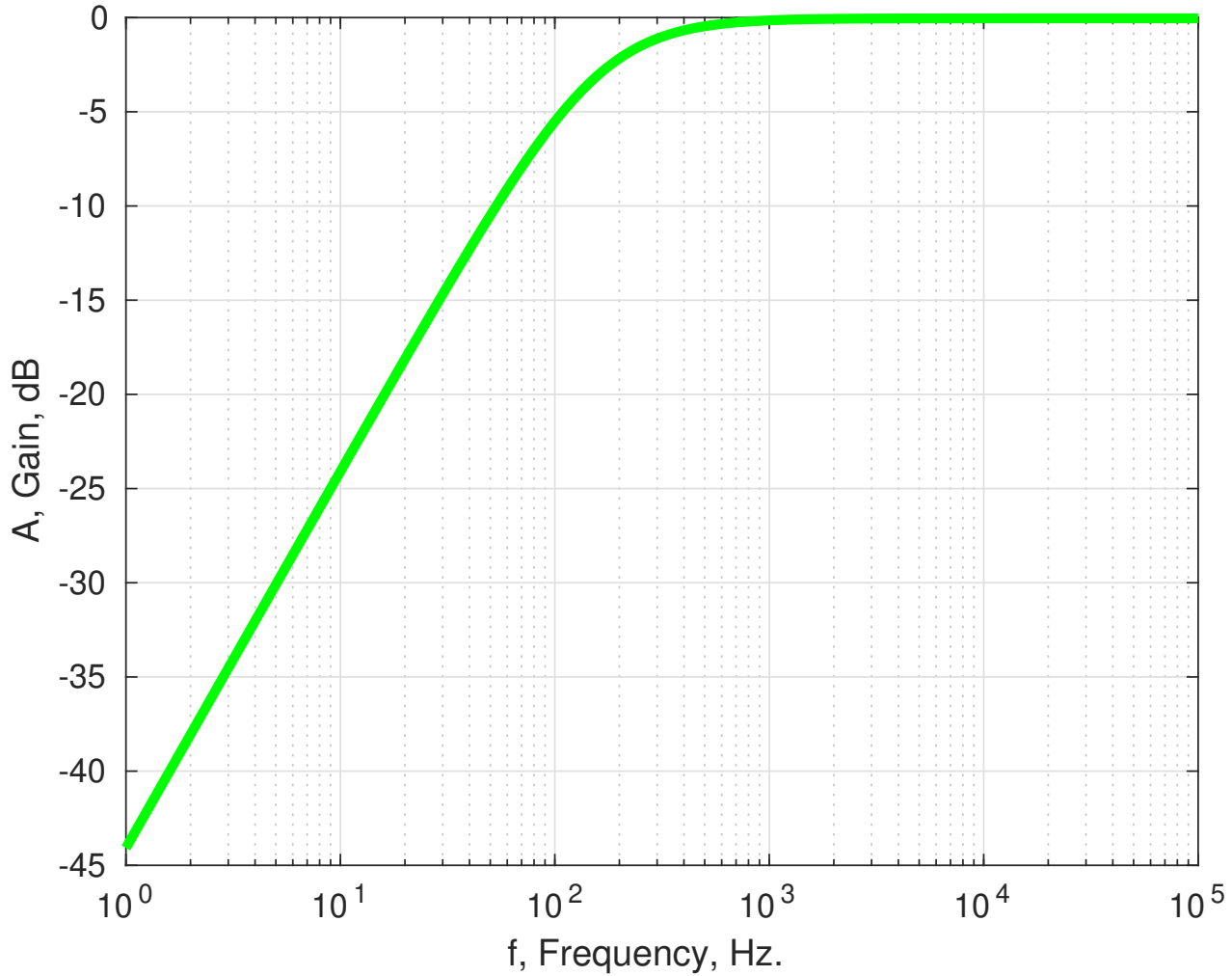
$= 544 + 101 \times 666 = 67.3k$

output impedance.

$z = R_E \| \frac{r_\pi + (R_S \| R_1 \| R_2)}{\beta+1} \approx 2k \| \frac{10k}{101}$

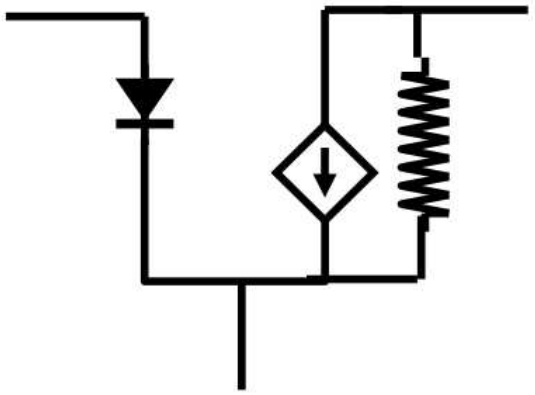
$z \; 100\,\Omega$

Common Collector Example (4)

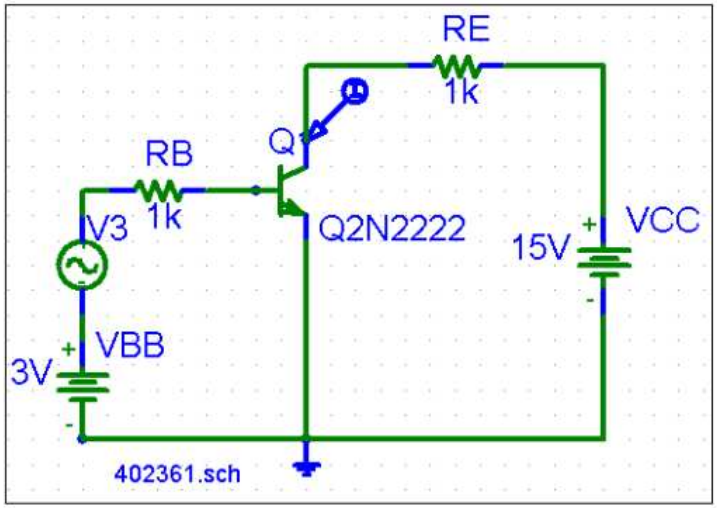


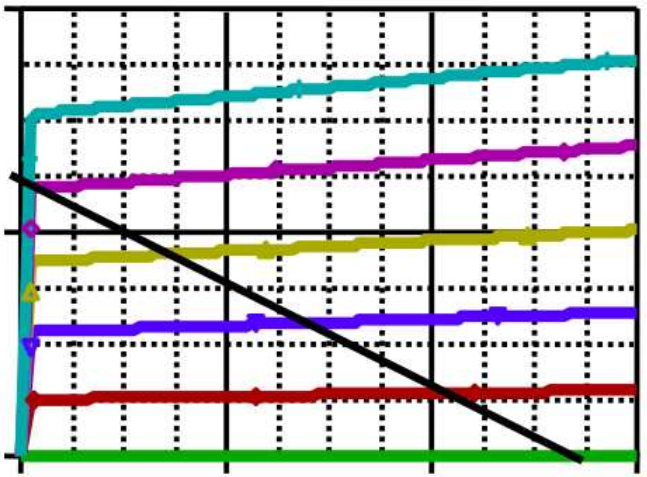
The Transistor So Far. . .

Pi Model



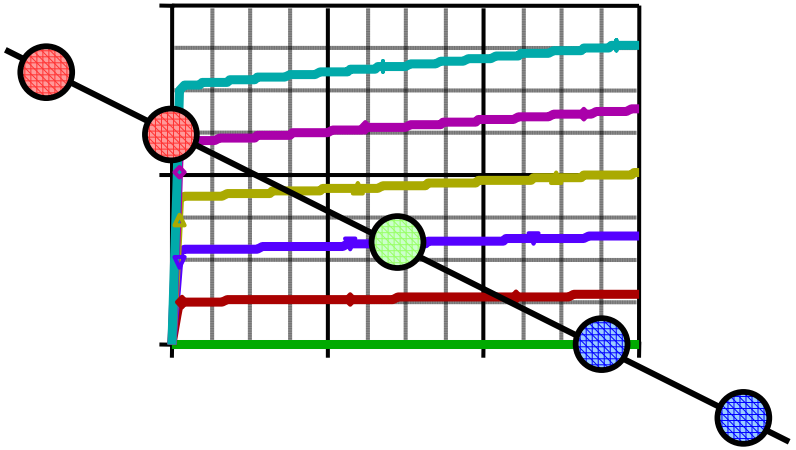
Pi Model Captures Active Mode Only. What if the external circuit can't satisfy this equation?



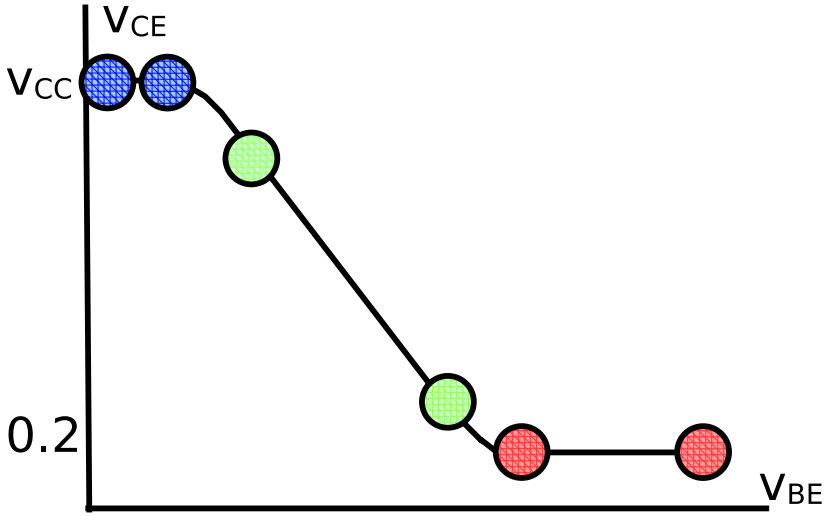


Active Mode Fails

- Solve Circuit assuming Active Mode
- Fail: $v_{CE} < 0$ Means Saturation
- Fail: $i_C < 0$ Means Cutoff

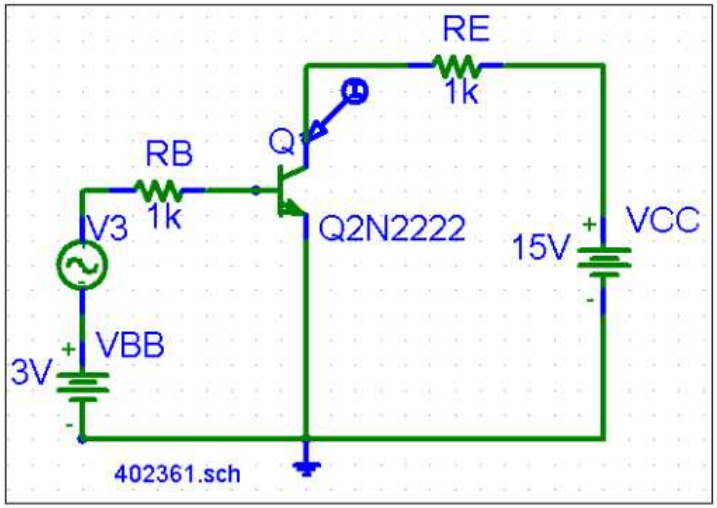


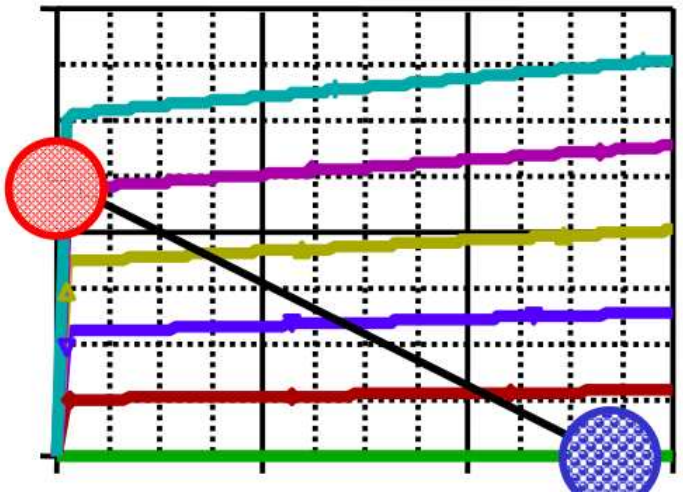
- Good Logic Device:
- Narrow Active Region
- Two Clear Answers Even If Input Varies a Bit



Transistor Modes

- Active Mode
  - Forward Biased BE Jct
  - Reverse Biased BC
- Cutoff Mode
  - Zero or Reverse BE
  - Zero or Reverse BC
- Saturation
  - Forward Biased BE
  - Forward Biased BC





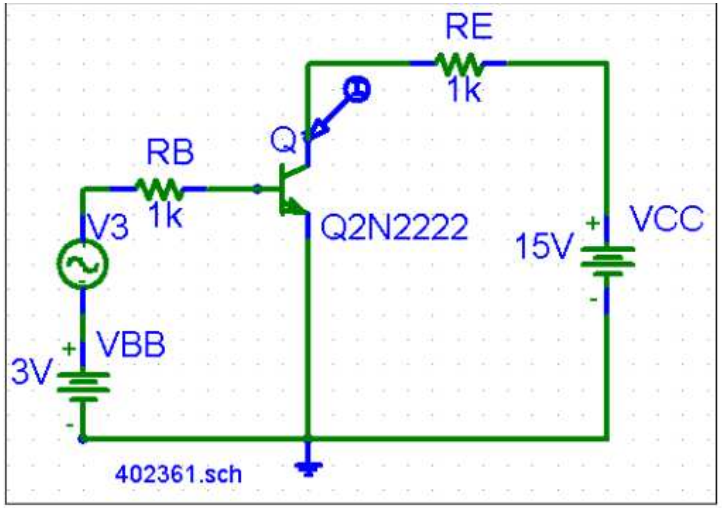
Cutoff

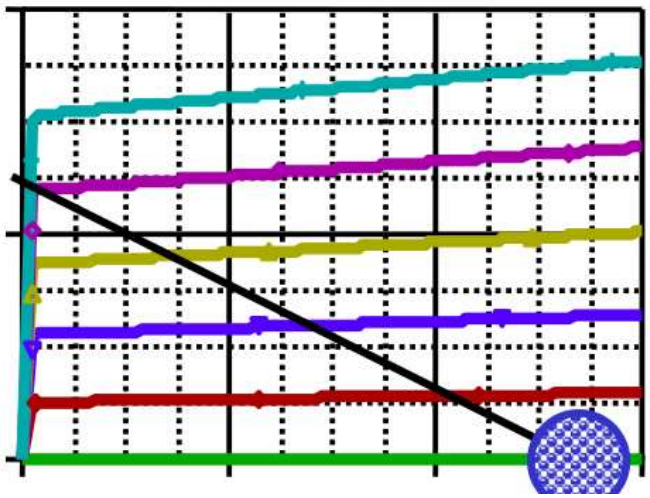
- Zero or Reverse BE Junction
- Zero or Reverse BC Junction

$$i_B = 0$$

$$i_C = 0$$

$$V_C = V_{CC}$$





Saturation, Simply (1)

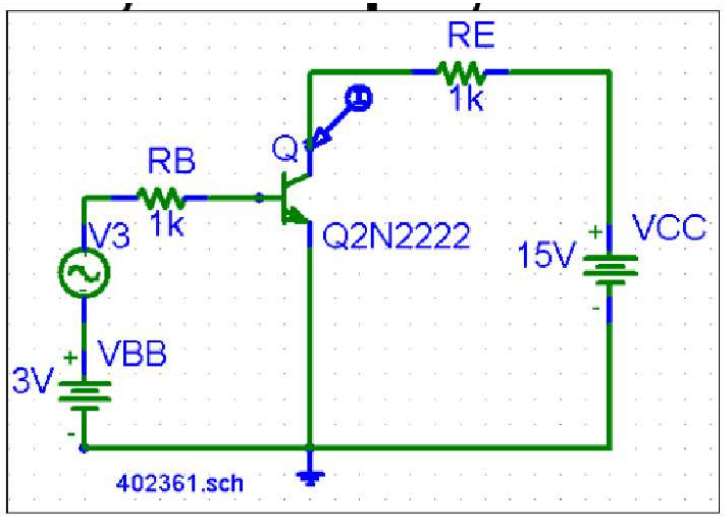
- Forward Biased BE Junction
- Forward Biased BC

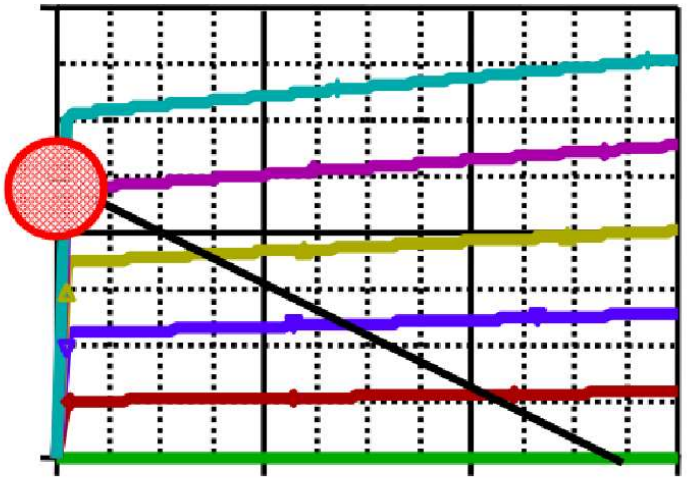
$$V_C \approx V_B$$

Saturation Current

$$\hat{I}_C = \frac{V_{CC} - V_B}{R_C}$$

$$\hat{I}_B = \frac{\hat{I}_C}{\beta}$$





Saturation Simply (2)

$$\hat{I}_C = \frac{V_{CC} - V_B}{R_C}$$

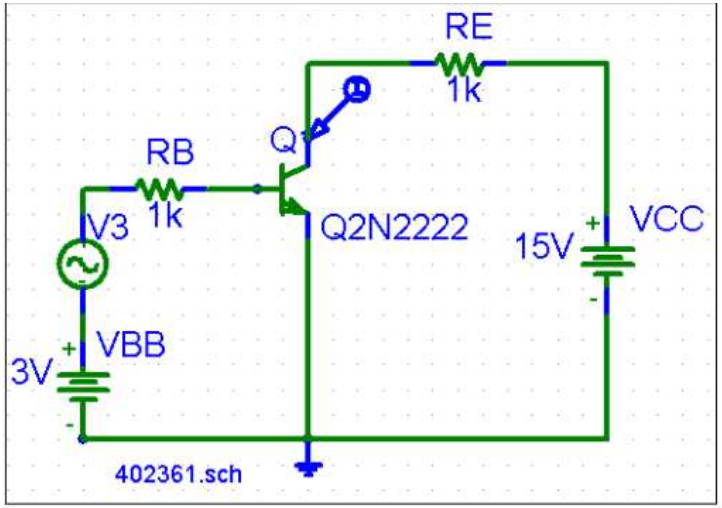
$$\hat{I}_B = \frac{\hat{I}_C}{\beta}$$

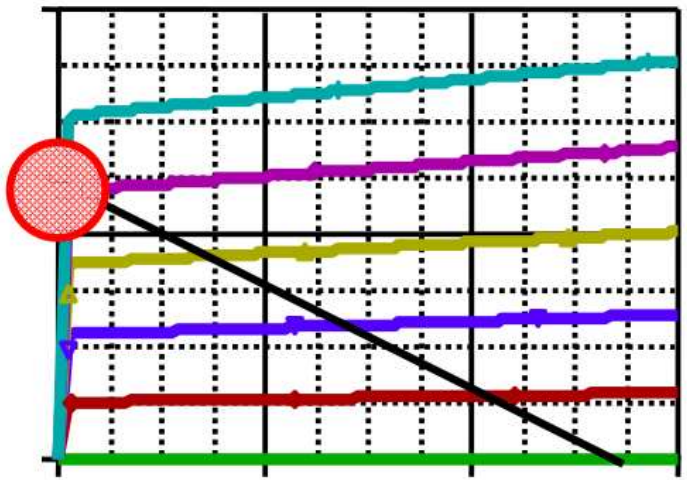
If the external circuit supplies

$$i_B > \hat{I}_B$$

Then

$$\frac{i_C}{i_B} < \beta$$



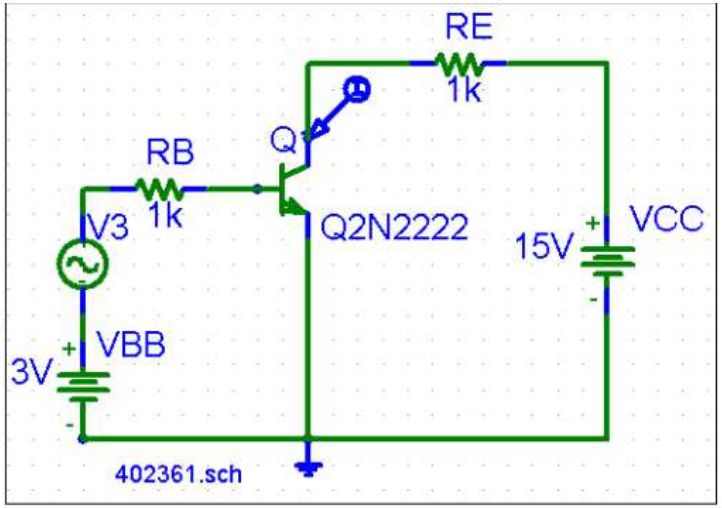


Saturation More Accurately

$$V_{BC} = 0.5 \text{ Volts}$$

$$V_{BE} = 0.7 \text{ Volts}$$

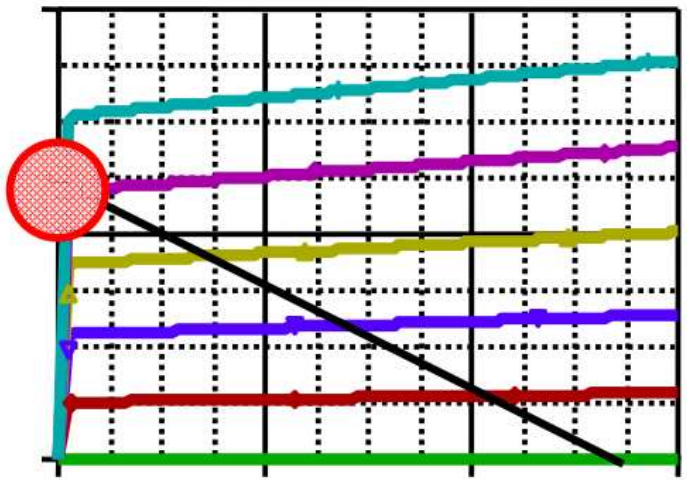
$$\hat{I}_C = \frac{V_{CC} - V_{CEsat}}{R_C} \approx$$



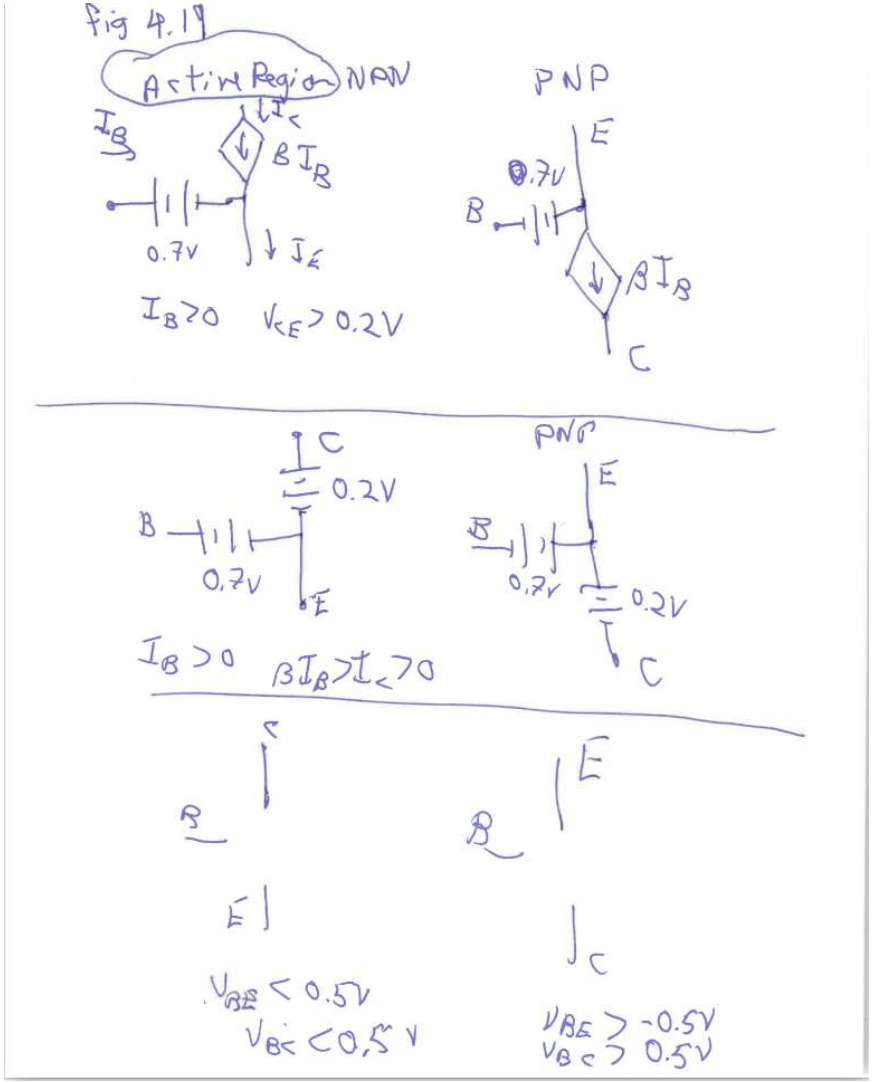
$$\frac{V_{CC} - 0.2\text{ V}}{R_C}$$

Edge of Saturation

$$I_{Beos} = \frac{I_{Csat}}{\beta}$$

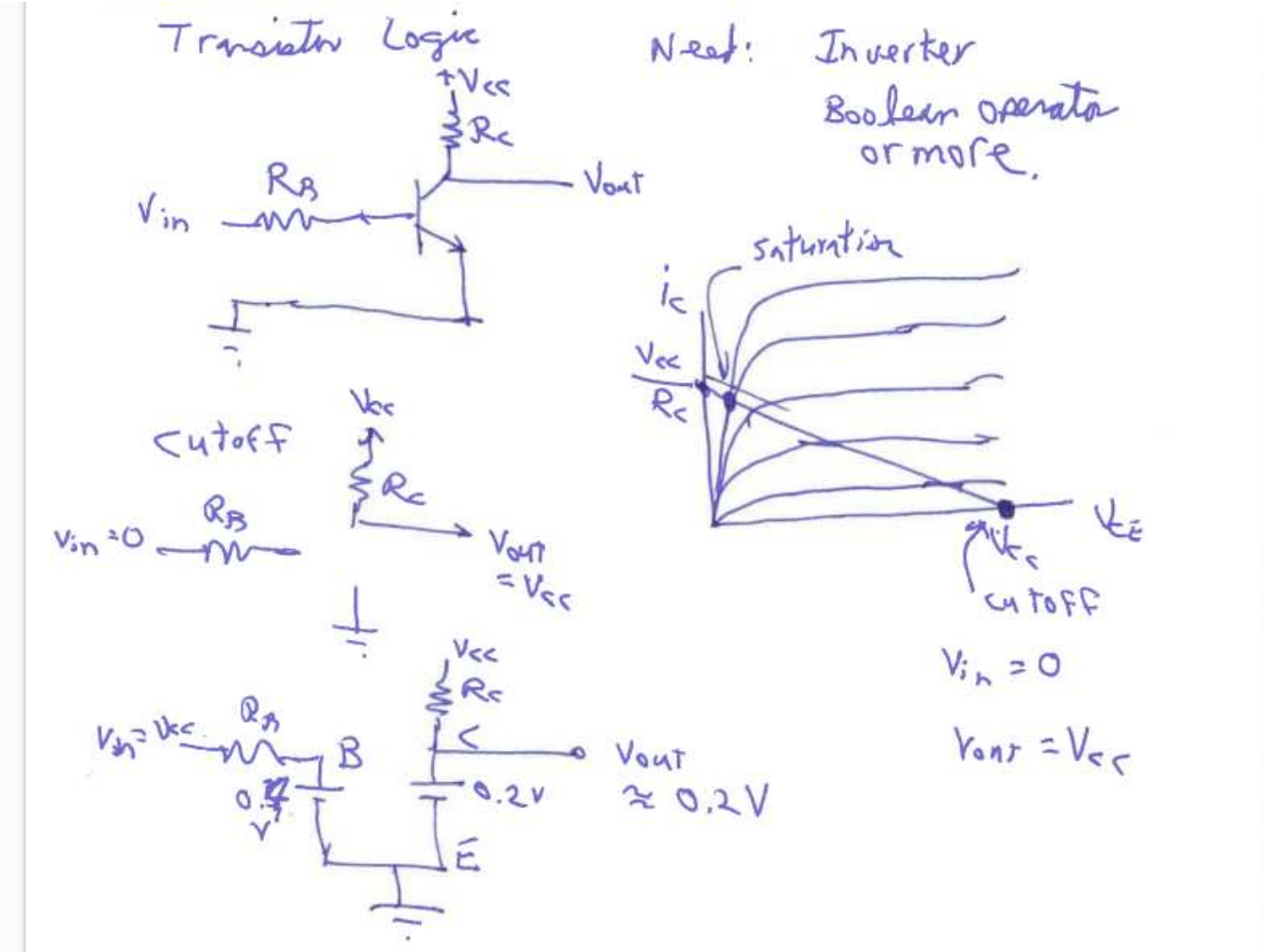


Pi Models in 3 Regions



- Try All Three
- Only One Will Work

Resistor-Transistor Logic



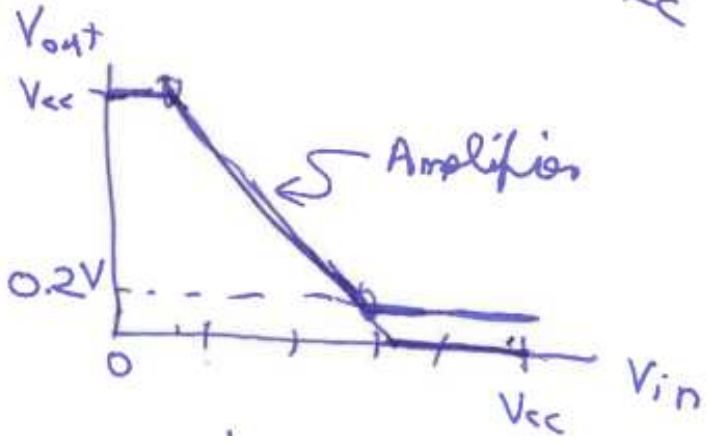
Logic Inverter

$V_{out} = 5\,V$

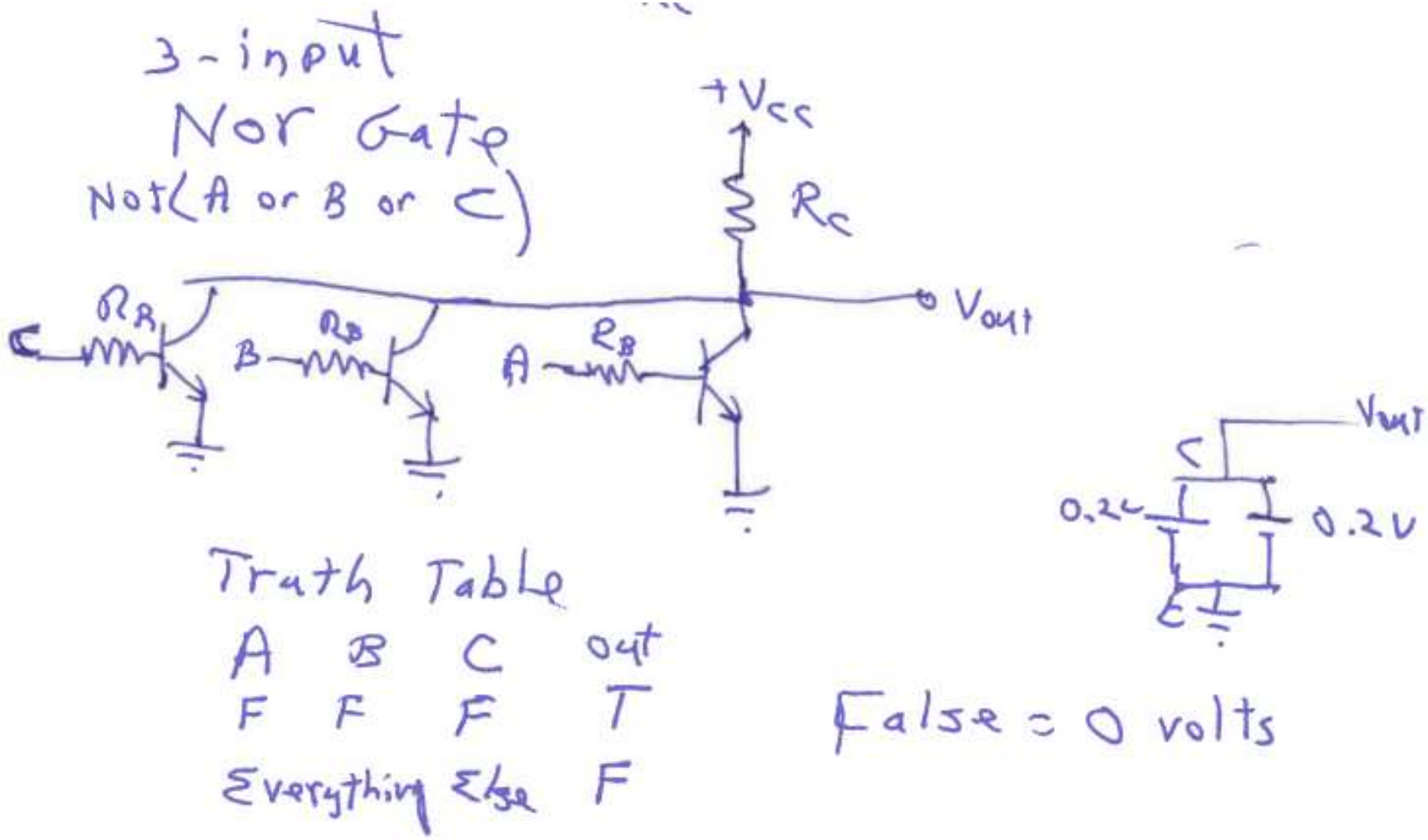
$P = \dfrac{V_{out}^2}{R_{load}} = \dfrac{25\,V^2}{R_{load}}$

$V_{out} = 0$

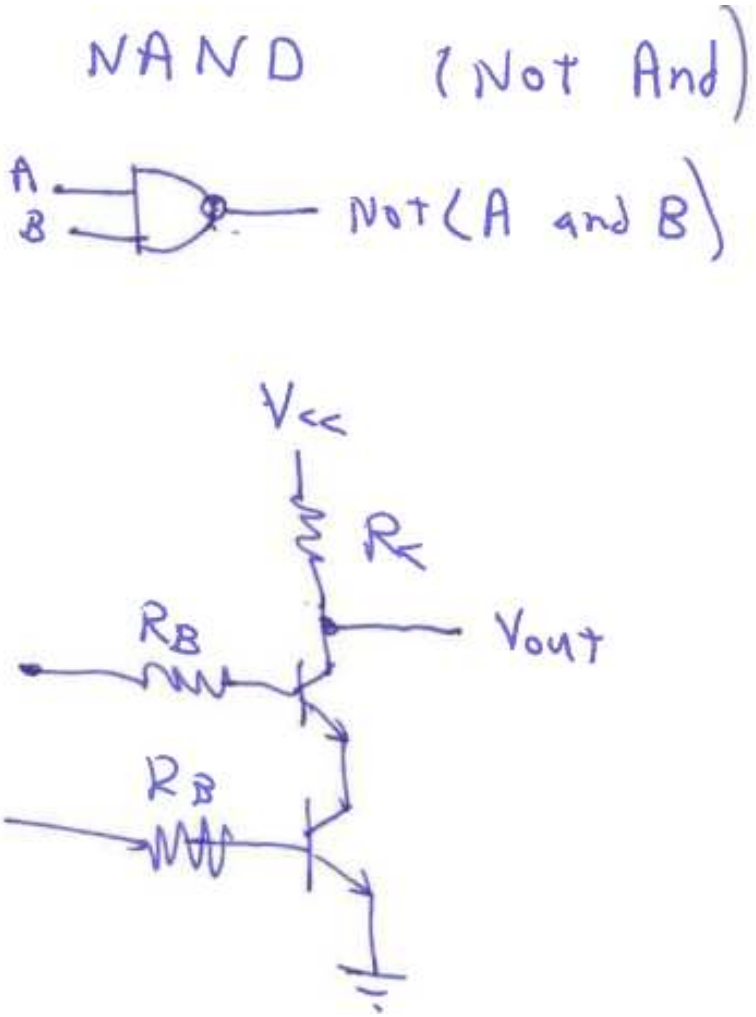
$P = \dfrac{V_{cc}^2}{R_c} = \dfrac{25\,V^2}{R_c}$



Logic NOR Gate



Logic NAND Gate



A	B	out
T	T	F
T	F	T
F	T	T
F	F	T

Issues to Consider

- Cascading
- Fanout
- Input Boundaries
- Output Boundaries