

Lab 1 Guideline

In this lab, we'll make ourselves familiar with Cadence and Hspice. And also, we will optimize the inverter, and study the cause and results of rising and falling delays in CMOS.

1. Report

Follow the student laboratory report format

(<http://www.ece.neu.edu/courses/eece4525/2017su/labrepform.pdf>).

Answer all the following questions (1~5). You can refer to our lab book(page 66).

2. Questions.

1. Why are 2 inverters (Xinv1 and Xinv2) needed before the CUT (Circuit Under Test – Xinv3) in the given example?
2. Why is the falling delay time faster than the rising delay time of your inverter?
3. How can you balance the inverter's rising and falling times?
4. 4. How can you get a faster inverter?
5. 5. How does the load capacitance (e.g., additional capacitance in the step 3) affect the delay time?

The following spice netlist has to be used to solve the above questions.

3. Circuit

<pre> ** Example : simulation of an inverter ** CMOS Inverter **----- ** Section 1: Environment ** Specify simulation environment **----- .Option post .LIB "cmos25_level49.lib" CMOS_MODELS **----- ** Section 2: Supply voltage ** Sepecify the supply voltage **----- vVDD VDD 0 2.5 vVSS VSS 0 0 **----- ** Section 3: Circuit netlist ** Netlist of an inverter **----- * circuit netlist Xinv1 TMP_IN TMP_1 VDD VSS invx Xinv2 TMP_1 IN VDD VSS invx Xinv3 IN OUT VDD VSS invx Cap OUT VSS 50fF </pre>	<pre> ***----- ***subcircuit (inverter) ***----- .Subckt invx KIN KOUT KVDD KVSS mp KVDD KIN KOUT KVDD cmosp l=0.25u w=4u mn KVSS KIN KOUT KVSS cmosn l=0.25u w=4u .ends **----- ** Section 4: Stimuli ** Sepecify the stimulus **----- vIN TMP_IN 0 pulse(0 2.5 0ps 400ps 400ps 5ns 10ns) **----- ** Section 5: Analysis ** Sepecify what type of analysis you want **----- .tran 1ps 30ns **----- ** Section 6: Results ** Sepecify what nodal value you are interested **----- .probe tran v(in) v(out) .end </pre>
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