LAB4. 4-Bit Ripple Carry Adder Design

In this lab, you will draw a 4-bit ripple carry adder (RCA) layout using Cadence (Composer). A schematic hierarchy of this design is shown in Figure 1. You'll design the RCA using Cadence.

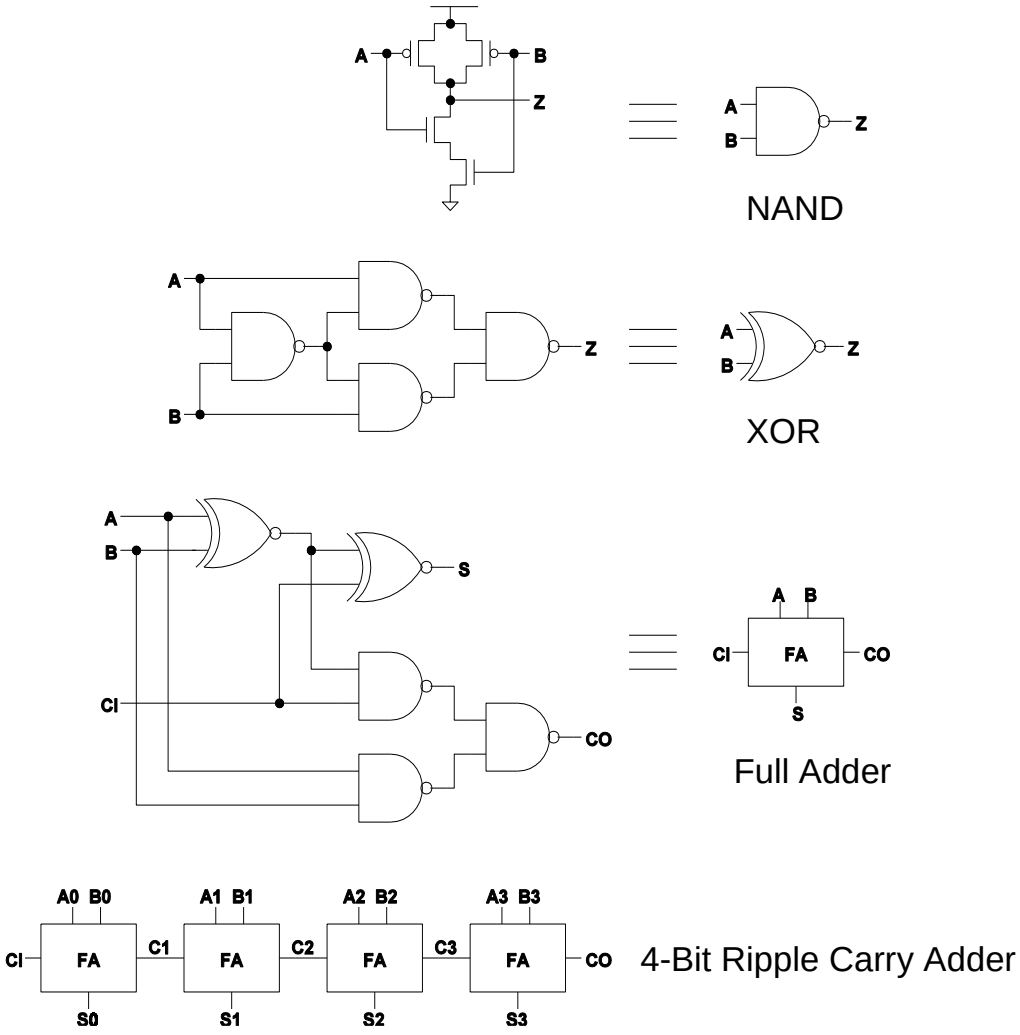


Figure1. 4-bit RCA schematic and symbol

Before designing the RCA, design a one-bit full adder (FA). Label the input data as A, B, and CI, and the output as S and CO. Use Composer cell hierarchy to design the FA. In order to simplify the layout, use three 2-input nand cells and two 2-input exclusive-or (XOR) cells as sub-cells in this lab. And XOR can be implemented using 4 nand cells as shown in Figure 1. The top-level parent cell, FA, will contain five children cells, nand_0, nand_1, nand_2, xor_0, and xor_1. When using cell hierarchy in Composer, make sure that the labels, **A, B, CI, S,** and **CO**, are placed on a square of paint contained in the top-level parent cell, **FA**. Then, using four FA cells, design a 4-bit RCA. Make sure that the labels of this RCA are A0~A3, B0~B3, CI, S0~S3, and CO.

Step 1.

1. Run virtuoso & under your working directory

2. Make a New Library (named "lab4)

Step 2. Design 2-input Nand gate

1. Make a new Cell under the lab4 library. (Cell Name : nand2, Tool : Composer-Schematic)

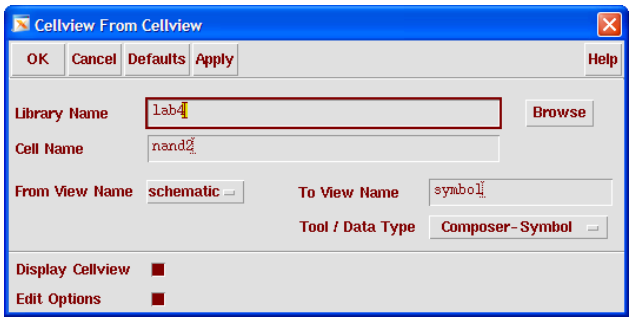
2. Draw 2-input nand circuit referred to Figure 1.

a) PMOS : W=2um, L=180nm
b) NMOS: W=1um, L=180nm

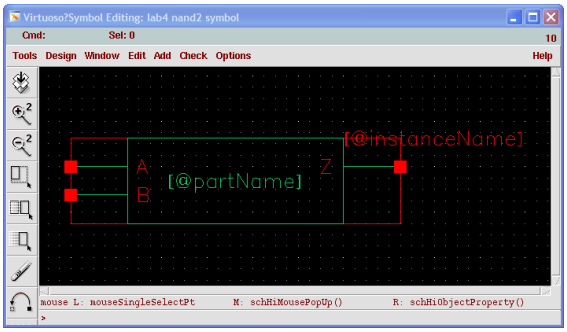
3. Save and Check the circuit (Select **Design->Save and Check**)

4. Create Symbol

a) Select **Design->Create Cellview->From Cellview**



b) Check the input names and output names in the symbol editor window



c) Select **Design->Save and Check**
d) close the symbol editor window

5. Check if the above symbol exists under “nand2” Cell in the Library Manager.

Step 3. Design 2-input Xor gate

1. Make a new Cell under the lab4 library. (Cell Name : xor2, Tool : Composer-Schematic)

2. Draw 2-input Xor circuit referred to Figure 1.

a) Select **ADD->Instance**
b) Choose “lab4” Library in the Component Browser
c) Choose “nand2” in the Component Browser
d) Place the cell on your schematic editor.

3. Save and Check the circuit (Select **Design->Save and Check**)

4. Create Symbol (same as the Step 2)

Step 4. Design Full Adder

1. Make a new Cell under the lab4 library. (Cell Name : FA, Tool : Composer-Schematic)

2. Draw Full Adder circuit referred to Figure 1. (same as the Step3)
- nand2 and xor cell are needed.

3. Save and Check the circuit (Select **Design->Save and Check**)

4. Create Symbol (same as the Step 2)

5. In the schematic editor window, Run **Analog Environment**.

6. Verify your FA design using ADE L

Step 5. Design 4-bit Ripple Carry Adder

1. Make a new Cell under the lab4 library. (Cell Name : 4RCA, Tool : Composer-Schematic)

2. Draw 4-bit RCA circuit referred to Figure 1. (same as the Step3)
- FA cell are needed.

3. Save and Check the circuit (Select **Design->Save and Check**)

4. In the schematic editor window, Run **Analog Environment**.

5. Verify your FA design using ADE L

Lab report guideline:

1. Write down the truth table of XOR2 gate, NAND2 gate, and NOR2 gate.

2. Explain about ripple-carry adder and carry-lookahead adder.
   (Include the advantages and disadvantages over each one.)