LAB 5. 4-Bit Ripple Carry Adder Design II

In this lab, you will draw another 4-bit ripple carry adder (RCA) layout using the full adder (FA) as shown in Fig.1. First, draw the stick diagram for this FA, and then create the cell using Cadence. Then, using four FA cells, design a 4-bit RCA. Make sure that the labels of this RCA are A0~A3, B0~B3, CI, S0~S3, and CO.

After parameter extraction, you'll simulate the netlist using Hspice as in Lab3. Before designing the RCA, design a one-bit full adder (FA) as one circuit. Label the input data as A, B, and CI, and the output as S and CO. When using cell hierarchy in Cadence, make sure that the labels, **A, B, CI, S,** and **CO**, are placed on a square of paint contained in the top-level parent cell, **FA**. Then, using four FA cells, design a 4-bit RCA. Make sure that the labels of this RCA are A0~A3, B0~B3, CI, S0~S3, and CO.

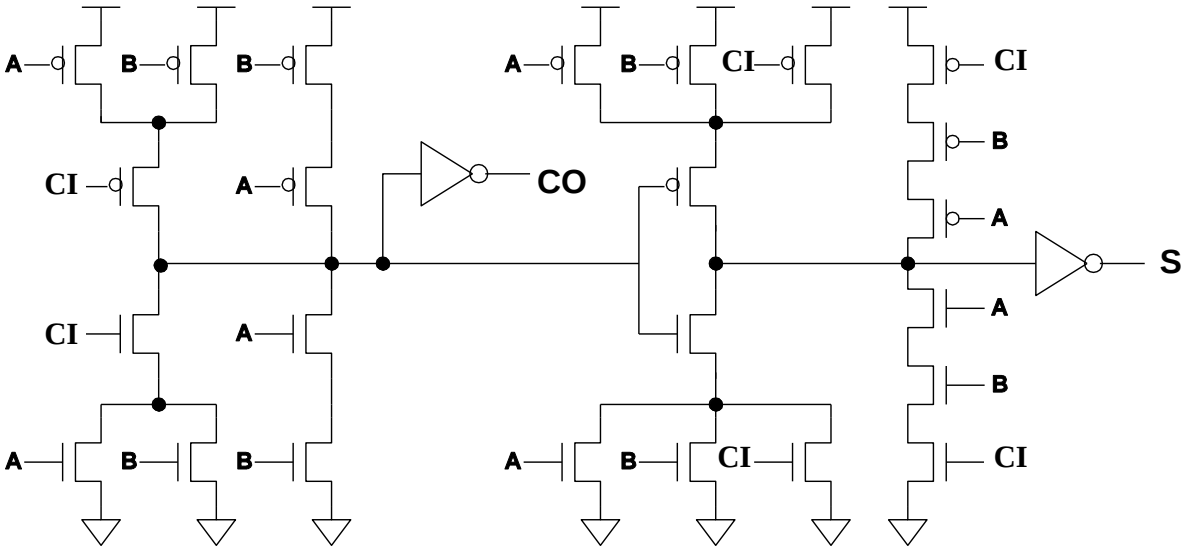

Fig.1 Full Adder Schematic

Step 1.

1. Run virtuoso & under your working directory

2. Make a New Library (named “lab5”)

Step 2. Design Full Adder

1. Make a new Cell under the lab5 library. (Cell Name : FA, Tool : Composer-Schematic)

2. Draw Full Adder circuit referred to Figure 1.

a) PMOS : W=2um, L=180nm
b) NMOS: W=1um, L=180nm
you should decide it as same size with lab4.

3. Save and Check the circuit (Select **Design->Save and Check**)

4. Create Symbol

a) Select **Design->Create Cellview->From Cellview**
b) Check the input names and output names in the symbol editor window
c) Select **Design->Save and Check**
d) close the symbol editor window

5. In the schematic editor window, Run **Analog Environment**.

6. Verify your simulation result.

Step 4. Design 4-bit Ripple Carry Adder

1. Make a new Cell under the lab4 library. (Cell Name: 4RCA, Tool : Composer-Schematic)

2. Draw 4-bit RCA circuit referred to Figure 1 of the last lab(lab 4).

3. Save and Check the circuit (Select **Design->Save and Check**)

4. In the schematic editor window, Run **Analog Environment**.

5. Verify your simulation result.

Lab Question:

1. Illustrate the difference of the design methods used in lab4 and lab5. Compare the area and speed of both design, you can estimate the area by counting the number of transistors.