

LAB6. Various XOR Implementations

Pre-Lab: Dynamic Logic and Transmission Gate

The dynamic logic uses a sequence of precharge and conditional evaluation phases to realize complex logic functions with less transistors. Consider Fig.1(a). When CLK is low (0), the output node Z is precharged to VDD by a PMOS transistor. During that time, the NMOS connected to GND is off. Thus, no DC current flows regardless of the values of the input signals. On the other hand, when CLK is high (1), the precharge PMOS is OFF, and the evaluation NMOS is turned ON. Depending on the values of the inputs and the composition of the pull-down network, a conditional path between Z and GND is created. If such a path exists, the output Z is discharged, and a low output signal is obtained. If not, the precharged value remains on the output node. Several important features of the dynamic gate are following:

1. The logic function is implemented by the NMOS pull-down network.
2. The number of transistors for dynamic logic is $N+2$ versus $2N$ for static CMOS.
3. Due to the reduced number of transistors per gate and the single transistors load per fan-in, the load capacitance for this gate is substantially lower than for static CMOS. This results in faster switching-speeds.
4. It consumes only dynamic power.

Another promising approach to implementing complex logic is to realize it as a logical network of transmission gates as shown in Fig.1(b). The Transmission Gate (TG) approach has the advantage of being simple and fast. Complex CMOS combinational logic is implemented with a minimal number of transistors. This reduces the parasitic capacitances and results in a faster circuit. This gate is composed of an NMOS transistor and a PMOS device in a parallel arrangement. The TG acts as a bi-directional switch controlled by the gate signals; B and BB for Fig.1(b). When $B = 0$, and $BB = 1$, both transistors in the upper TG are on, allowing the signal to

pass through the gate. On the other hand, the transistors in the lower TG are OFF. When $B = 1$, and $BB = 0$, the upper TG is in cutoff and the lower TG is ON.

Design of XOR using Dynamic logic and Transmission Gate

You made a static XOR gate in Lab3. In this lab, you will design two different XOR layouts using Cadence as shown in Fig 1. And after parameter extraction, you'll simulate the netlist using AimSpice. For simplicity, assume the complimentary signals are given as shown in Fig.1. Make sure that the labels are, **A**, **B**, **AB**, **BB**, **CLK** and **Z**.

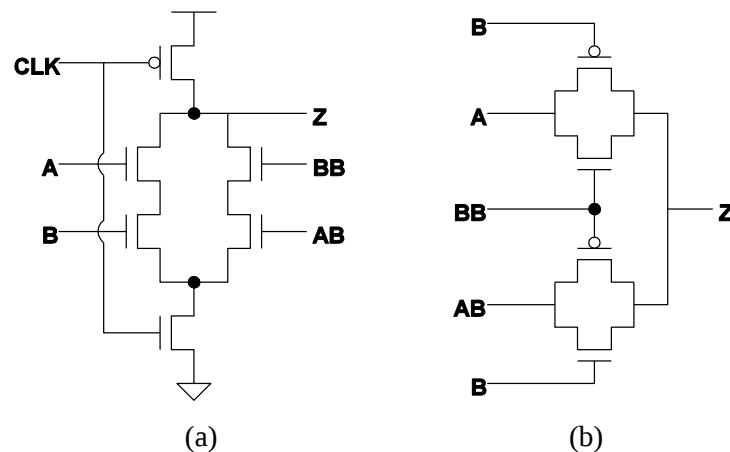


Figure 1 XOR schematics: Dynamic vs. Transmission gate

In Fig.1, the first XOR is implemented using the dynamic circuit scheme while the other consists of two identical transmission gates. The first one will be drawn as one level. Fig.2 shows the stick diagram for the dynamic circuit. The second XOR implementation will be designed hierarchically using the transmission gate implemented in Lab3. The procedures for drawing and simulating circuits are identical to the previous labs. You can use the input deck of SPICE from Lab2.

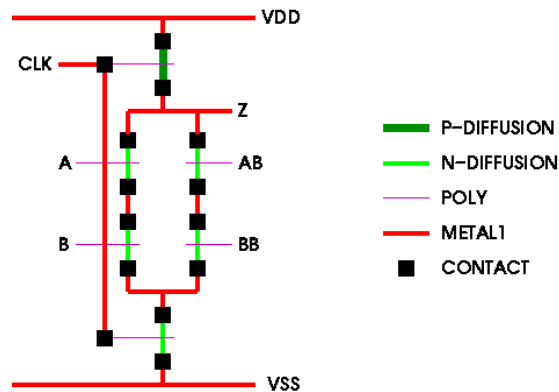


Fig.2 A stick diagram for dynamic XOR

Step 1.

1. Run virtuoso & under your working directory
2. Make a New Library (named “lab6”)

Step 2. Design Dynamic XOR

1. Make a new Cell under the lab6 library. (Cell Name : dynamic, Tool : Composer-Schematic)
2. Draw Dynamic XOR circuit referred to Fig.L5.1.
 - a) PMOS : W=2um, L=180nm
 - b) NMOS: W=1um, L=180nm
3. Save and Check the circuit (Select **Design->Save and Check**)
4. In the schematic editor window, Run **Analog Environment**.
5. Verify your simulation result.

Step 3. Design Transmission XOR

1. Make a new Cell under the lab6 library.
(Cell Name : transmission, Tool : Composer-Schematic)
2. Draw Transmission XOR circuit referred to Fig.L5.1.
 - a) PMOS : $W=2\mu m$, $L=180nm$
 - b) NMOS: $W=1\mu m$, $L=180nm$
3. Repeat step 3~5 in Step 3.

Lab Questions:

1. Compare dynamic gate, static gate and transmission gate.
(It is better use a table to point out the difference, pro. and con. of each implementation)
2. Draw a stick diagram of Transmission XOR. (Refer to Fig.2)