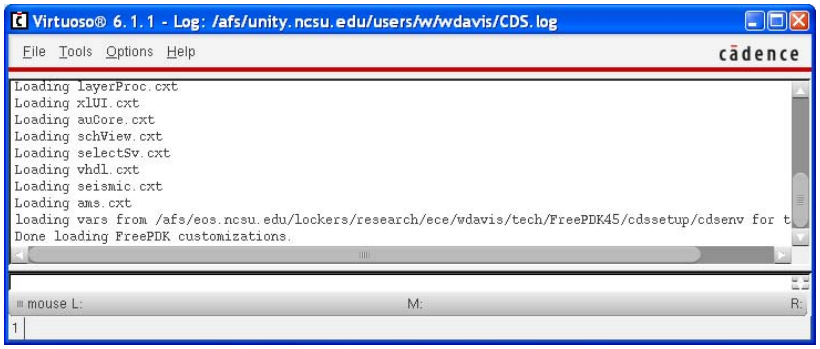
Tutorial:Layout Tutorial

In this tutorial you will go through creating an Inverter layout while performing design-rule checks (DRC). This tutorial assumes that you have logged in to an COE or ECE machine and are familiar with basic UNIX commands.

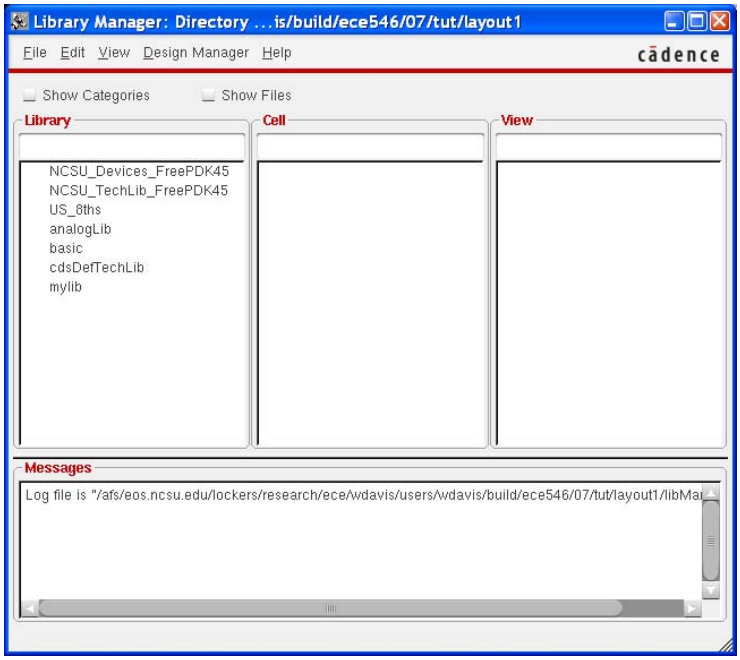
Create Aliases to Setup Your Environment

```
% tcsh
%source cadence_setup.cshrc
% source setup_hspice_new.csh
% icfb &
```

The first window that appears is called the CIW (Command Interpreter Window).

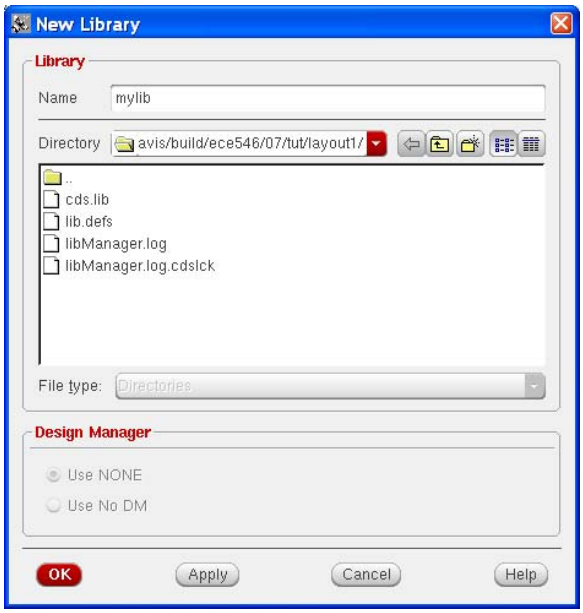


Open the library manager by selecting **Tools->LibraryManager**. This window allows you to browse the available libraries and create your own.



Create New Library

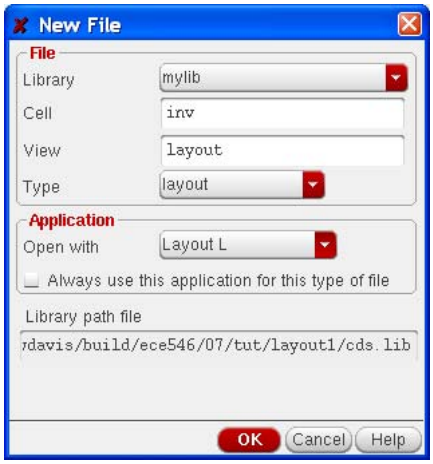
In the Library Manager, create new library called **mylib**. Select **File->New->Library**. This will open new dialog window, in which you need to enter the name and directory for your library. By default, the library will be created in the current directory. After you fill out the form, it should look something like this:



Click OK. Next, you will see a window asking you what technology you would like to attach to this library. Select "Attach to an existing technology library" and click OK. In the next window, select "NCSU_TechLib_FreePDK45". You should see the library "mylib" appear in the Library Manager.

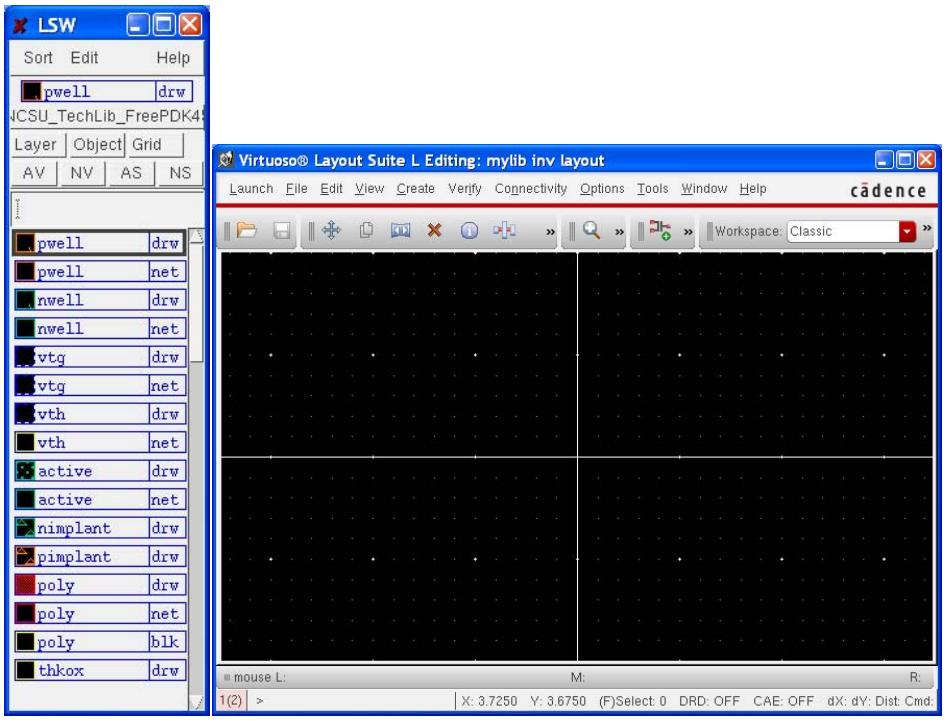
Create New Layout View

Next, select the library you just created in the Library Manager and select **File->New->Cell View...**. We will create a layout view of an inverter cell. Simply type in "inv" under cell-name and "layout" under view. Click OK or hit "Enter". Note that the "Application" is automatically set to "Layout L", the layout editor.



Alternatively, you can select the "Layout L" tool, instead of typing out the view name. This will automatically set the view name to "layout".

Click Ok. You may see a warning about upgrading the license. Simply click Ok to ignore this warning. After you hit "OK", the Virtuoso screen will appear as shown below. In addition, the LSW window (Layer Selection Window), which shows various mask layers, will automatically pop up.

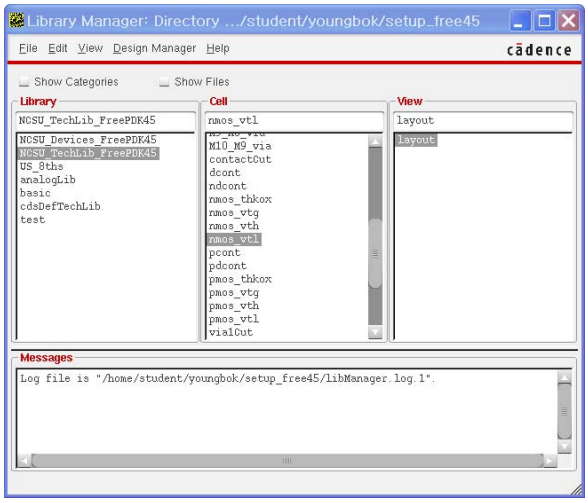


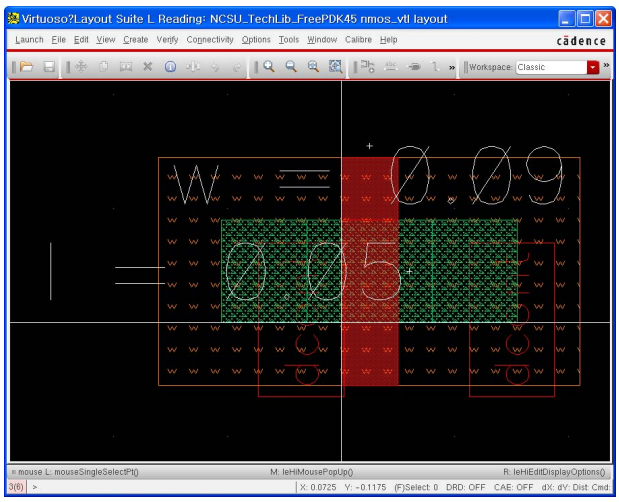
Now you are ready to draw objects in the Virtuoso window. In this section you learn to place copies of other cells: **pmos_vtl** and **nmos_vtl**.

Select NCSU_TechLib_FreePDK45(Library) -> nmos_vtl(Cell) -> layout (View). The You will see the nmos_vtl layout cell. Select whole cell by dragging whole area and copy (press ‘C’ button and select selected are) . Place in the layout editor. It’s channel length is 50nm and width is 90nm. X and Y axis scale unit is µm.

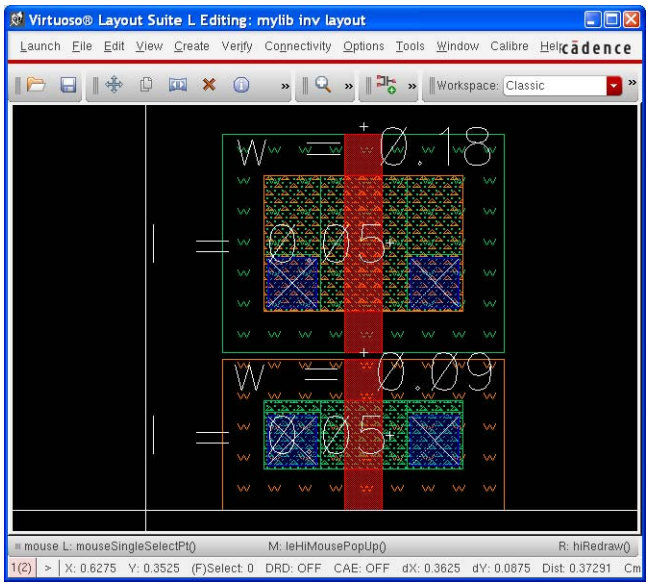
This cell is smallest cell in this library. You can adjust the size of transistor by streching (Edit-> Stretch or pressing ‘s’) and editing using edit functions(move, copy, stretch, delete)

It is composed of following layers: **pwell**, **active**, **nimplant**, **poly**, **metal1**, **contact**, and **text**.





Draw NMOS and PMOS transistor. Finally the transistor looks like this.



you should be able to figure out that the NMOS uses the following layers: **pwell**, **active**, **nimplant**, **poly**, **metal1**, **contact**, and **text**. The PMOS is like it, except that it uses layers **pimplant** and **nwell** instead of pwell and nimplant.

You could paint these shapes manually in the current cell-view

Note also the letters "drw", "net", and "pin" next to each entry in the LSW. These are the *purposes* of a shape. The purpose is used to indicate special functionality of a shape. We will discuss these more in later tutorials. For now, remember that "drawing" is the purpose that indicates that a shape will appear in the mask layout. You will sometimes see "drawing" abbreviated as "drw", and sometimes "dg".

Selecting and Moving Layout

By default, if you simply drag out a region while holding down the left mouse button (Button-1), whatever is within the box will be selected and highlighted in white.

> Drag a box over the nmos you just instantiated. When you release the mouse button, whatever is "selected", in this case the nmos cell, will be highlighted.

Once you have selected an object (that is, an instance or a shape) you can do lots of things with it.

> For example you can move it by typing the m hot-key. You can move layout up/down/left/right one grid at a time by clicking at the selection and moving the mouse. Try it.

You can also select objects by clicking on them.

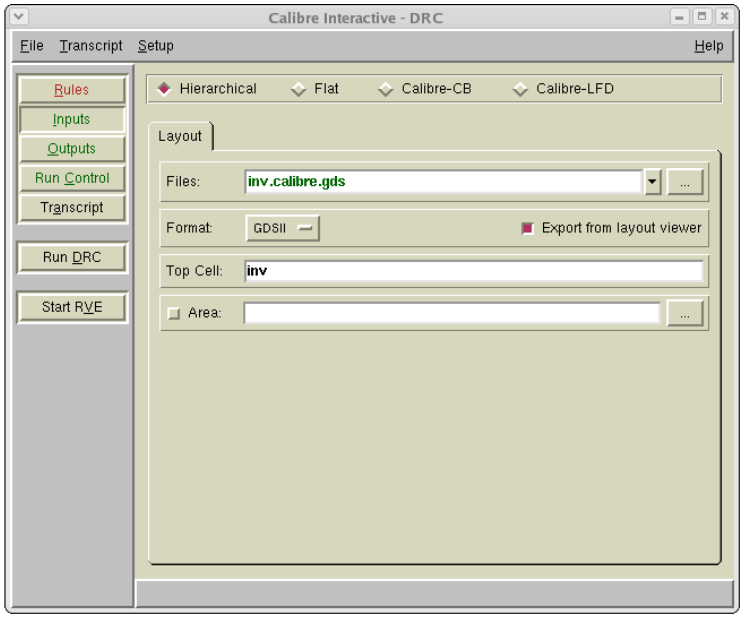
> Clicking the left mouse button once on an instance or shape selects it.

If you didn't place your NMOS and PMOS cells exactly as illustrated above, try moving them now until they are.

DRC

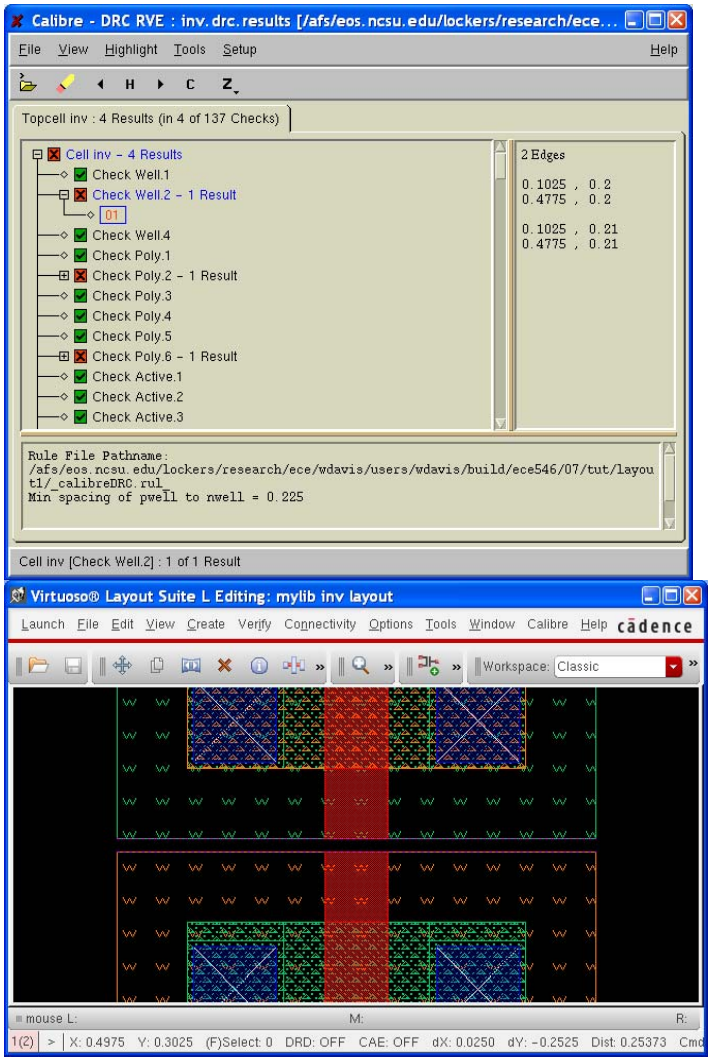
Refer to **Design Rules** in http://www.eda.ncsu.edu/wiki/FreePDK45:Contents

To perform a Design Rule Check (DRC), choose **Calibre->Run DRC…**. The DRC form appears, as shown below. Then click "Run DRC". If you do not see the window appear, or if you get an error, then it's possible that you didn't type "add calibre" as instructed above. You will need to exit Virtoso, log out, and log back in, setting up your environment in the correct order.



Viewing DRC Errors

You can learn about the errors by clicking on the rule in the Results Viewing Environment (RVE) window that pops up after DRC is complete. Click on an error and hit "shift-H" to highlight the error in the layout viewer as shown. **NOTE:** In order for Shift-H to work as described here, in the DRC RVE window, choose **Setup->Options...**, select "Zoom cell view to highlights by 0.7", and click "OK". You should only need to do this once. Your choice will be saved for the next time that you log in.



In this particular case, the transistor wells are too close together. Fix this error by moving up the pmos. It's good practice to space the NMOS and PMOS transistors by the smallest amount allowed in order to make the layout as dense as possible. You can draw temporary rulers by hitting "k" and dragging a ruler. You can clear the rulers by hitting "Shift-K". These rulers can help you to draw dense layout much faster than you would by constantly running DRC.

Move the PMOS and re-verify until there are no DRC errors. You can re-run DRC by simply clicking on "Run DRC" in the DRC Form window. You will be asked if you want to overwrite the layout file (inv.calibre.gds). Click Ok. Virtuoso is exporting a file to Calibre every time you run DRC. Note that you will need to save your layout each time you run DRC. Otherwise, the check will run on the last layout you saved.

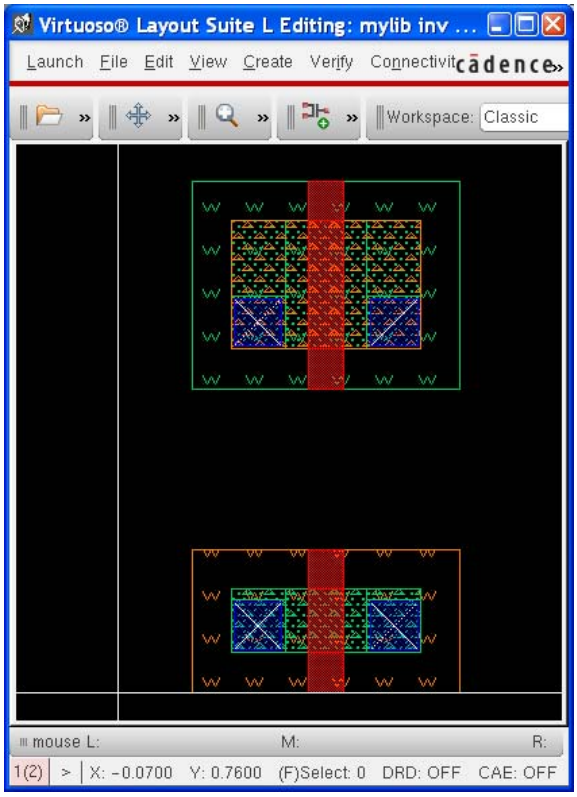
Keep modifying your layout until there are no errors. You will know that there are no errors when there are no red boxes in the RVE. Alternatively, you can look in the file **inv.drc.summary**. When the layout is "DRC Clean", the last line of this file should read "TOTAL DRC Results Generated: 0".

You will notice that there is one rule that you cannot satisfy by moving around the P-Cells (rule Metal.4, which requires the minimum area of metal1 to be 0.00845). We will fix this error later on.

To learn more about each design-rule, follow the links the the "Tool Tips" section of the course web-page, under "Design Rules".

If you simply want to remove the error markers, choose **Highlight->Clear Highlights…** in the RVE.

Once you are done, your layout should look like the one below:



Painting

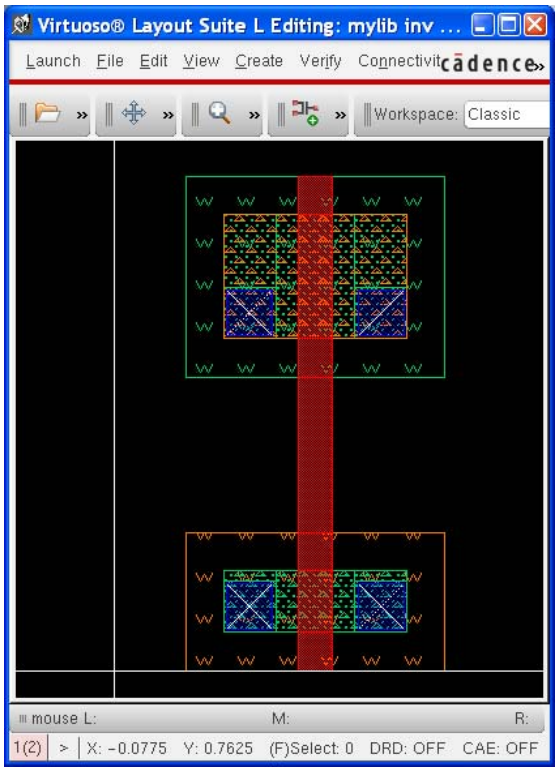
We are now going to "paint" a piece of poly to connect the pmos and nmos devices together. We do this by creating a shape, in this case, a rectangle.

Select the poly layer in the LSW by left-clicking on it.

Hit “r” to draw a rectangle and draw the poly area.

Hit “Escape” to stop drawing rectangles.

Your layout should look like this:



Another type of shape that you can create is a paths. Connect the drain nodes of the NMOS and PMOS transistor as follows:

Select the metal1 layer in the LSW by left-clicking on it.

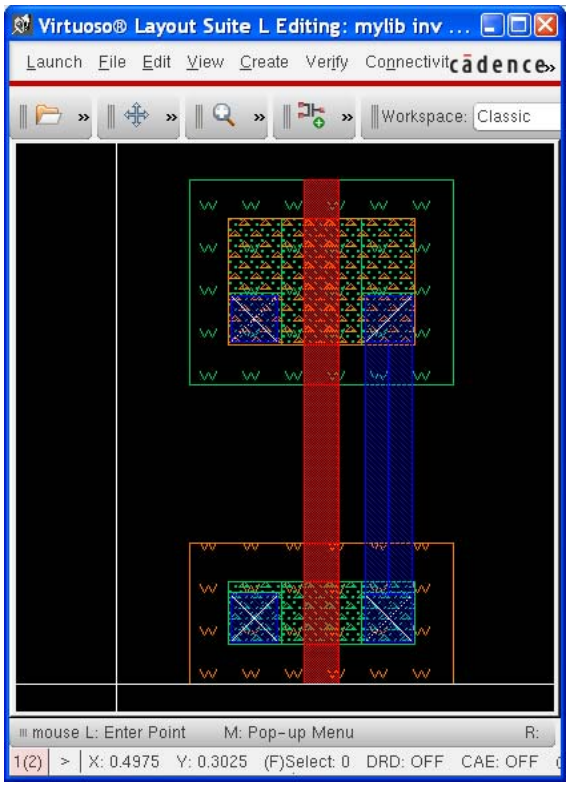
Hit “p” to create a path.

Set the **Width** to **0.065** in the dialog box. (If you do not see the dialog box, then you can adjust the width after you draw the path by selecting it and hitting "q" to edit the properties. Set the width to 0.065 in the properties.)

Click on one end of the path, and double click to end the path.

Hit “Escape” to stop drawing paths.

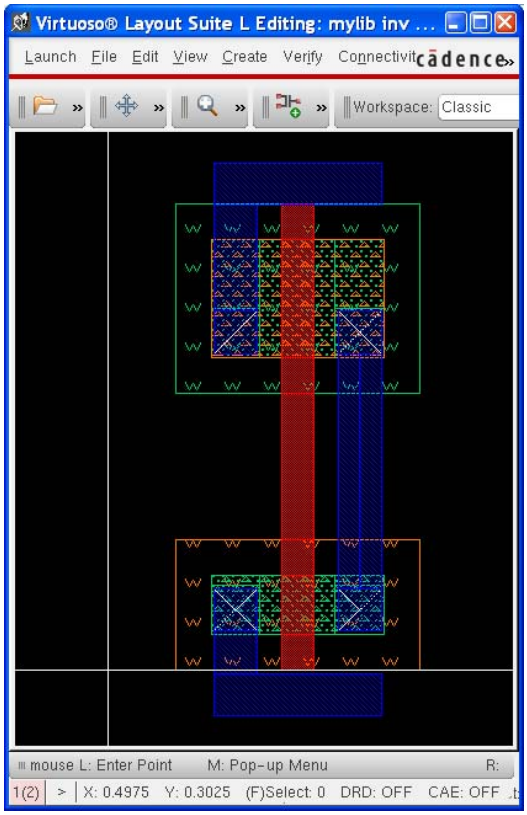
Your layout should look like this:



If you don't like the way your drawing turned out, you can select a shape and delete it with the delete key, or you can hit "s" (for stretch), and click on one of the sides of a path or rectangle to stretch it into the position that you like.

Also, you may want to run DRC checks periodically to make sure you're making progress in good direction. It's also a good idea to save occasionally, by selecting **File->Save**.

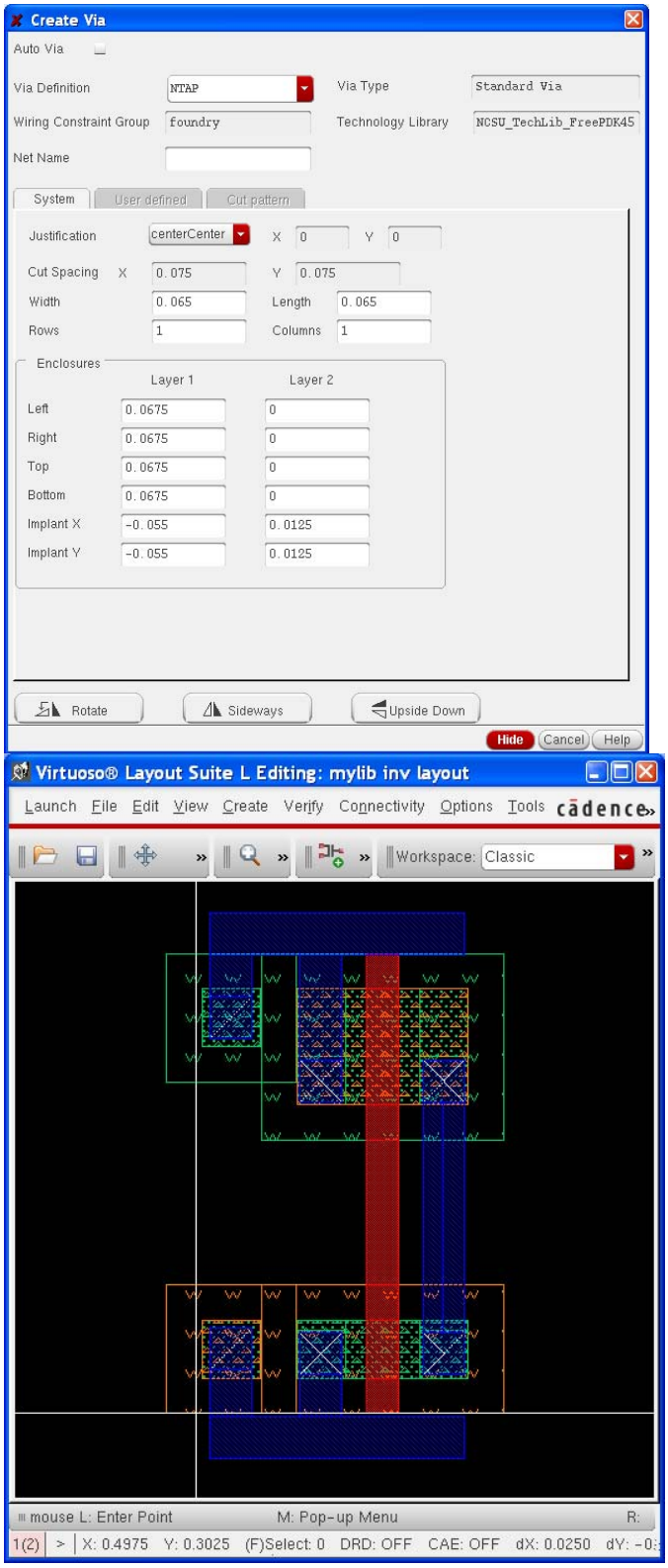
Next, create strips of metal1 for VDD and GND. We typically make these shapes as horizontal bars across the top and bottom, and therefore call them "supply rails". We then need to connect the rails to the source nodes of the transistors. Create these rails now, and make your design look like the one below. Again, try to make the layout as compact as possible and the supply rails as thin as possible, running DRC as often as needed to learn the design rules.



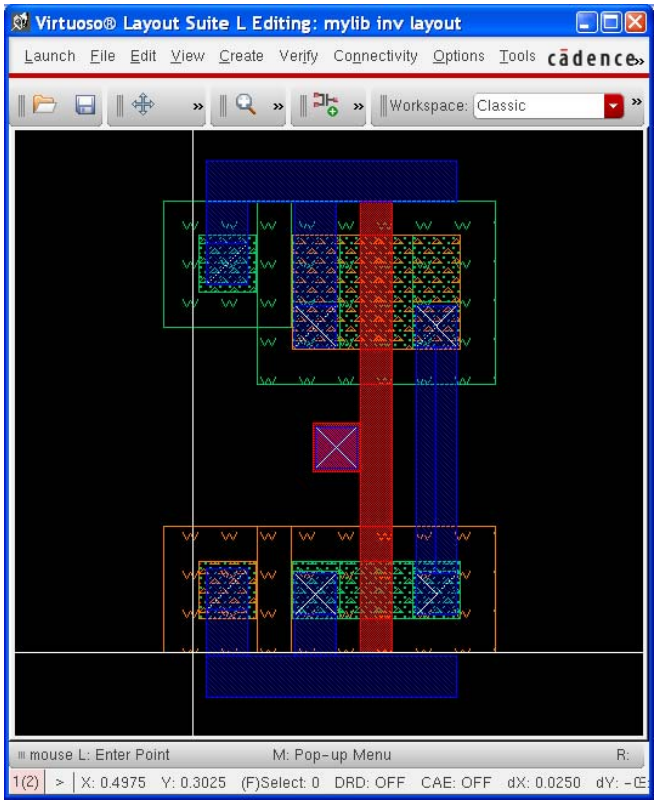
Add Vias

Next, we need to add contacts (also called vias) to wells, which serve as the bulk node of the transistors. Transistors do not have well-contacts by default, because they take up so much room. Several transistors can often share the same well-contact. In this class, we will require that every gate (that is, NOT, AND, OR, XOR, etc.) has at least one contact to each well.

Create an **NTAP** via by choosing **Create->Via...** or simply hitting "o". You should see the **Create Contact** pop-up appears, as shown below. Set the "Via Definition" to "NTAP". The other options should be set correcly by default. Place it as close as possible to the PMOS transistor. Likewise, create an instance of the **PTAP** cell and place it as close as possible to the NMOS transistor. Again, try to make the layout as dense as possible. We will need to connect these NTAP and PTAP cells to the power rails. Create **metal1** rectangles to connect these contacts to the rails. When you are done, your layout should look approximately like the one below.

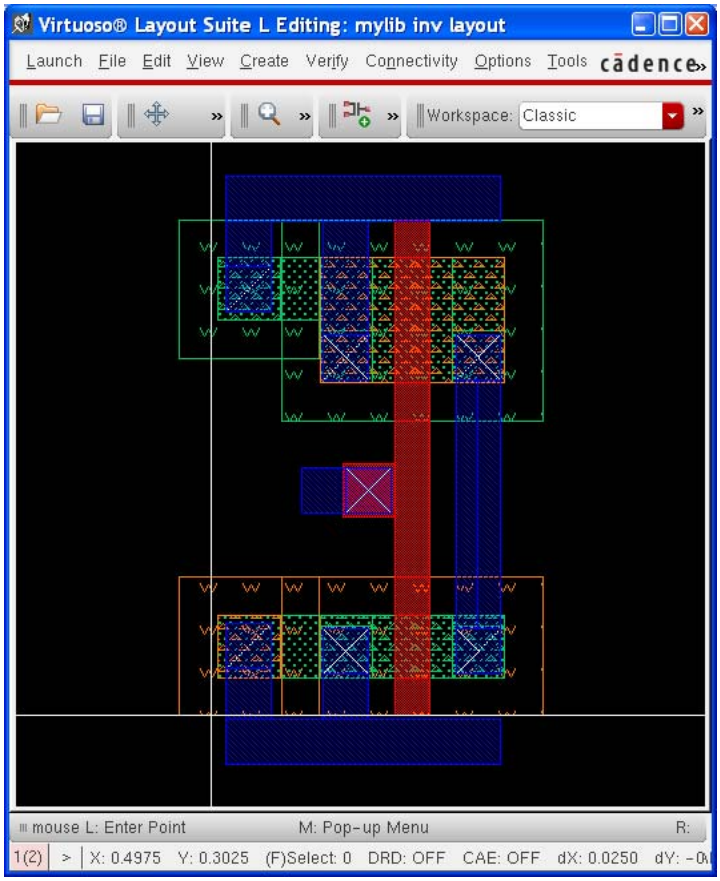


Next, add a gate-connection in *metal1*, with a metal1-to-poly *via*. Do this by choosing **Create->Via...** again and set the contact type to **M1_POLY**. Position the via as shown below.



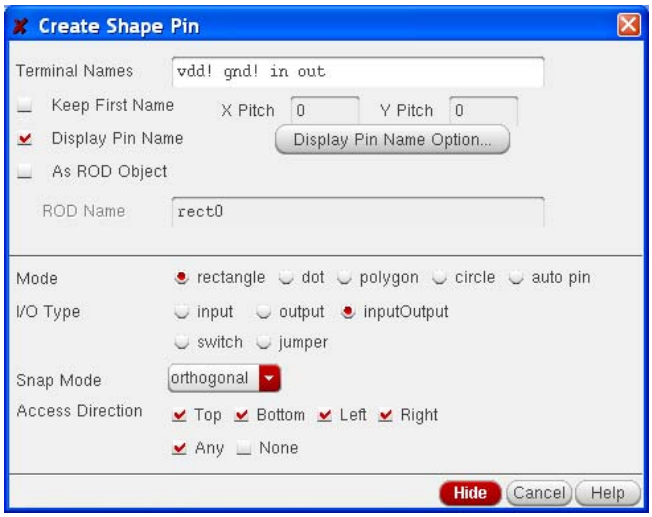
All of the **Metal.4** rules should be passing, now, except for the POLY via that we just created. To fix this error, extend the **metal1** shape to the left of the contact by 65nm, as shown below. That will fix the error.

To finish our layout, we may also want to add some active shapes in between the **NTAP** contact and **pmos_vtl** P-Cell, as shown below. This will allow us to make a more compact layout than we would be able to make without these shapes. Do the same between the **PTAP** contact and **nmos_vtl** P-Cell.

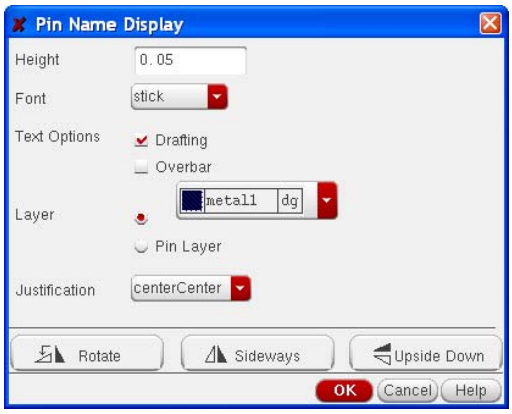


Create Pins

Lastly, we need to create pins so that the nodes in our layout have names that are human-readable. Create these pins by selecting **Create->Pin…**. You should see a dialog box appear, like the one below. Type the names vdd!, gnd!, in, and out in the "Terminal Names" text-box as shown below. Select "Display Pin Name". Leave all other options as they are.



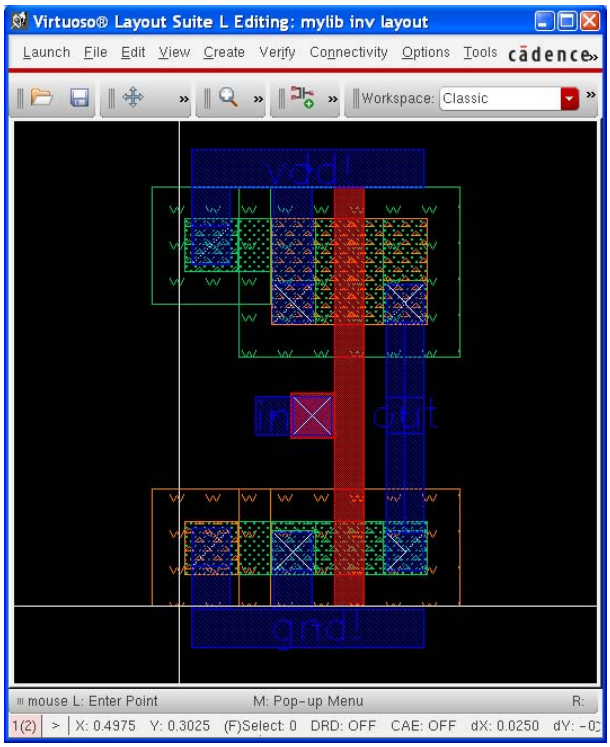
Next, click the “Display Pin Name Option…” button. You will see another dialog box appear:



Set the height to **0.05** um and the layer to **metal1-dg** (drawing). Click OK.

Next, click on the layout where you want each pin to be placed. You will need to click three times: twice to create a rectangle for the pin, and a third time to place the label. The shape of your rectangle doesn’t really matter, as long as it only covers area that is already covered by **metal1-dg**. When you are done, your layout should look like the one below.

Important Note: It is absolutely essential that you select the *Display Pin Name* box to create a label for each pin. The label must be in the same layer as the metal shape and must overlap the shape. This is necessary to pass Calibre LVS. This is not needed to finish Layout Tutorial #1; *however*, if you do not get into this habit now, then you will not be able to finish Layout Tutorials #2 and #3.



Congratulations! You have completed the tutorial. Save your design and select **File->Print** to print out a copy of your layout.

If you would like to learn more about the layout editor, you view the Cadence documentation. Start the documentation browser by typing

```
cdsdoc &
```