5. Hspice Netlist Extraction with Cadence

This tutorial explains how to extract a HSPICE netlist from your cellview from either the schematic or layout view.

- From Virtuoso (the layout view):
  a) Get the extracted view of the layout:
     1. Select Verify -> Extract.
     2. To extract parasitic capacitances for NCSU kit:
        1. Click the Set Switches button.
        2. Select `Extract_parasitic_caps` option. If you use capacitors or resistors, like in many analog applications, select `Extract_cap` and `Extract_resistor` also.
        3. In the CIW, type "NCSU_parasiticCapIgnoreThreshold=x" with x being the maximum value of capacitance to ignore (in Farads); 1e-18 is a typical value.
        4. Leave all other options as default.
        5. Click OK.
     3. Click OK.

  b) Start Analog Environment: Select Tools -> Analog Environment from the extracted window.
  c) Go to Netlist Extraction Procedure below.

- From Composer (the schematic view):
  a) All nodes must be named first - unless you are satisfied with automatically-generated names / node numbers. If they are not already named, left click each node (or wire connected to the node), then choose Edit -> Properties -> Object
  b) Start Analog Environment: Select Tools -> Analog Environment from the command (CIW) window.
  c) Go to Netlist Extraction Procedure below.

From Analog Environment: (Note: You must have the extracted view open in the background)

- Select Setup->Simulator/Directory/Host.
  a) Select the hspiceS simulator.
  b) Set your project directory. This will be where all your files will be created.

- Select Setup->Design
  a) Library name: (your library name)
  b) Cell Name: (your cell name)
  c) View Name: Extracted OR Schematic, depending on whether you started with layout or schematics
  d) Open Mode: Read
  Click OK to close the window.
- Select Setup->Environment.
  a) Insert "extracted" before "hspiceS" on the Switch View List if you started with layout; if you started with schematic, insert "schematic" instead if not already there, but it should be already there.
  b) Insert "ivpcell" before "hspiceS" on the Stop View List.
  c) Select the Include File Syntax to be hspice.
- Create Netlist.
  a) Select Simulation -> Netlist -> Create Final.
  c) Save the file displayed. This is the HSPICE netlist of your design.
    - If your circuit is very large, you may get OUT OF MEMORY errors. If this is the case, add the following three lines to your ~/.cdsenv file:

```
cdsSpice.init    languageSize    int    500
spectreS.init    languageSize    int    500
hspiceS.init     languageSize    int    500
```

- Exit Analog Environment: Select Session -> Quit.
- When asked if you wish to save current state, click No.

Special Note about Pin Names:If you have defined your pin names to have more than 16 characters, this exceeds the HSPICE label limit. In your extracted netlist, that node will be assigned to a number instead.

- NOTE: When using both switch-level and gate-level logic in a schematic
  1. Extract standard cells corresponding to the gates in your schematic

     a) Open the extracted view of a standard cell in Cadence Virtuoso.
     b) Follow instructions for extraction from layout given in the Netlist Extraction Procedure below. The HSPICE netlist is the subcircuit definition of the corresponding gate. (Ex: wand2_2.sp)

  2. Extract schematic for Netlist using instructions given in the Netlist Extraction Procedure below.
  3. Include the subcircuit definition in the top-level circuit HSPICE file using a .include statement. (Ex: ?.include ?./wand2_2.sp??)