

2. Schematic Entry with Composer

2-1 Creating the Schematic

(1) Creating a library and a schematic cell view

At first a new library that will contain the data for the implemented cell is created. From the menu bar of the Library Manager select

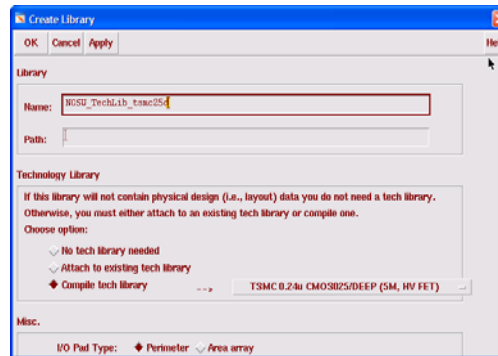
*In Library Manager, Click **File - New - Library***

In the Name field, enter “ **NCSU_TechLib_tsmc25d**”

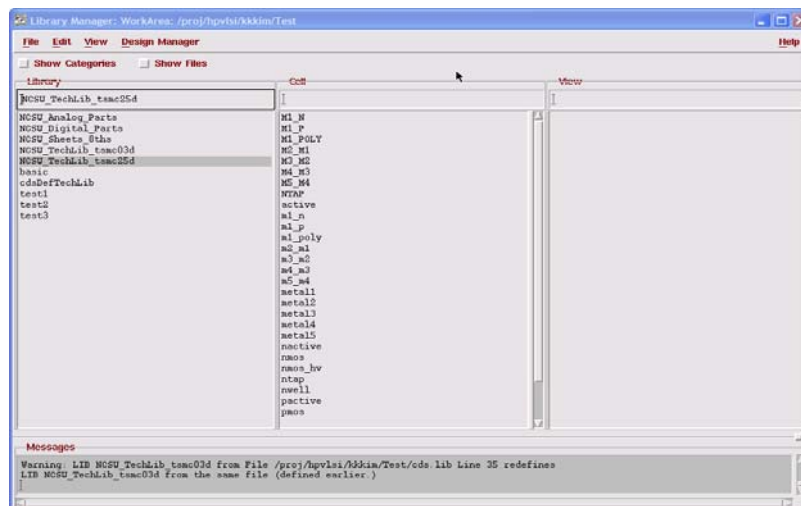
In the Technology Library box, select

Compile tech library -> TSMC 0.24u

Press OK.

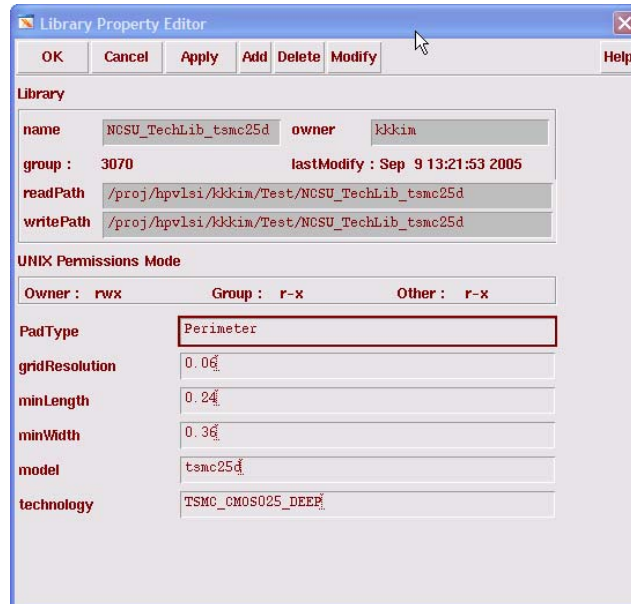


Then the Library Manager will refresh as follows:



Select **NCSU_TechLib_tsmc25d**, and *In Library Manager, Click **Edit - Properties***

In the model field, enter **tsmc25d**, and click **OK**.



(2) Creating working library and a schematic cell view

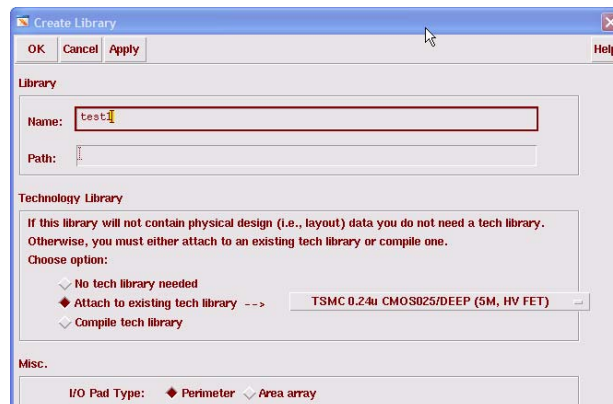
*In Library Manager, Click **File - New - Library***

In the Name field, enter “**test**”

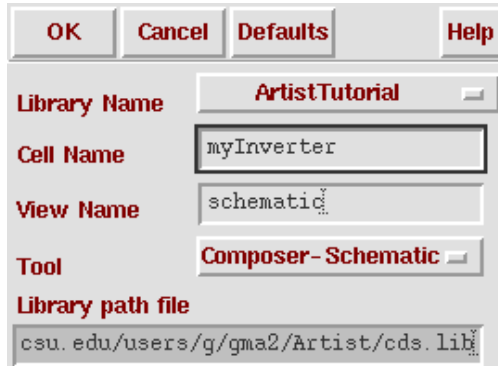
In the Technology Library box, select

Attach to existing tech library -> TSMC 0.24u

Press OK.



In **Library Manager**, select **ArtistTutorial**
From the Menu Bar, select **File -> New -> CellView**
Fill the Form as follows, then click **OK**



OK Cancel Defaults Help

Library Name ArtistTutorial

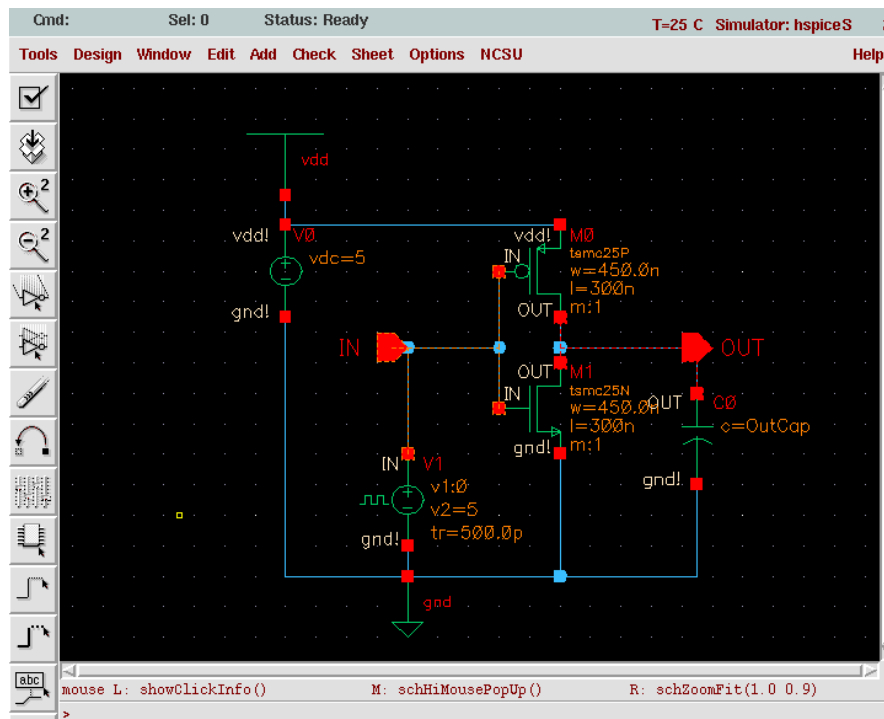
Cell Name myInverter

View Name schematic

Tool Composer-Schematic

Library path file csu.edu/users/g/gma2/Artist/cds.lib

A blank Schematic window will then appear.
We need to generate a schematic as shown below:

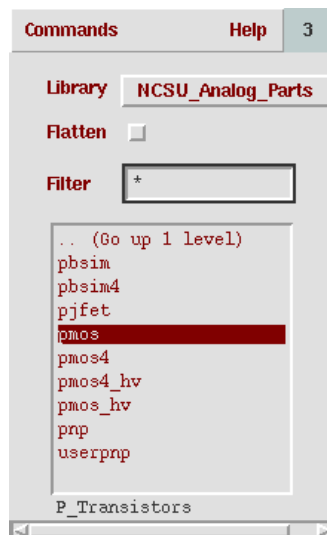


Drawing the schematic

To generate a schematic like this, you will need to go through the following steps:

From the Schematic Window menu, select Add -> instance (shortcut <i>)

The Component Browser, will then pop up.



In the **Library** field, select **NCSU_Analog_Parts**

We will place the following instances in the **Schematic Window** from the **NCSU_Analog_Parts** library as instructed below:

N_Transistor : nmos

P_Transistor : pmos

Supply_Nets : vdd , gnd

Voltage_Sources : vdc, vpulse

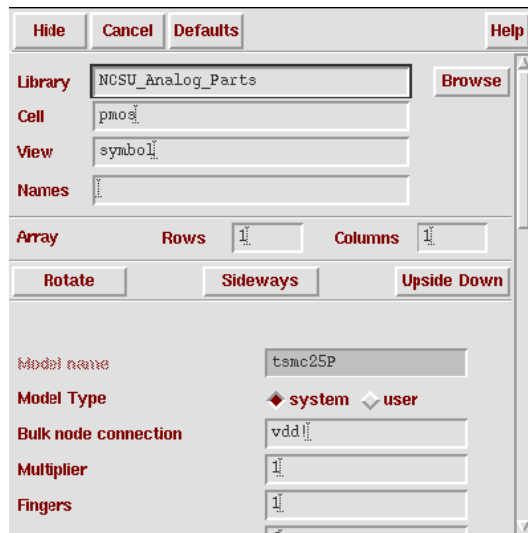
R_L_C : cap

Note: pay attention to the parameters specified in *vdc*, *vpulse*, and *cap*. These parameters are very important in simulation

A. Place pmos instance:

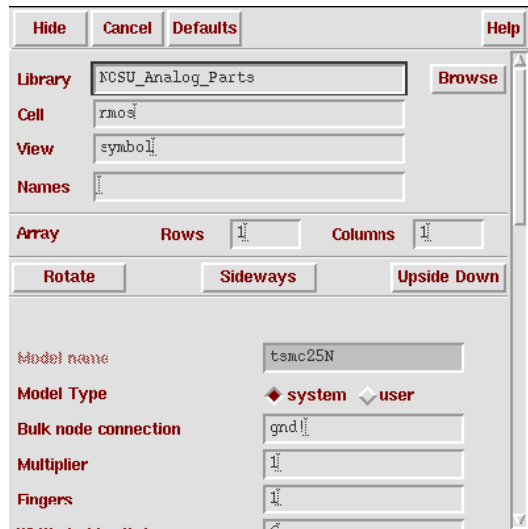
In **Component Browser**, select **P_Transistor** and then **pmos**

Place it in the **Schematic Window**



B. Place nmos instance:

In **Component Browser**, select **N_Transistor** and then **nmos**
Place it in the **Schematic Window**



C. Place gnd instance:

In **Component Browser**, select **Supply_Nets** and then **gnd**
Place it in the **Schematic Window**

Hide	Cancel	Defaults	Help
Library	NCSU_Analog_Parts		Browse
Cell	gnd		
View	symbol		
Names			
Array	Rows	Columns	
Rotate	Sideways	Upside Down	

D. Place vdd instance:

In **Component Browser**, select **Supply_Nets** and then **vdd**
Place it in the **Schematic Window**

Hide	Cancel	Defaults	Help
Library	NCSU_Analog_Parts		Browse
Cell	vdd		
View	symbol		
Names			
Array	Rows	Columns	
Rotate	Sideways	Upside Down	

E. Place IN pin:

From the **Schematic Window** menu, select **Add -> Pin...**
In the Pin Name field , enter “**IN**”
In the Direction field, select **input**
Place it in the **Schematic Window**

Hide	Cancel	Defaults	Help
Pin Names	IN		
Direction	input	Bus Expansion	off on
Usage	schematic	Placement	single multiple
Rotate	Sideways	Upside Down	

G. Place vdc instance

In **Component Browser**, select **Voltage Sources** and then **vdc**
In the DC voltage field, enter “**2.5 V**”

Place it in the **Schematic Window**

Hide Cancel Defaults Help

Library: NCSU_Analog_Parts Browse

Cell: vdd

View: symbol

Names:

Array: Rows: Columns:

Rotate Sideways Upside Down

AC magnitude:

AC phase:

DC voltage: 5 V

Noise file name:

Number of noise/freq pairs:

H. Place vpulse instance

In **Component Browser**, select **Voltage_Sources** and then **vpulse**

Enter the values as shown in the following form (next page)

Place it in the **Schematic Window**

Edit Object Properties

OK Cancel Apply Defaults Previous Next Help

Apply To: only current instance

Show: ☐ system ☒ user ☒ CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	NCSU_Analog_Parts	off
Cell Name	vpulse	off
View Name	symbol	off
Instance Name	v1	off

Add Delete Modify

User Property	Master Value	Local Value	Display
IvsIgnore	TRUE		off

CDF Parameter

CDF Parameter	Value	Display
AC magnitude		off
AC phase		off
Voltage 1	0 V	off
Voltage 2	5 V	off
Delay time	0 s	off
Rise time	500p s	off
Fall time	500p s	off
Pulse width	3n s	off
Period	6ns	off
DC voltage		off
Noise file name		off
Number of noise/freq pairs	0	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Frequency		off
Number of harmonics	1	off
Gibb's compensation	<input type="checkbox"/>	off
DC source		off

I. Place cap instance

In **Component Browser**, select **R_L_C** and then **cap**

In the Capacitance field, enter “**OutCap F**”

(This **Design Variable** will be used in **Artist**.)

Place it in the **Schematic Window**

The screenshot shows the 'Component Browser' dialog box. At the top are buttons: OK, Cancel, Apply, Defaults, Previous, Next, and Help. Below these are 'Apply To' (only current, instance) and 'Show' (system, user, CDF) options. The main section has 'Browse' and 'Reset Instance Labels Display' buttons. It contains a table with columns 'Property', 'Value', and 'Display'. The properties listed are Library Name (NCSU_Analog_Parts), Cell Name (cap), View Name (symbol), and Instance Name (c0), all with 'off' in the Display column. Below this is another table for 'CDF Parameter' with columns 'Value' and 'Display'. The parameters listed are Capacitance (OutCap F), Initial condition, Model name, Width, Length, and Multiplier, all with 'off' in the Display column. At the bottom are 'Add', 'Delete', and 'Modify' buttons.

Property	Value	Display
Library Name	NCSU_Analog_Parts	off
Cell Name	cap	off
View Name	symbol	off
Instance Name	c0	off

CDF Parameter	Value	Display
Capacitance	OutCap F	off
Initial condition		off
Model name		off
Width		off
Length		off
Multiplier	1	off

J. Place wires

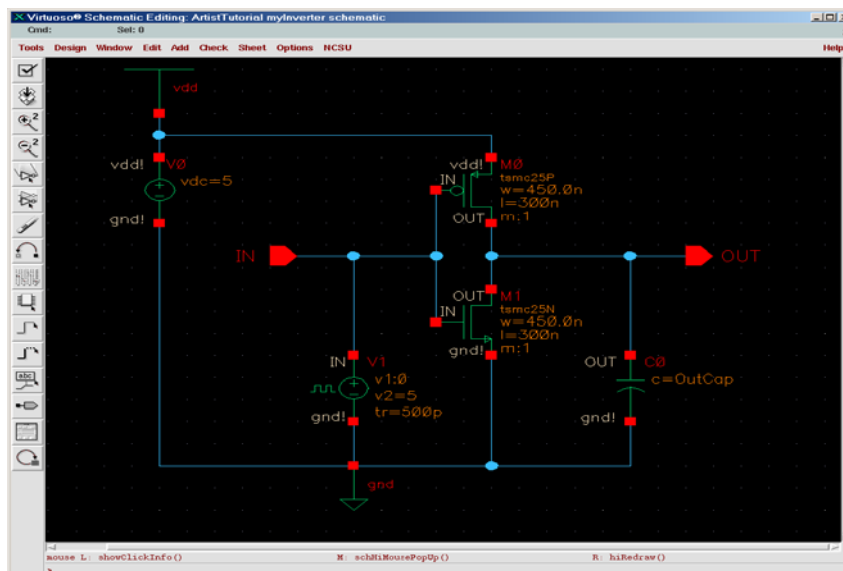
In the **Schematic Window** menu, select **Add -> Wire (narrow)**

Place the wire to connect all the instances

Select **Design -> Check and Save**. CIW will report any errors.

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Your schematic should look like the one shown below.

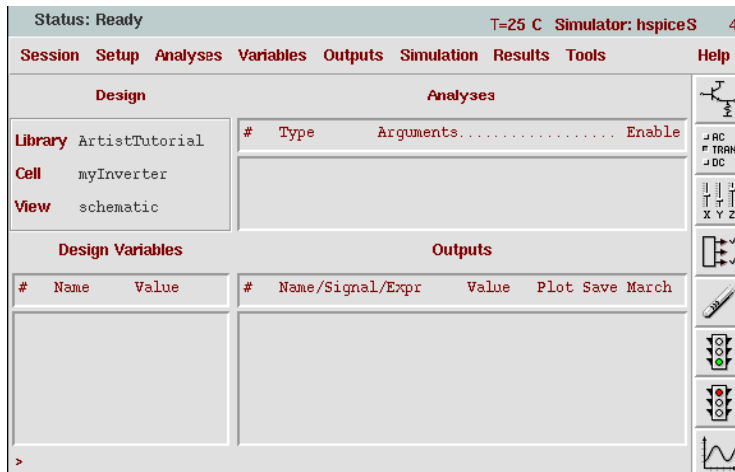


2-2. Schematic Simulation

You are now prepared to simulate your circuit.

From the **Schematic Window** menu, select **Tools -> Analog Environment**

A window will pop-up. This window is the **Analog Environment Simulation Window**.



A. Choose a Simulator

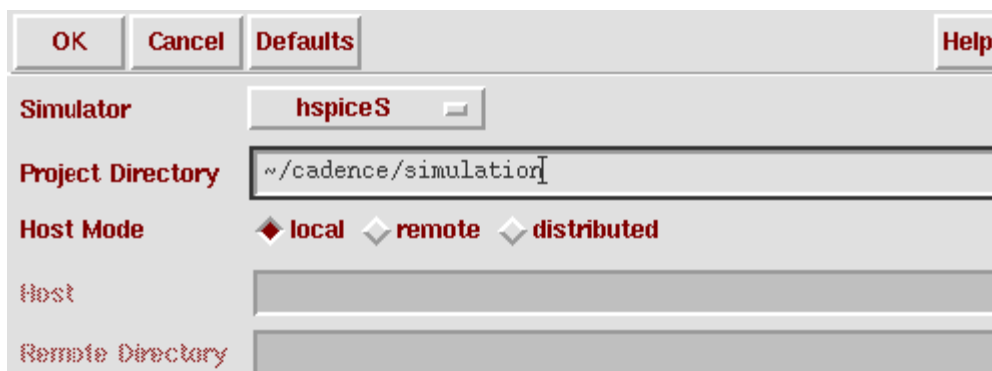
From the **Analog Environment** menu, select **Setup -> Simulator/Directory/Host**.

Enter the fields as shown below.

Choose **hspiceS** as your simulator.

Your simulation will run in the specified Project Directory.

You may choose any valid pathname and filename that you like.



B. Choose Analysis

We will do Transient Analysis on the circuit that we just produced.

From the **Analog Environment** menu, select **Analyses -> Choose...**

Fill out the form as follows:

OK Cancel Defaults Apply Help

Analysis ◇ dc ◇ noise ◇ ac ◆ tran

Transient Analysis

From 0 To 15n By 0.1n

Max Step

Enabled ☒

C. Add a Variable

From the **Analog Environment** menu, select **Variables -> Edit**

The **Editing Design Variables** form will appear.

Fill out the form as shown below, and then click **Add** to send this Variable to the Table of Design Variables.

(We entered the OutCap Design Variable in section 3.I.)

OK Cancel Apply Apply & Run Simulation Help

Selected Variable Table of Design Variables

Name OutCap # Name Value

Value (Expr) 0.01p

Add Delete Change Next Clear Find

Cellview Variables Copy From Copy To

D. Setup Output

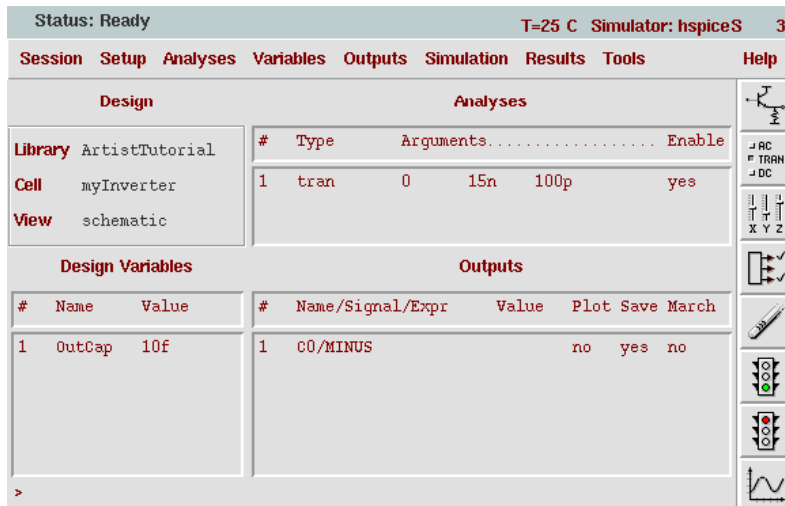
When using Transient Analysis, the transient voltage will be saved automatically.

We can save the current through capacitor C0 in the schematic by doing the following:

From the **Analog Environment** menu, select

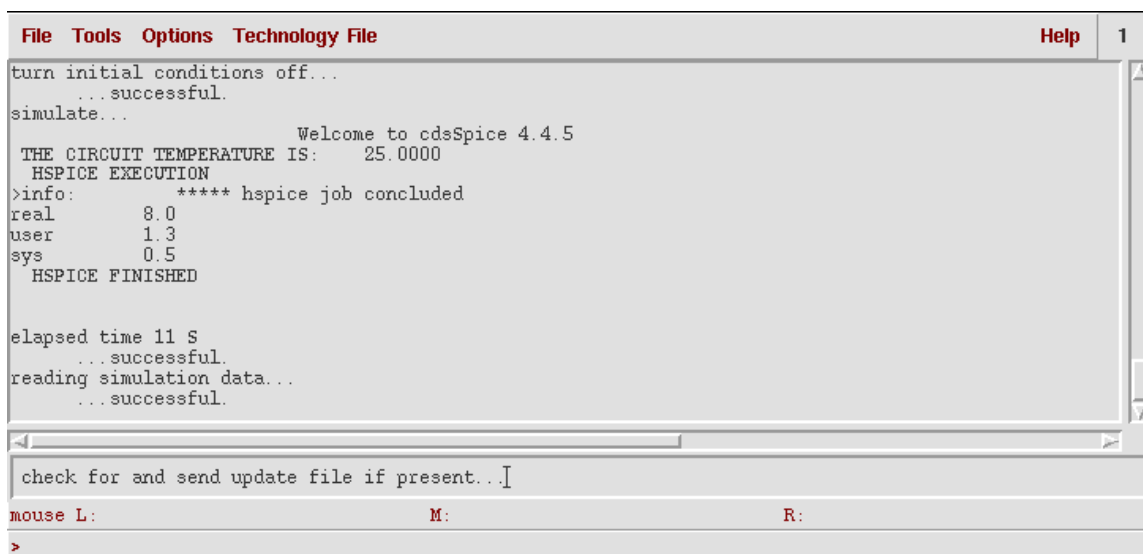
Outputs -> To be Saved -> Select On Schematic

In the **Schematic Window**, click on the lower terminal (not the wire) of capacitor C0. After you click on the terminal, the **Analog Environment Window** should look like this:



Simulating the schematic

From the **Analog Environment** menu, select **Simulation -> Run**. Look at the echoing information in the **CIW** window. If the simulation succeeds, the window will display “...successful.”



Waveform Window

From the **Analog Environment** menu, select

Results -> Direct Plot -> Transient Signal

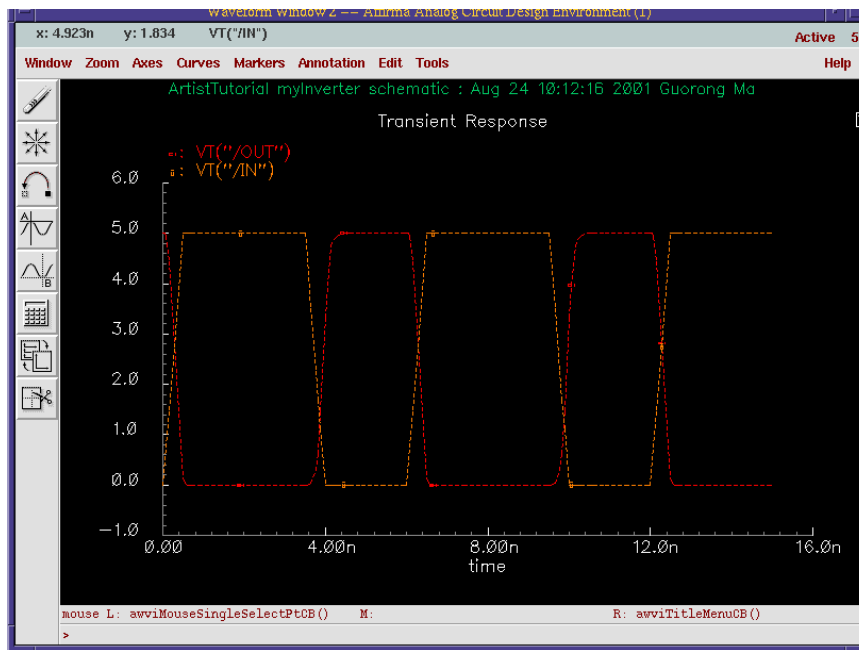
The **Waveform Window** will then pop up

In the **Schematic Window**,

Click on the IN wire and then **Click on the OUT wire**

Press **ESC** on your keyboard

The two curves (IN and OUT) will then be displayed in this window:



The following simulator settings have to be made:

menu bar command	details
<i>Setup - Simulator/Directory/Host</i>	<ul style="list-style-type: none"> - Set <i>Simulator</i> to <i>spectre</i> - Also the <i>Project Directory</i> could be changed here
<i>Setup - Model Libraries</i>	<ul style="list-style-type: none"> - Paths to the <i>Model Library Files</i> should be okay
<i>Setup - Temperature</i>	<ul style="list-style-type: none"> - Set <i>Degrees</i> to <i>25</i>
<i>Setup - Environment</i>	<ul style="list-style-type: none"> - <i>Switch View List</i> should be set to <i>spectre cmos_sch schematic</i> - <i>Stop View List</i> should be set to <i>spectre ahdl</i>
<i>Analyses - Choose</i>	<ul style="list-style-type: none"> - Set <i>Analysis</i> to <i>trans</i> - Set <i>Stop Time</i> to <i>200n</i> - <i>Accuracy Defaults</i> should be set to <i>conservative</i> - A description of the analysis will be listed in the field <i>Analyses</i> of the Affirma Analog Environment tool - To edit the <i>Analyses</i> entries either double-click on an entry or select <i>Analyses Choose</i> again
<i>Variables - Copy From Cellview</i>	<ul style="list-style-type: none"> - Variables in the simulation schematic will be identified and will be listed in the field <i>Design Variables</i> of the Affirma Analog Environment tool - To edit the <i>Design Variables</i> entries either double-click on an entry or select <i>Variables - Edit</i> from the menu bar - Set <i>output_load</i> to <i>15f</i> - Set <i>input_slew</i> to <i>1n</i>
<i>Outputs - To Be Plotted - Select On Schematic</i>	<ul style="list-style-type: none"> - Select the signals to plot in the simulation schematic: net (must be named!) => voltage; object node => current into the object through this node - Selected signals will be listed in the field <i>Outputs</i> of the Affirma Analog Environment tool - To edit the <i>Outputs</i> entries either double-click on an entry or select <i>Outputs - Setup</i> from the menu bar

Other commands of the Analog Environment:

command	menu bar command
Run the simulation without rebuilding the netlist	<i>Simulation - Run</i>
Create the netlist if the schematic has changed	<i>Simulation - Netlist - Create</i>
View the netlist	<i>Simulation - Netlist - Display</i>
Force the recreation of the netlist even if the schematic didn't change	<i>Simulation - Netlist - Recreate</i>
Plot the simulation results manually	<i>Results - Plot Outputs - Transient</i>
Start a parametric analysis (sweep design variables in a specific range)	<i>Tools - Parametric Analysis</i>
Calculate parameters of the cell (propagation delay, output slew, ...) from the simulation results	<i>Tools - Calculator</i>
Browse the simulation results	<i>Tools - Results Browser</i>
Open an additional waveform window	<i>Tools - Waveform</i>
Save an OCEAN script to perform the simulation of the netlist	<i>Session - Save Script</i>
Save the current Affirma Analog Environment settings	<i>Session - Save State</i>
Load Affirma Analog Environment settings	<i>Session - Load State</i>
Specify the directory where the Affirma Analog Environment settings are saved	<i>Session - Options (field: State Save Directory)</i>