2. Schematic Entry with Composer

2-1 Creating the Schematic

(1) Creating a library and a schematic cell view

At first a new library that will contain the data for the implemented cell is created. From the menu bar of the Library Manager select

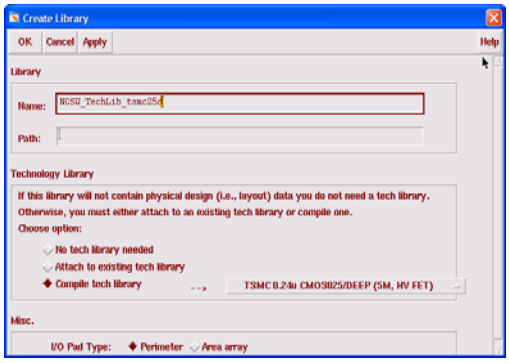
*In Library Manager, Click **File - New - Library***

In the Name filed, enter " **NCSU_TechLib_tsmc25d**"

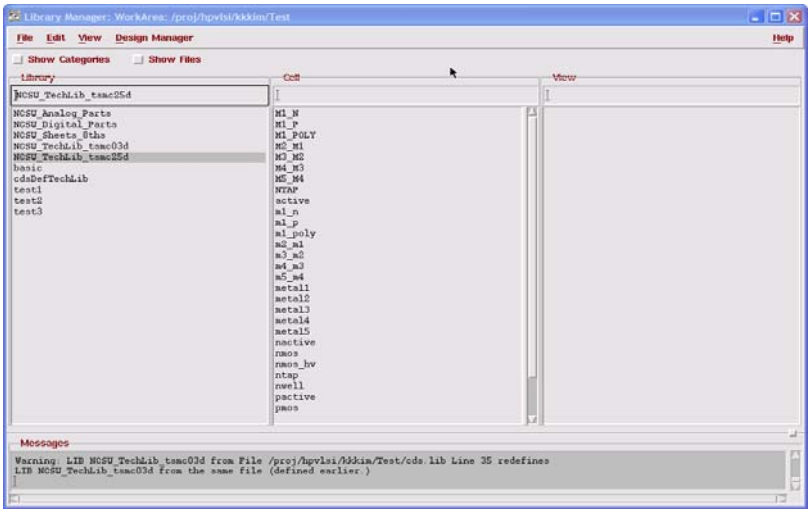
In the Technology Library box, select

Compile tech library -> TSMC 0.24u

Press OK.

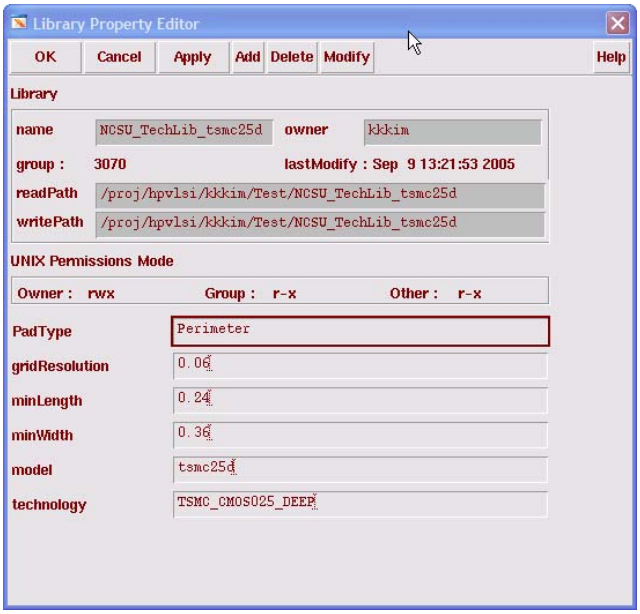


Then the Library Manager will refresh as follows:



Select **NCSU_TechLib_tsmc25d**, and *In Library Manager, Click* ***Edit - Properties***

In the model field, enter **tsmc25d**, and click **OK**.



(2) Creating working library and a schematic cell view

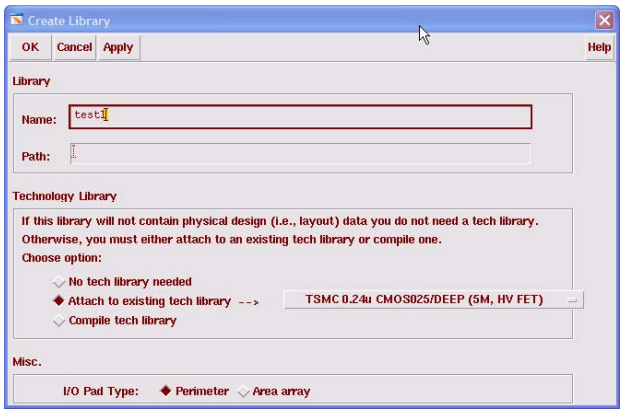
In Library Manager, Click ***File - New - Library***

In the Name filed, enter " **test**"

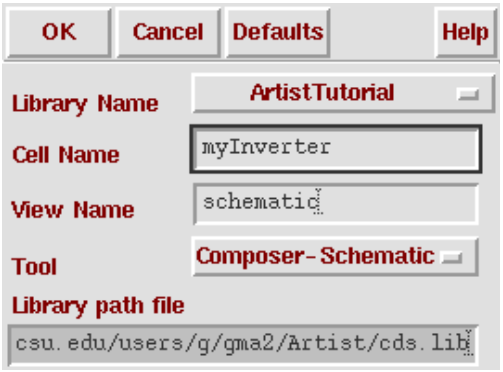
In the Technology Library box, select

Attach to existing tech library -> TSMC 0.24u

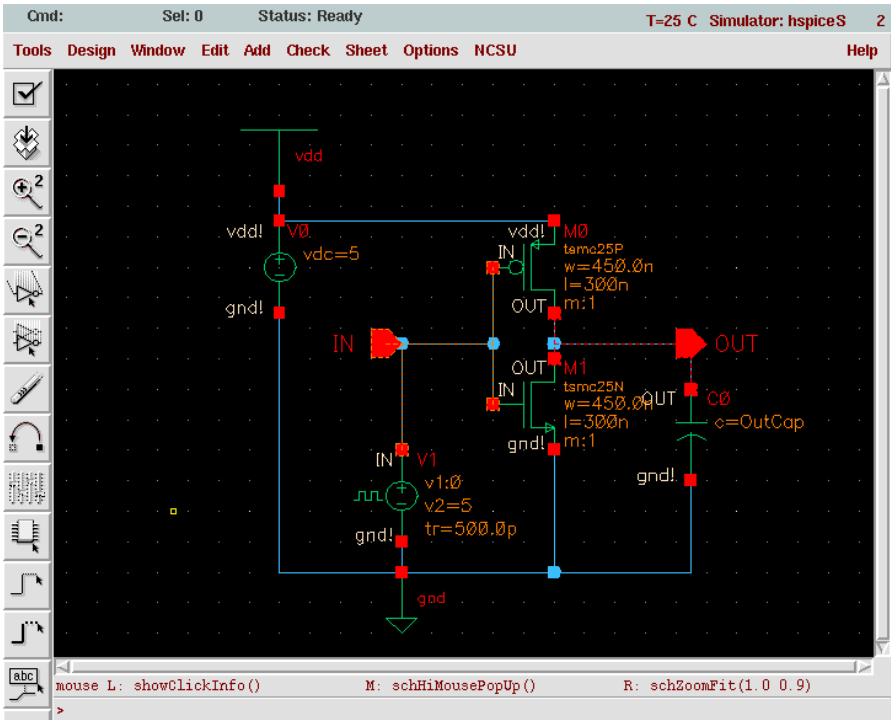
Press OK.



In **Library Manager,** select **ArtistTutorial**
From the Menu Bar, select **File -> New -> CellView**
Fill the Form as follows, then click **OK**



A blank Schematic window will then appear.
We need to generate a schematic as shown below:

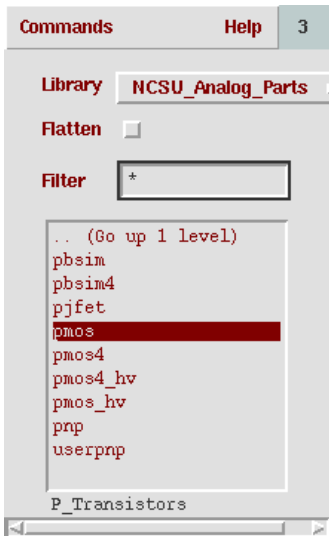


Drawing the schematic

To generate a schematic like this, you will need to go through the following steps:

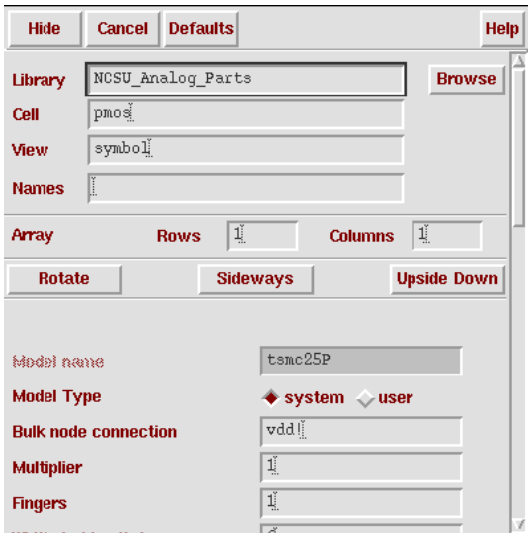
From the Schematic Window menu, select Add -> instance (shortcut <i>)

The Component Browser, will then pop up.

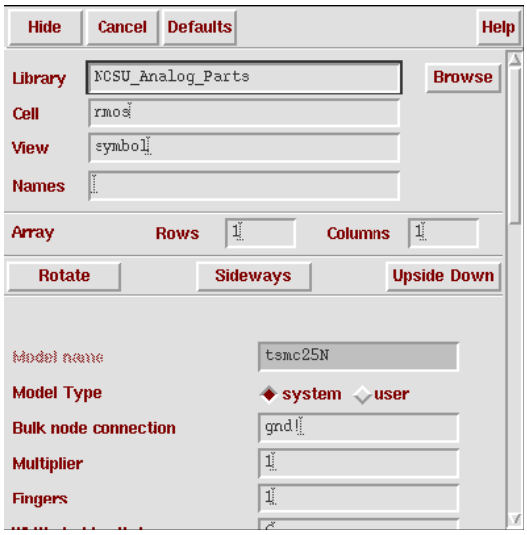


In the **Library** field, select **NCSU_Analog_Parts**
We will place the following instances in the **Schematic Window** from the **NCSU_Analog_Parts** library as instructed below:
N_Transistor : nmos
P_Transistor : pmos
Supply_Nets : vdd , gnd
Voltage_Sources : vdc,vpulse
R_L_C : cap
Note: pay attention to the parameters specified in *vdc, vpulse,* and *cap*. These parameters are very important in simulation

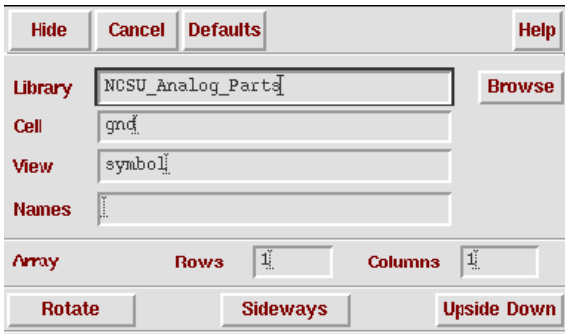
A. Place pmos instance:
In **Component Browser**, select **P_Transistor** and then **pmos**
Place it in the **Schematic Window**



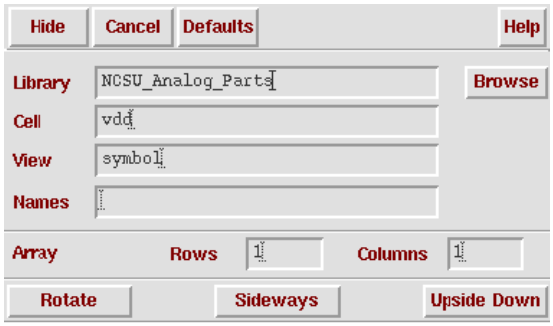
B. Place nmos instance:
In **Component Browser**, select **N_Transistor** and then **nmos**
Place it in the **Schematic Window**



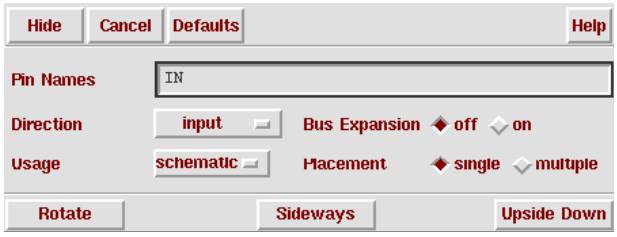
C. Place gnd instance:
In **Component Browser**, select **Supply_Nets** and then **gnd**
Place it in the **Schematic Window**



D. Place vdd instance:
In **Component Browser**, select **Supply_Nets** and then **vdd**
Place it in the **Schematic Window**

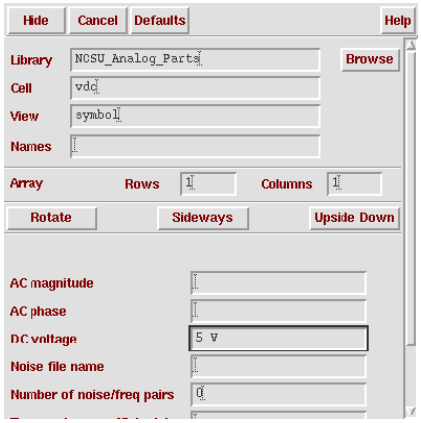


E. Place IN pin:
From the **Schematic Window** menu, select **Add -> Pin...**
In the Pin Name field , enter "**IN**"
In the Direction field, select **input**
Place it in the **Schematic Window**



G. Place vdc instance
In **Component Browser**, select **Voltage Sources** and then **vdc**
In the DC voltage field, enter "**2.5 V**"

Place it in the **Schematic Window**



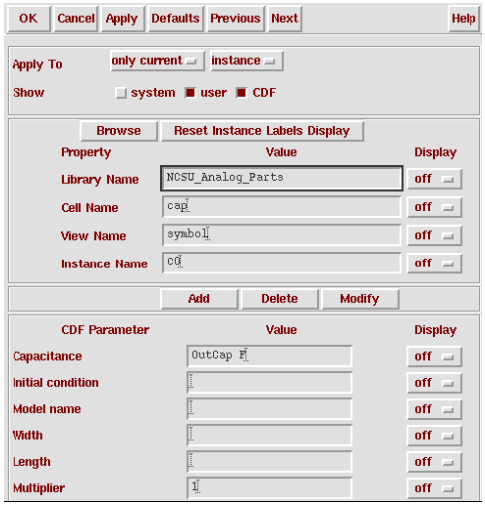
H. Place vpulse instance

In **Component Browser**, select **Voltage_Sources** and then **vpulse**

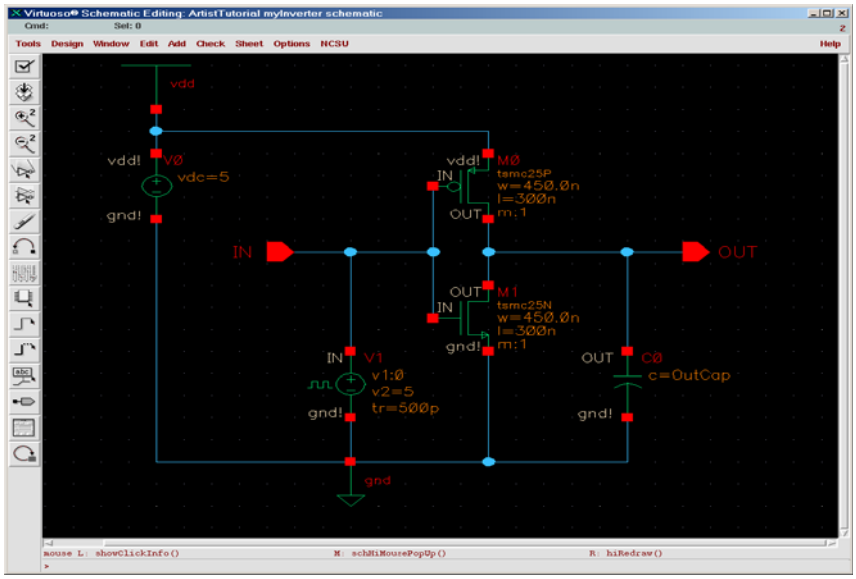
Enter the values as shown in the following form (next page)

Place it in the **Schematic Window**

I. Place cap instance
In **Component Browser**, select **R_L_C** and then **cap**
In the Capacitance field, enter "**OutCap F**"
(This **Design Variable** will be used in **Artist**.)
Place it in the **Schematic Window**

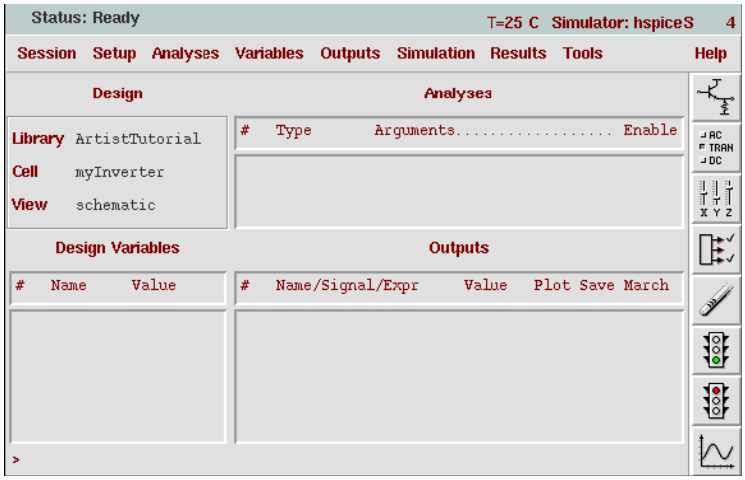


J. Place wires
In the **Schematic Window** menu, select **Add -> Wire (narrow)**
Place the wire to connect all the instances
Select **Design -> Check and Save**. CIW will report any errors.
13
Your schematic should look like the one shown below.

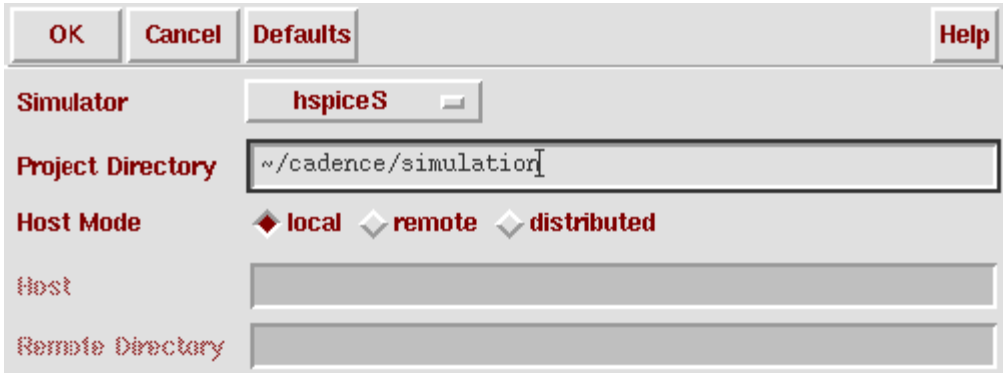


2-2. Schematic Simulation

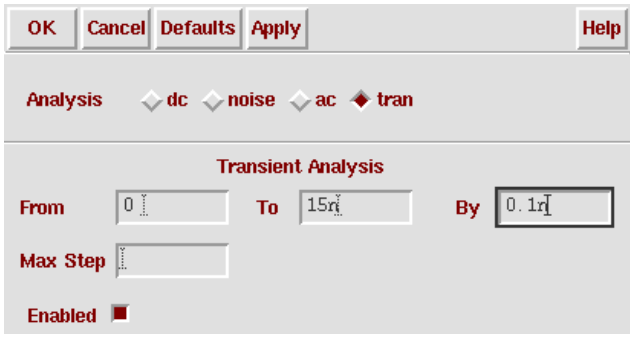
You are now prepared to simulate your circuit.
From the **Schematic Window** menu, select **Tools -> Analog Environment**
A window will pop-up. This window is the **Analog Environment Simulation Window**.



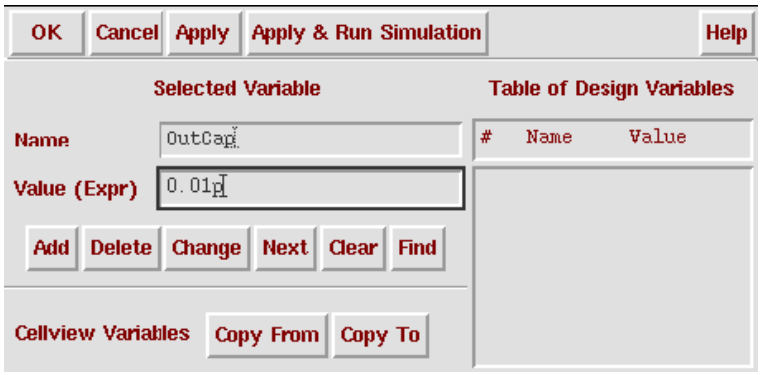
A. Choose a Simulator
From the **Analog Environment** menu, select **Setup -> Simulator/Directory/Host**.
Enter the fields as shown below.
Choose **hspiceS** as your simulator.
Your simulation will run in the specified Project Directory.
You may choose any valid pathname and filename that you like.



B. Choose Analysis
We will do Transient Analysis on the circuit that we just produced.
From the **Analog Environment** menu, select **Analyses -> Choose...**
Fill out the form as follows:

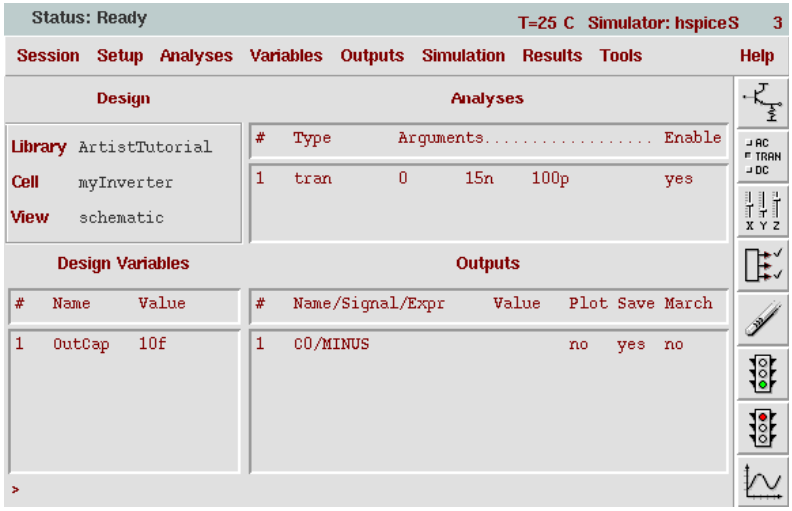


C. Add a Variable
From the **Analog Environment** menu, select **Variables -> Edit**
The **Editing Design Variables** form will appear.
Fill out the form as shown below, and then click **Add** to send this Variable to the Table of Design Variables.
(We entered the OutCap Design Variable in section 3.I.)



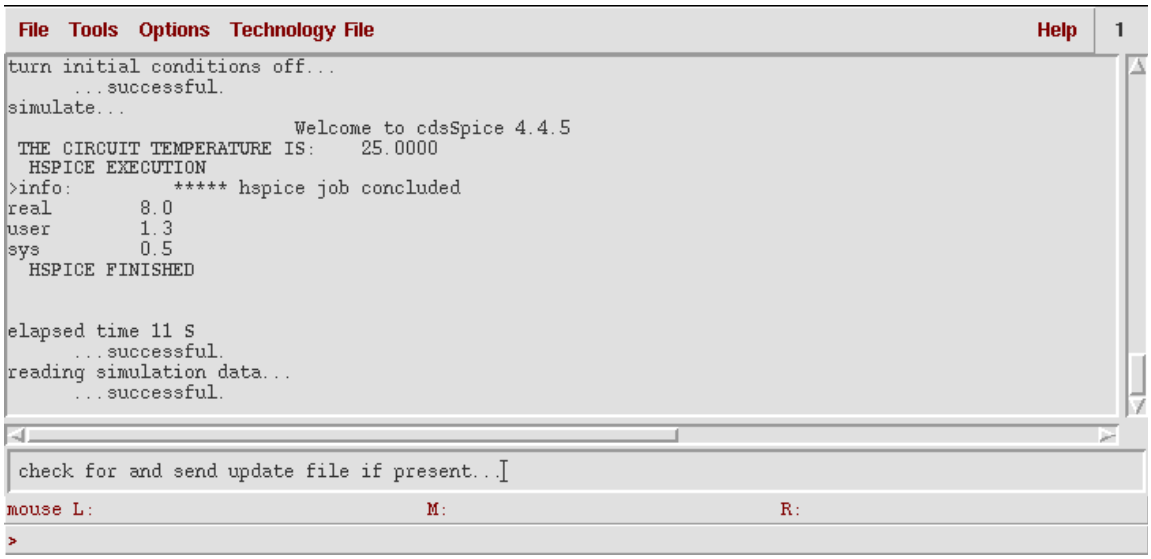
D. Setup Output
When using Transient Analysis, the transient voltage will be saved automatically.
We can save the current through capacitor C0 in the schematic by doing the following:
From the **Analog Environment** menu, select
Outputs -> To be Saved -> Select On Schematic

In the **Schematic Window**, click on the lower terminal (not the wire) of capacitor C0. After you click on the terminal, the **Analog Environment Window** should look like this:



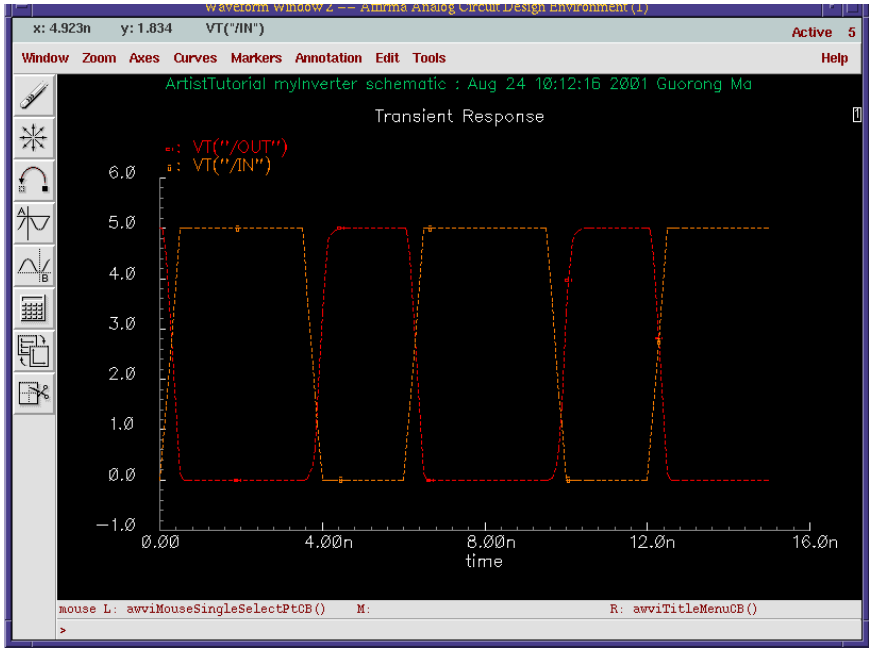
Simulating the schematic

From the **Analog Environment** menu, select **Simulation -> Run**,
Look at the echoing information in the **CIW** window.
If the simulation succeeds, the window will display "...successful."



Waveform Window

From the **Analog Environment** menu, select
Results -> Direct Plot -> Transient Signal
The **Waveform Window** will then pop up
In the **Schematic Window**,
Click on the IN wire and then **Click on the OUT wire**
Press **ESC** on your keyboard
The two curves (IN and OUT) will then be displayed in this window:



The following simulator settings have to be made:

menu bar command	details
Setup - Simulator/Directory/Host	- Set *Simulator* to *spectre* - Also the *Project Directory* could be changed here
Setup - Model Libraries	- Paths to the *Model Library Files* should be okay
Setup - Temperature	- Set *Degrees* to *25*
Setup - Environment	- *Switch View List* should be set to *spectre cmos_sch schematic* - *Stop View List* should be set to *spectre ahdl*
Analyses - Choose	- Set *Analysis* to *trans* - Set *Stop Time* to *200n* - *Accuracy Defaults* should be set to *conservative* - A description of the analysis will be listed in the field *Analyses* of the Affirma Analog Environment tool - To edit the *Analyses* entries either double-click on an entry or select *Analyses Choose* again
Variables - Copy From Cellview	- Variables in the simulation schematic will be identified and will be listed in the field *Design Variables* of the Affirma Analog Environment tool - To edit the *Design Variables* entries either double-click on an entry or select *Variables - Edit* from the menu bar - Set *output_load* to *15f* - Set *input_slew* to *1n*
Outputs - To Be Plotted - Select On Schematic	- Select the signals to plot in the simulation schematic: net (must be named!) => voltage; object node => current into the object through this node - Selected signals will be listed in the field *Outputs* of the Affirma Analog Environment tool - To edit the *Outputs* entries either double-click on an entry or select *Outputs - Setup* from the menu bar

Other commands of the Analog Environment:

command	menu bar command
Run the simulation without rebuilding the netlist	*Simulation - Run*
Create the netlist if the schematic has changed	*Simulation - Netlist - Create*
View the netlist	*Simulation - Netlist - Display*
Force the rectreation of the netlist even if the schematic didn't change	*Simulation - Netlist - Recreate*
Plot the simulation results manually	*Results - Plot Outputs - Transient*
Start a parametric analysis (sweep design variables in a specific range)	*Tools - Parametric Analysis*
Calculate parameters of the cell (propagation delay, output slew, ...) from the simulation results	*Tools - Calculator*
Browse the simulation results	*Tools - Results Browser*
Open an additional waveform window	*Tools - Waveform*
Save an OCEAN script to perform the simulation of the netlist	*Session - Save Script*
Save the current Affirma Analog Environment settings	*Session - Save State*
Load Affirma Analog Environment settings	*Session - Load State*
Specify the directory where the Affirma Analog Environment settings are saved	*Session - Options* (field: *State Save Directory*)