EECE7248 Lab #1:
Common-Emitter and Common-Source Amplifier

Gyunam Jeon, Yixuan He, Yong-Bin Kim

In this lab, you will use both BJT (npn) and CMOS (nMOS) to design the common source and emitter amplifier. You utilize the lab tutorial schematic and test bench. There are four regions (0 = off, 1 = linear, 2 = saturation, 3= subthreshold) in MOSFET, and five regions (0 = off, 1 = forward bias, 2 = reverse bias, 3 = saturation, 4 = breakdown) in BJT. You need to identify the devices' region and plot curves. In addition, you used "DC" analysis in Lab #1.

Design #1. Common Source Amplifier (nMOS with passive load, R_D)

1) plot V_{OUT} (DC) vs V_{IN} (DC) and identify the region (off, linear, and saturation) of nMOS transistor
    a. Change R_D (500Ω, 1KΩ, 10KΩ, 100KΩ) with fixed nMOS W/L ratio (32um/180nm)
    b. Change W/L ratio (4um/180nm, 16um/180nm, 32um/180nm, 32um/1um) with fixed R_D (500Ω)

    ***** Notes *****

    *To plot V_{OUT} vs V_{IN}, you need to sweep the input DC voltage (Make the DC voltage in "vsin (analoglib)" as a variable) from 0V to 1.8V with 0.1V interval.

    To sweep the DC voltage, select DC in Analyses → enable "Design Variable" → Select design variable → choose "variable name" → choose number of Start and Stop in Sweep Range → select linear in sweep type → choose a number in step size

    *To plot the graphs with different parameters together in one screen, select the option in the ADE_L Window as follow.

2) plot I_D (DC) vs $V_{DS=OUT}$ (DC) and identify the region (off, linear, and saturation) of nMOS
    a. Change W/L ratio (4um/180nm, 16um/180nm, 32um/180nm, 32um/1um) with fixed R_D (500Ω)
    b. Change VGS (from 0V to 1.8V with 0.1V interval) with fixed (500Ω) and W/L (32um/180nm)

    ***** Notes *****

    *To plot I_D vs V_{DS}, you need to save the current, I_D. Select "Outputs" → "Save All" → enable "all" of "select device currents" in the basic tab. Furthermore, you need to add a VDC (DC voltage

source) in analogLib library to the OUT wire and sweep the voltage from 0V to 1.8V with 0.1V interval.

*Select DC voltage in the "vsin" and sweep the voltage from 0V to 1.8V with 0.1V interval. Furthermore, you need to probe a drain terminal of nMOS (a red square instead a wire). To sweep two different variables simultaneously in Virtuoso, select "Tools" in ADE_L → Parametric Sweep.

3) Plot gain of the amplifier in dB with varying the load, R_D and W/L (V_{GS} = 0.75V)
    a. Change R_D (500Ω, 1KΩ, 10KΩ, 100KΩ) with fixed nMOS W/L ratio (32um/180nm)
    b. Change W/L ratio (4um/180nm, 16um/180nm, 32um/180nm, 32um/1um) with fixed R_D (500Ω)

Design #2. Common Emitter Amplifier (npn BJT with passive load, R_D)

Create new cell (schematic) in the AIC_Lab library and place the npn BJT and the passive load, R_D to form the common emitter amplifier.

1) plot V_{OUT} vs V_{IN} and identify the region of npn BJT
    a. Change R_D (500Ω, 1KΩ, 10KΩ, 100KΩ) with fixed npn emitter width (0.6)

2) plot I_b vs V_{IN} curve and identify the region of npn BJT
    a. Change R_D (500Ω, 1KΩ, 10KΩ, 100KΩ) with fixed npn emitter width (0.6)

3) Plot gain of the amplifier with varying the load, R_D (V_{BE} = 0.75V)
    a. Change R_D (500Ω, 1KΩ, 10KΩ, 100KΩ) with fixed npn emitter width (0.6)

*********Please take the "Student Laboratory Report Format" on the course (Lab) web page as a reference when you write the lab report. Notice that for this lab, appropriate comments and conclusions are required. Besides, the images of the circuit schematic and test bench are also required in the report. ***********