EECE7248 Lab Tutorial: Common-Source Amplifier Layout

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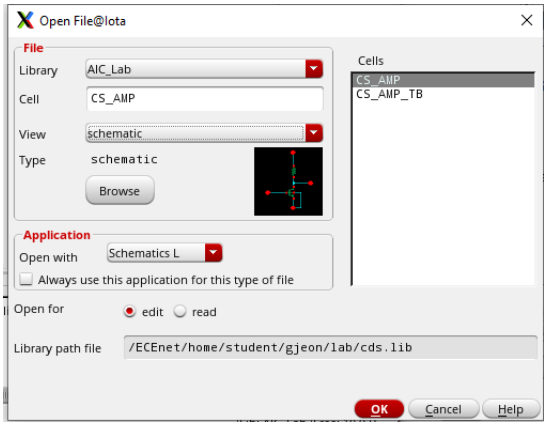
This tutorial briefly introduces the circuit simulation in Cadence. A simple common-source amplifier has been built and simulated step by step using layout entry.

Layout

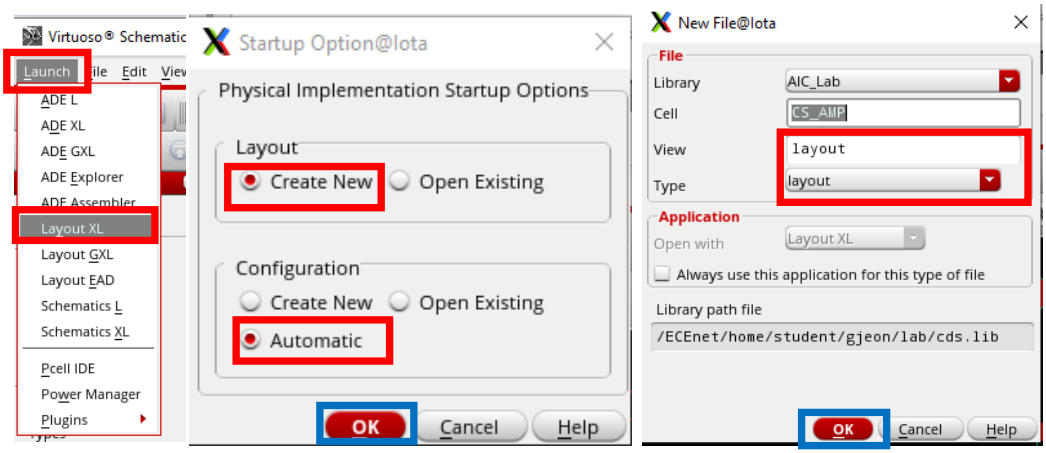
1. Open Existing Schematic

- Select “File” in CIW → “Open” to open the existing schematic (Ex: CS_AMP) .
- You can always manage your libraries by selecting “Tools” in CIW → “Library Manager”.



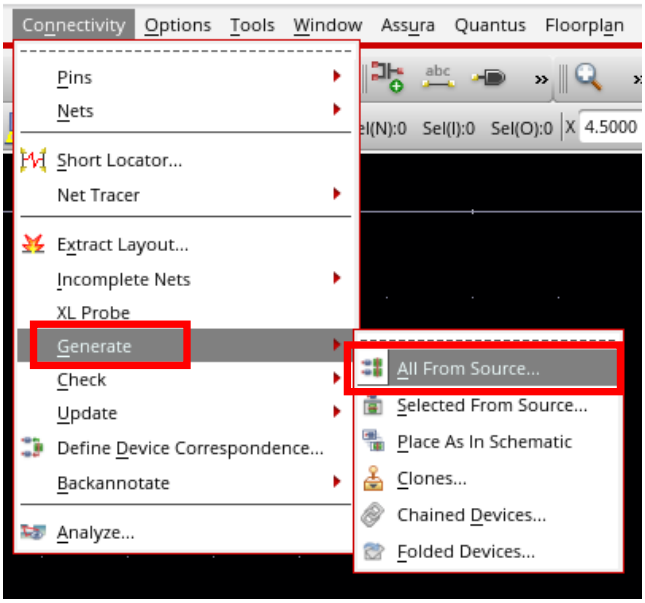
2. Create a Layout

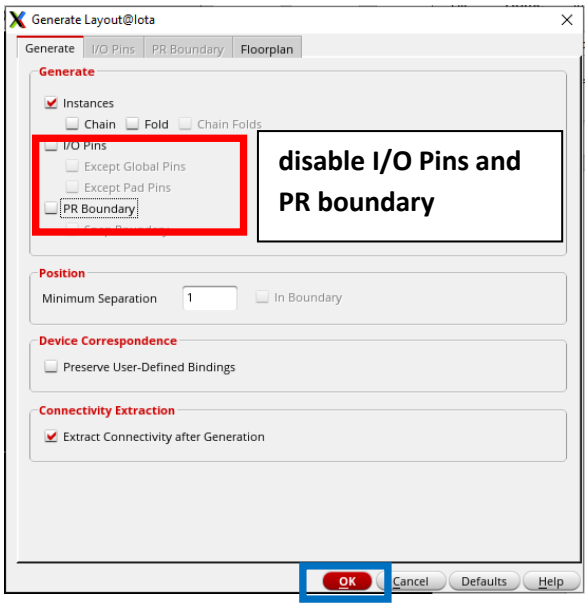
- After opening the schematic of the commons source amplifier,
- Select “Launch” → “Layout XL” to create a layout for CS_AMP schematc.

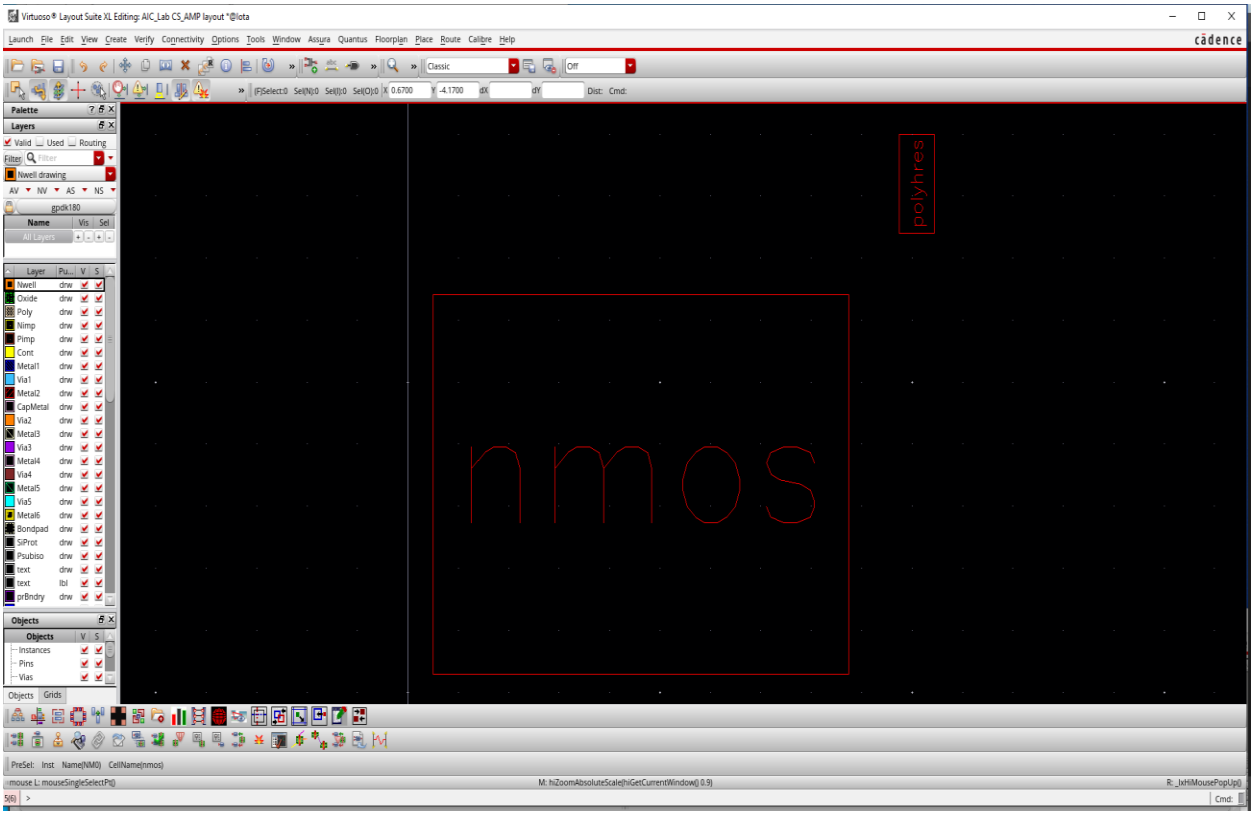


3. Generate Layout from Source

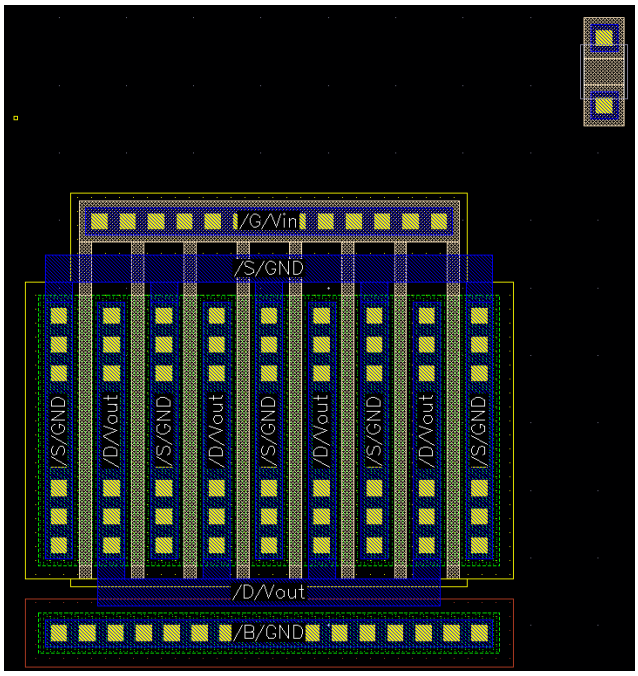
- After opening the layout windows,
- Select "Connectivity" → "Generate" → "All From Source" to load matched layout from schematic



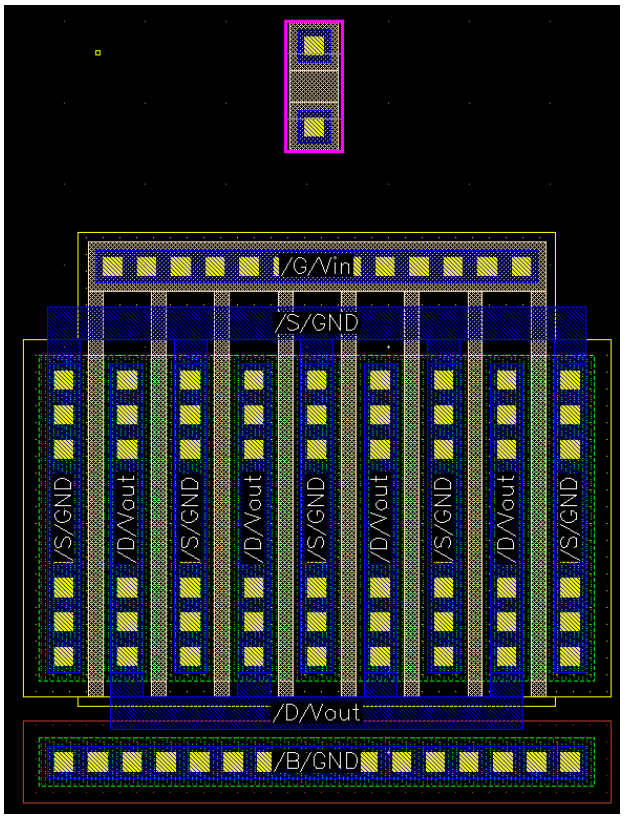




- To view layers in the layout windows, press the **SHIFT key** and the **letter F** and the layers will be appeared.

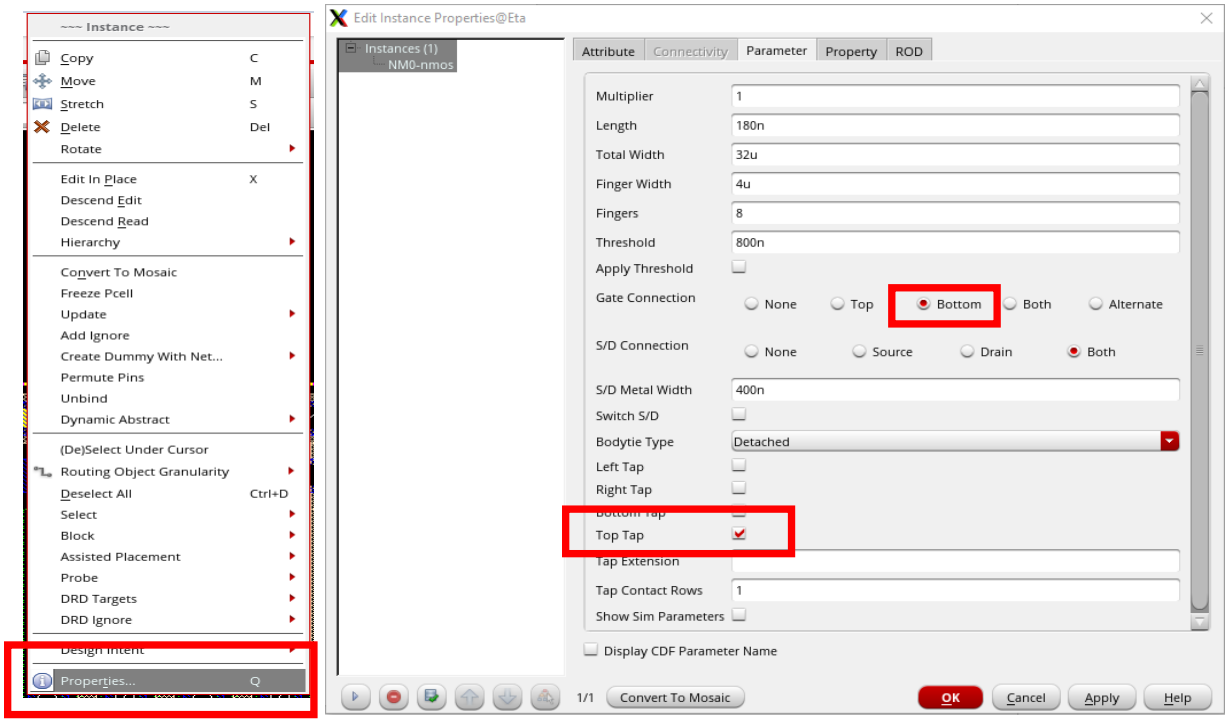


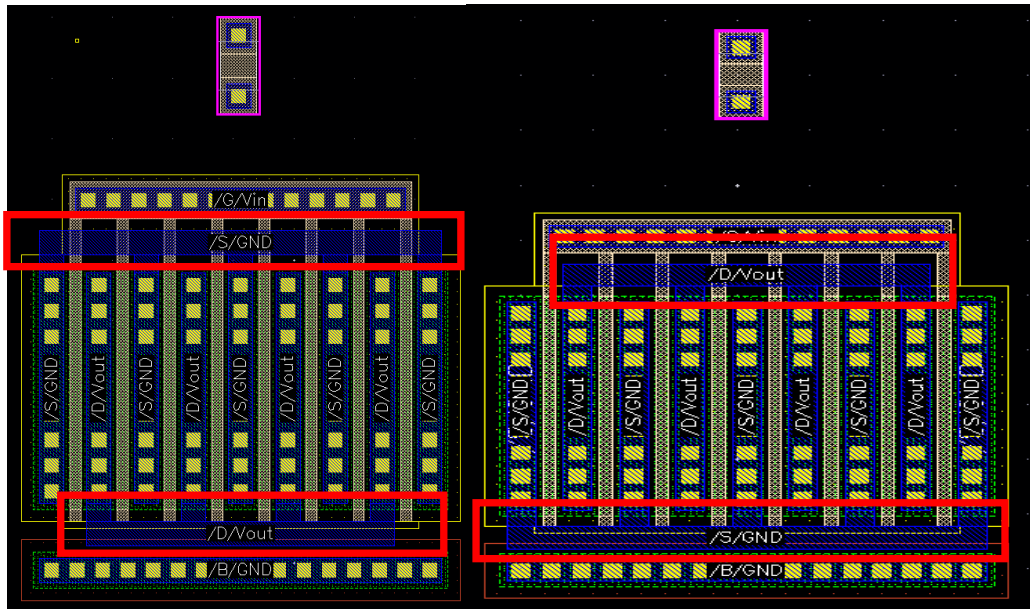
- Move the resistor in the middle as shown in the figure below.
- Press “Letter M” → Click “Resistor” → Drag the resistor.



4. Relocate Body Layer and Rotate Layout

- To relocate body in the layout,
- Select “nMos” → click “right mouse button” → “properties” (shortcut key: Q)
- Change Body to “Top Tap”
- Rotate the nMOS layer (Select “nMos” → Click “right mouse button” → “Rotate” → “Flip Vertically”)

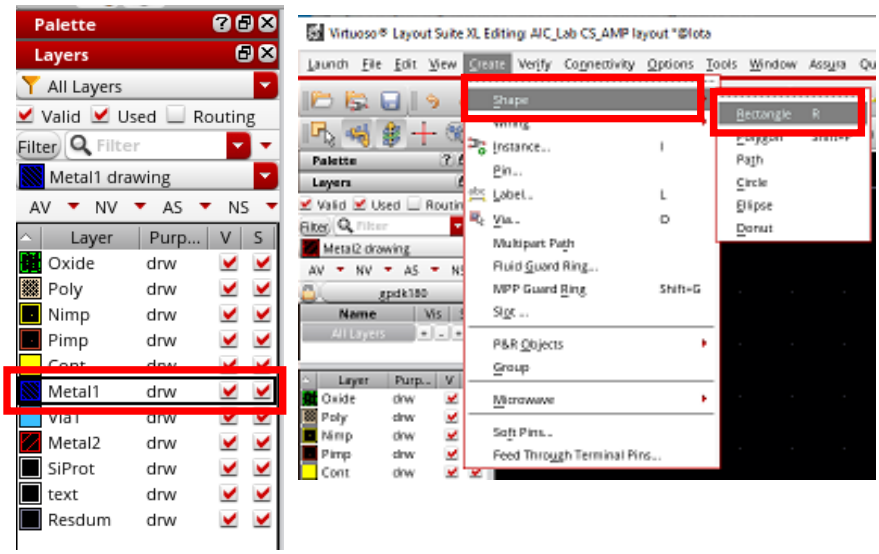




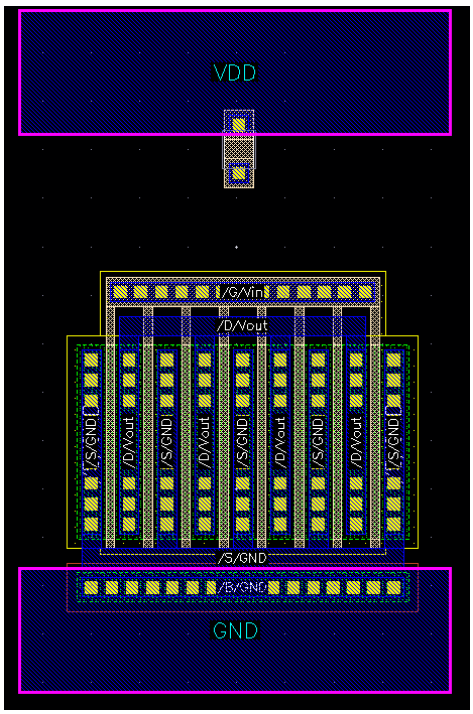
- **Before** **After relocation and Rotation**

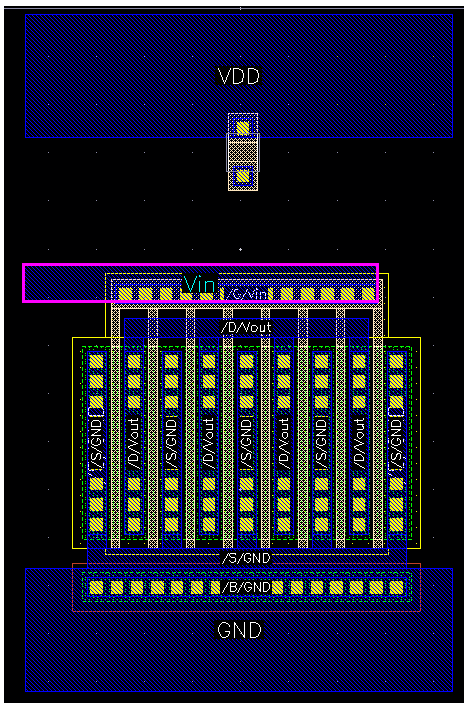
5. Draw Metal 1 Layer

- To draw the metal 1 layer (horizonal layer),
- Select “Metal 1 ” in layers window → “Create” → “Shape” → “Rectangle” (shortcut key: R)
- Make a large rectangle using left mouse button (Click one point → extend the rectangle → click the another point)



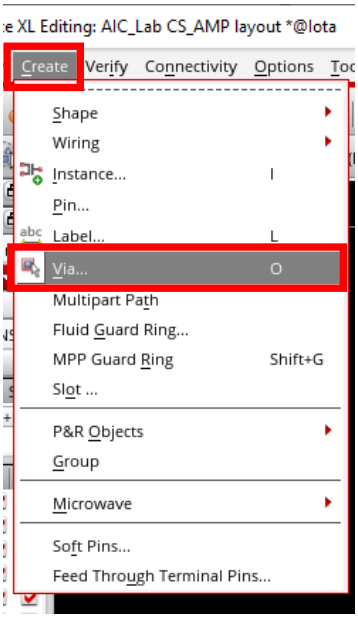
- Draw VDD, GND, and Vin as shown in the figures below.

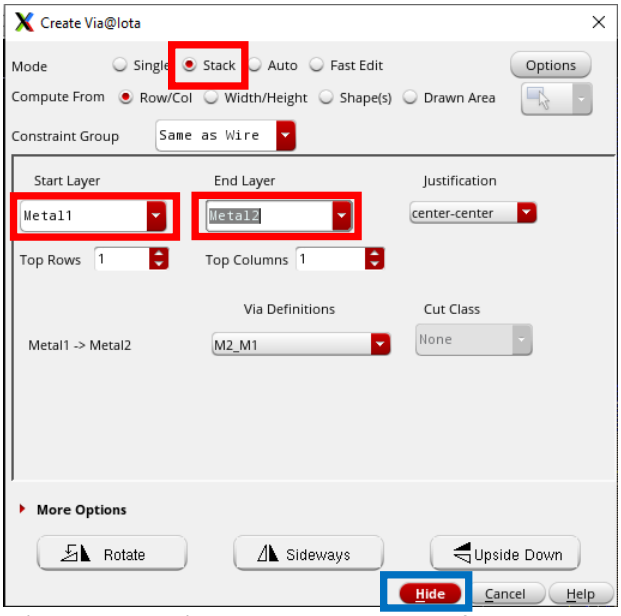




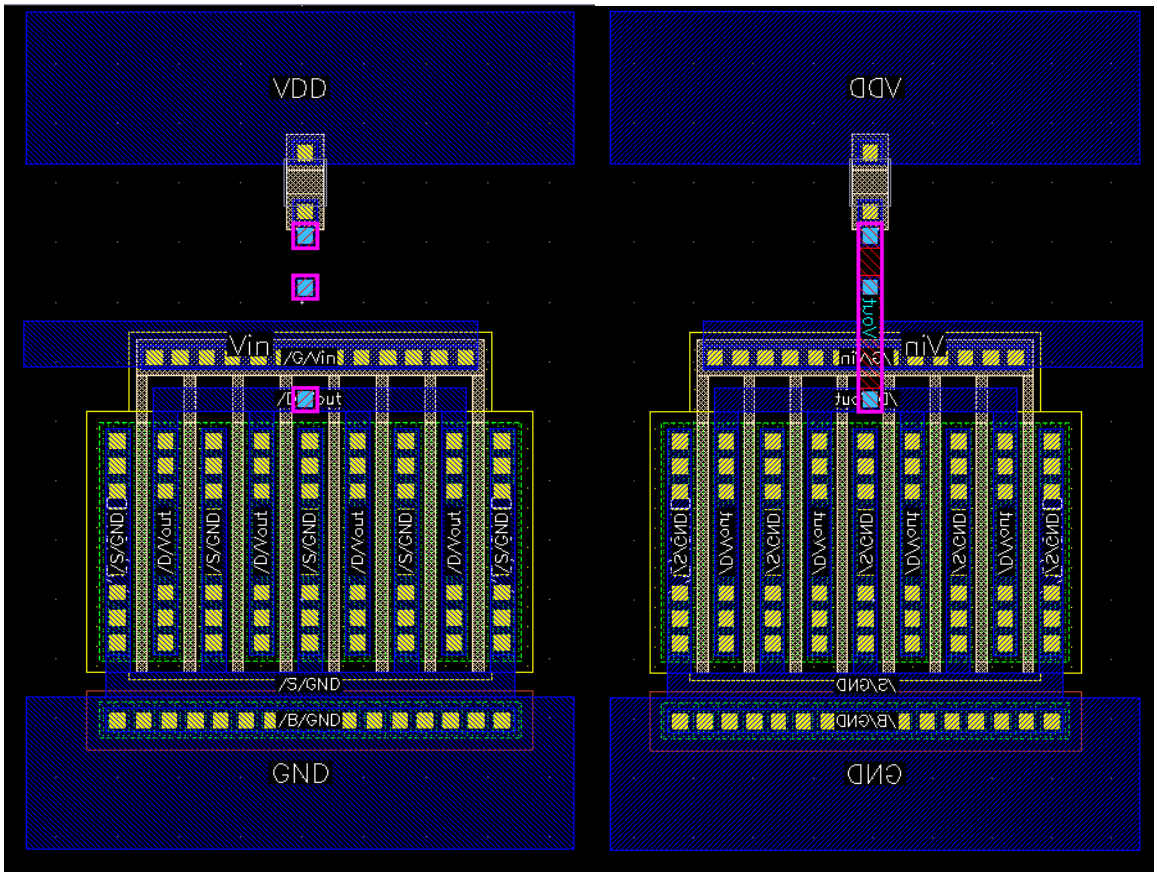
6. Place a Via

- To place a via (Connection between Metal 1 and Metal 2)
- Select “Create” → “Via” (Shortcut key: O)

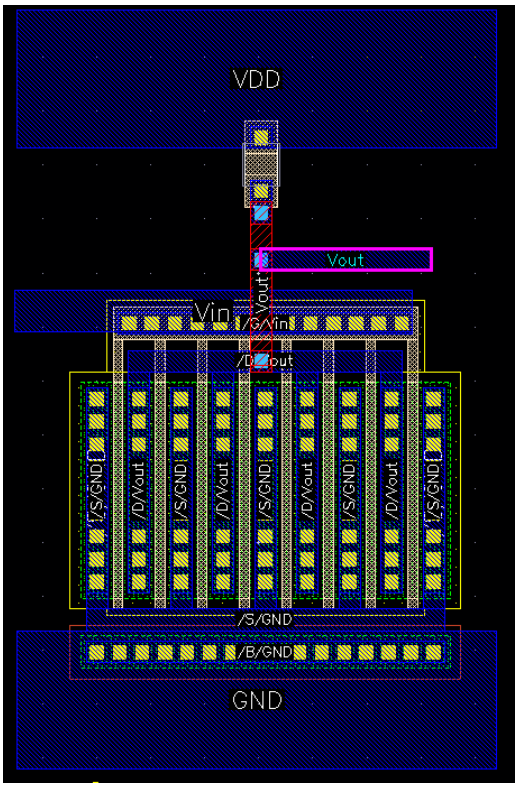




- Place the Vias and draw metal 2 (vertical layer) layer as shown in the figure below.

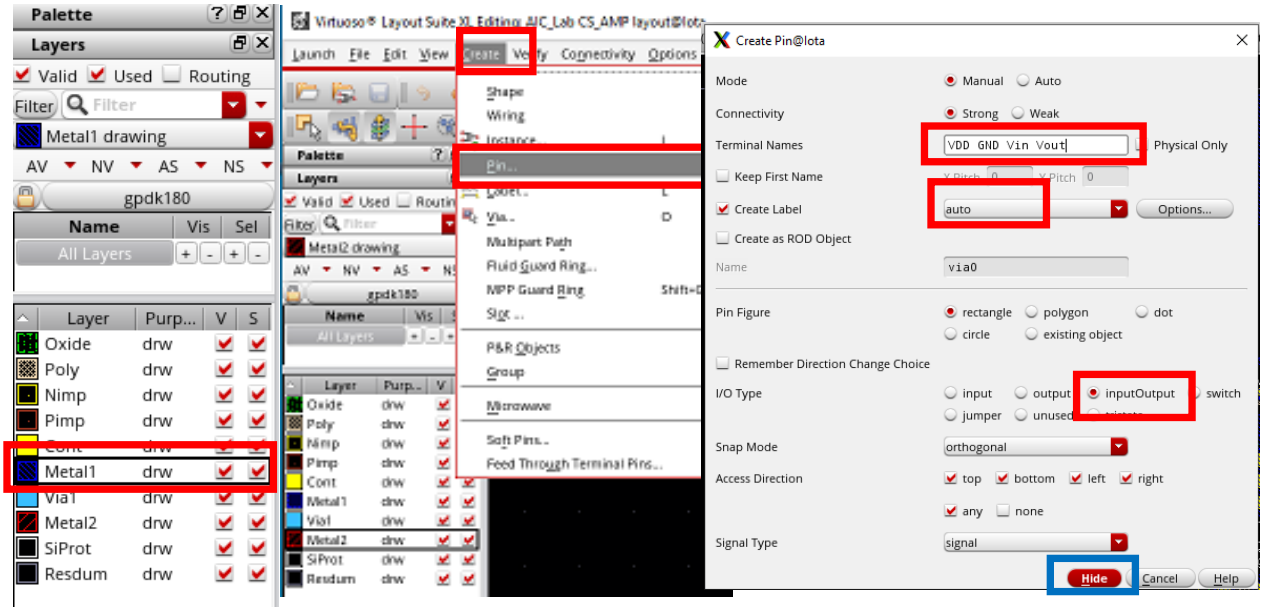


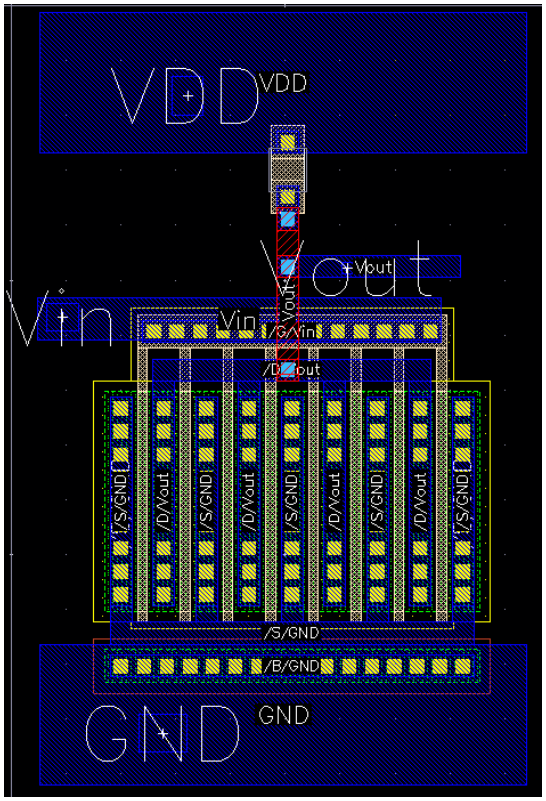
- Draw Vout layer by using Metal 1 as shown in the figure below.



7. Place a Pin

- To place pins (VDD, GND, Vin, and Vout) in the layout,
- Select “Metal 1” in Layers windows → “Create” → “Pin”
- Terminal Names: VDD GND Vin Vout
- Make a rectangle using the left mouse button
- Make sure save the layout



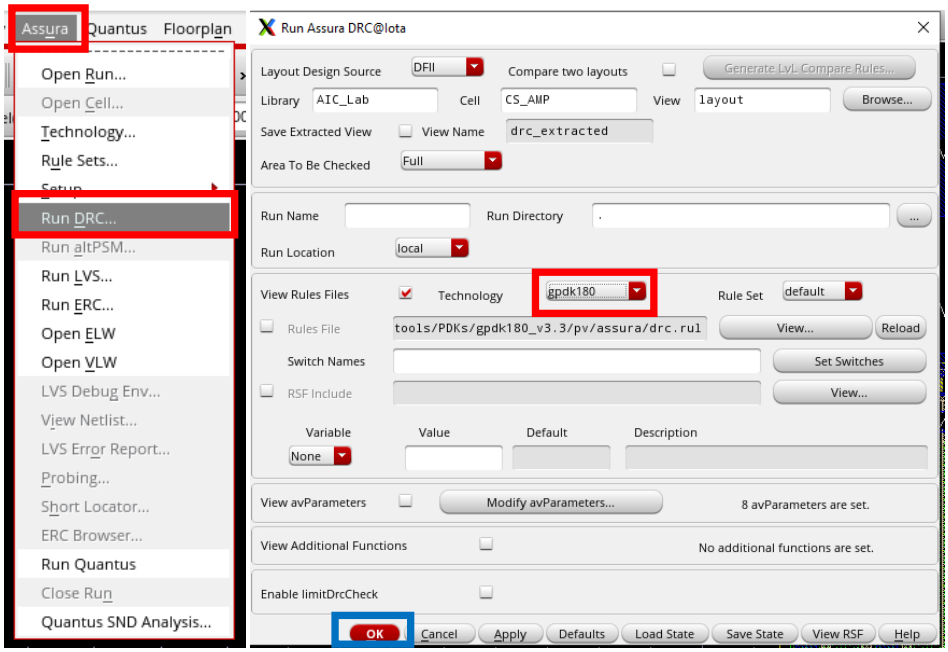


- All pin names in the layout and schematic must be matched to pass LVS.

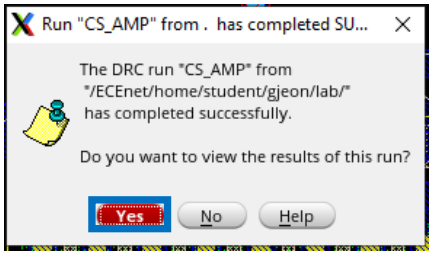
Verification

1. DRC (Design Rule Check)

- To check design rule in the layout,
- Select “Assura” → “Run DRC”

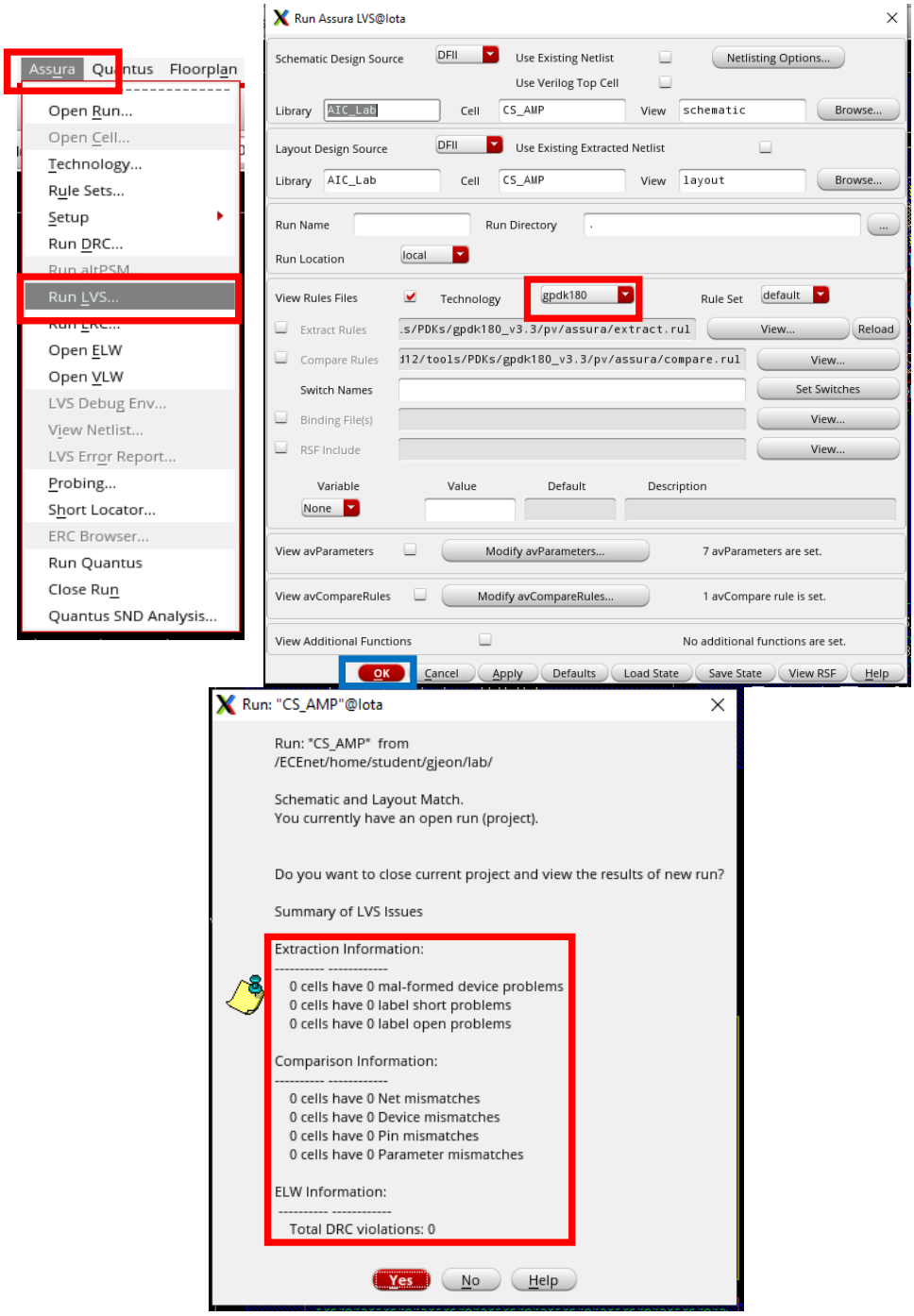


- If your layout does not violate any rules, you will get “No DRC errors Found” message.



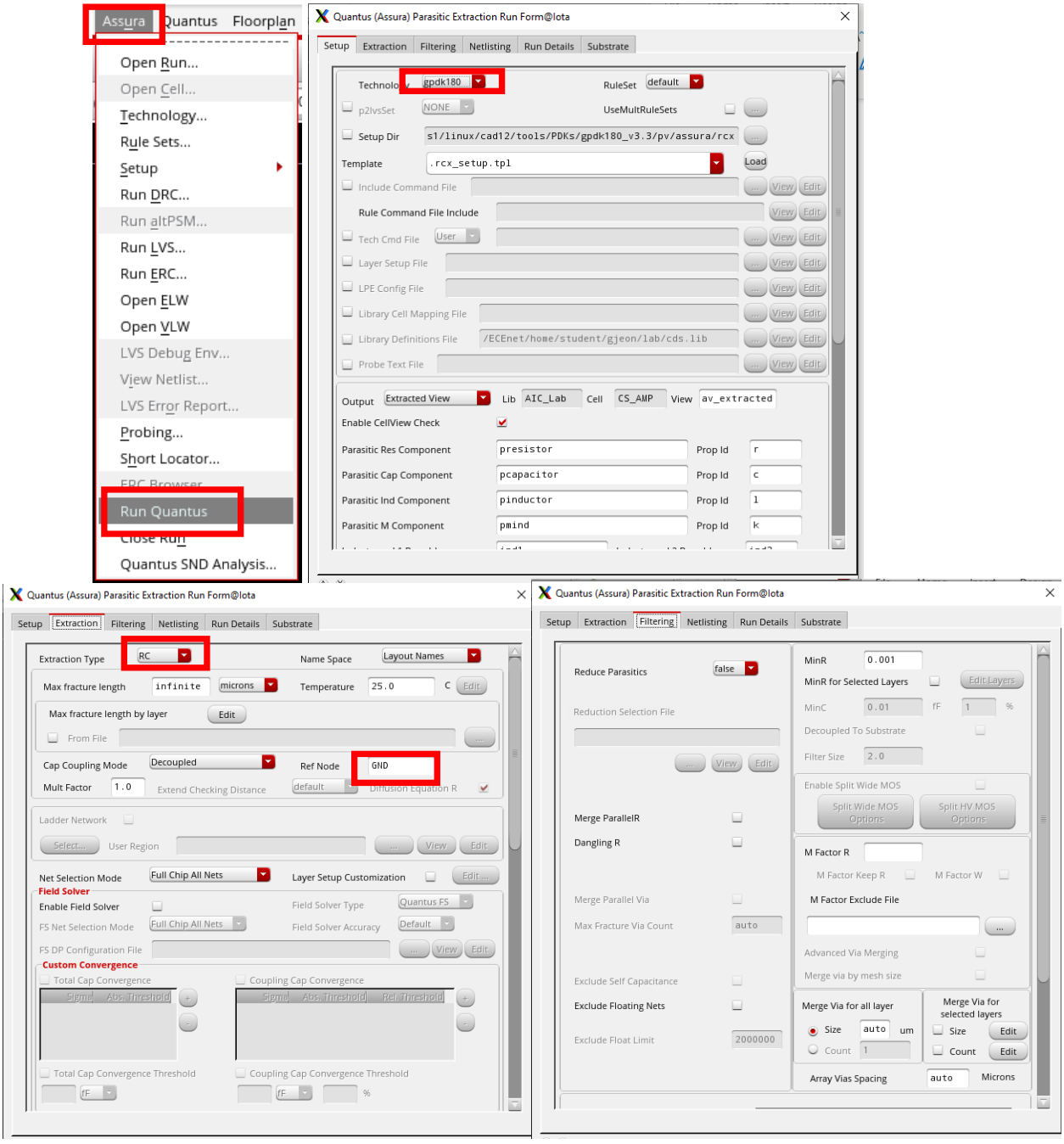
2. LVS (Layout VS Schematic)

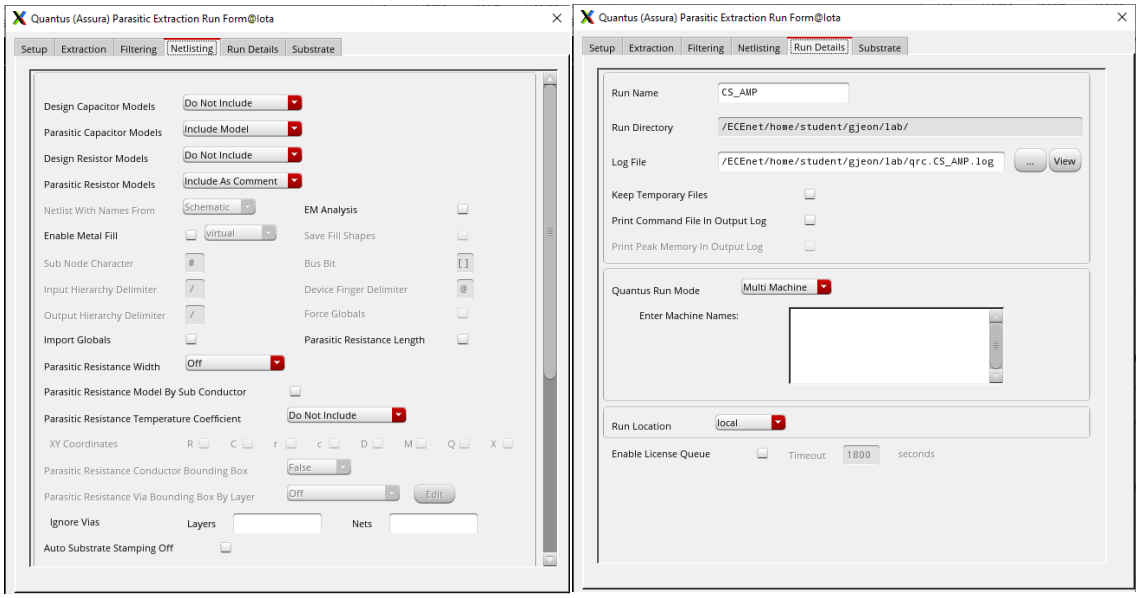
- To check LVS simulation,
- Select “Assura” → “Run LVS”



3. Parasitic Extraction (QRC)

- To extract parasitic RC of the metal layers,
- Select “Assura” → “Run Quantus”
- After checking all the red boxes, select “Ok”




Quantus (Assura) Parasitic Extraction Run Form@lota
Setup
Extraction
Filtering
Netlisting
Run Details
Substrate
Design Capacitor Models
Do Not Include
Parasitic Capacitor Models
Include Model
Design Resistor Models
Do Not Include
Parasitic Resistor Models
Include As Comment
Netlist With Names From
Schematic
EM Analysis
Enable Metal Fill
virtual
Save Fill Shapes
Sub Node Character
#
Bus Bit
[ ]
Input Hierarchy Delimiter
/
Device Finger Delimiter
@
Output Hierarchy Delimiter
/
Force Globals
Import Globals
Parasitic Resistance Length
Parasitic Resistance Width
Off
Parasitic Resistance Model By Sub Conductor
Parasitic Resistance Temperature Coefficient
Do Not Include
XY Coordinates
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Parasitic Resistance Conductor Bounding Box
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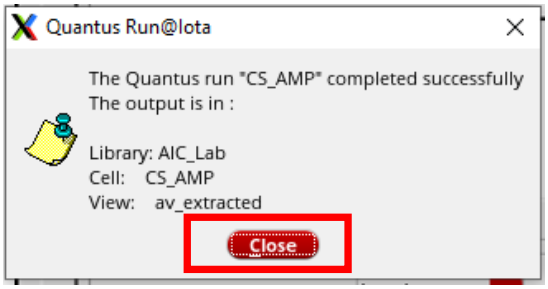
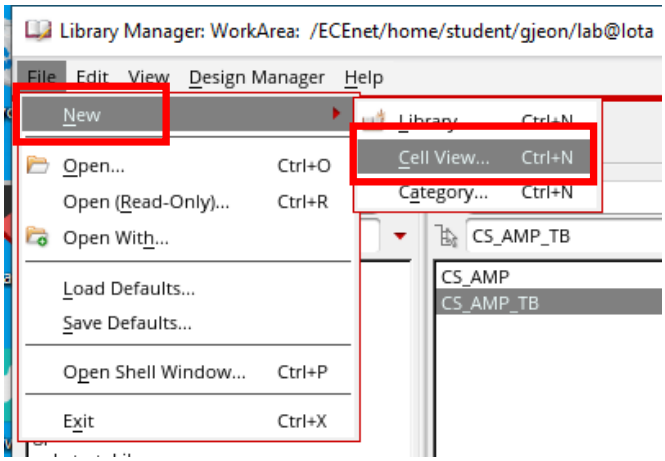
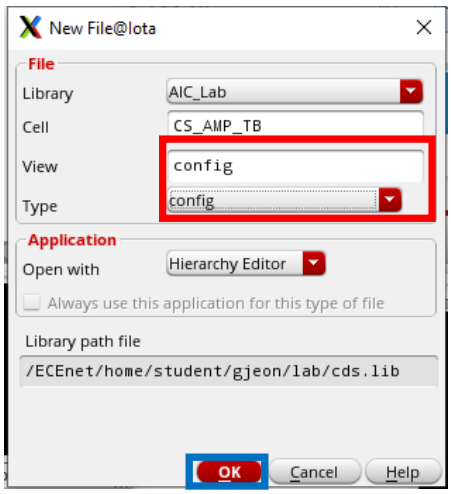
Parasitic Resistance Via Bounding Box By Layer
Off
Edit
Ignore Vias
Layers
Nets
Auto Substrate Stamping Off
Quantus (Assura) Parasitic Extraction Run Form@lota
Setup
Extraction
Filtering
Netlisting
Run Details
Substrate
Run Name
CS_AMP
Run Directory
/ECEnet/home/student/gjeon/lab/
Log File
/ECEnet/home/student/gjeon/lab/qrc.CS_AMP.log
...
View
Keep Temporary Files
Print Command File In Output Log
Print Peak Memory In Output Log
Quantus Run Mode
Multi Machine
Enter Machine Names:
Run Location
local
Enable License Queue
Timeout
1800
seconds


Quantus Run@lota
The Quantus run "CS_AMP" completed successfully
The output is in :
Library: AIC_Lab
Cell: CS_AMP
View: av_extracted
Close

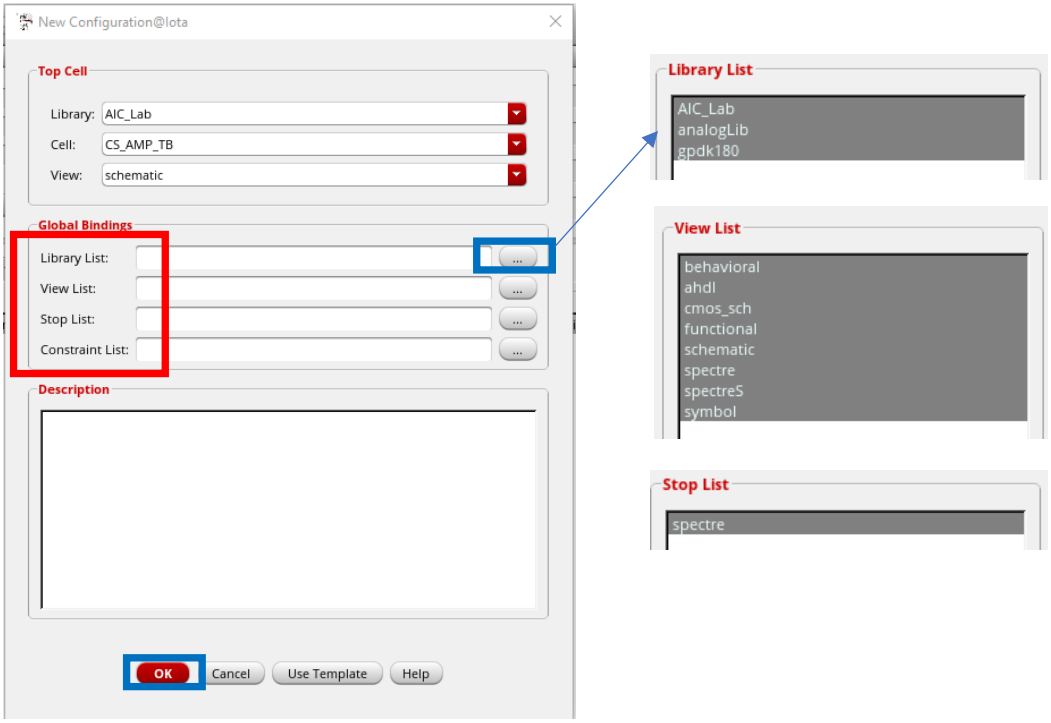
4. Post-Simulation

- The parasitic RC are implemented in the av_extracted.
- To use the parasitic RC in the simulation,
- Select “File” in library manager → “New” → “Cell View” → “config” in the view

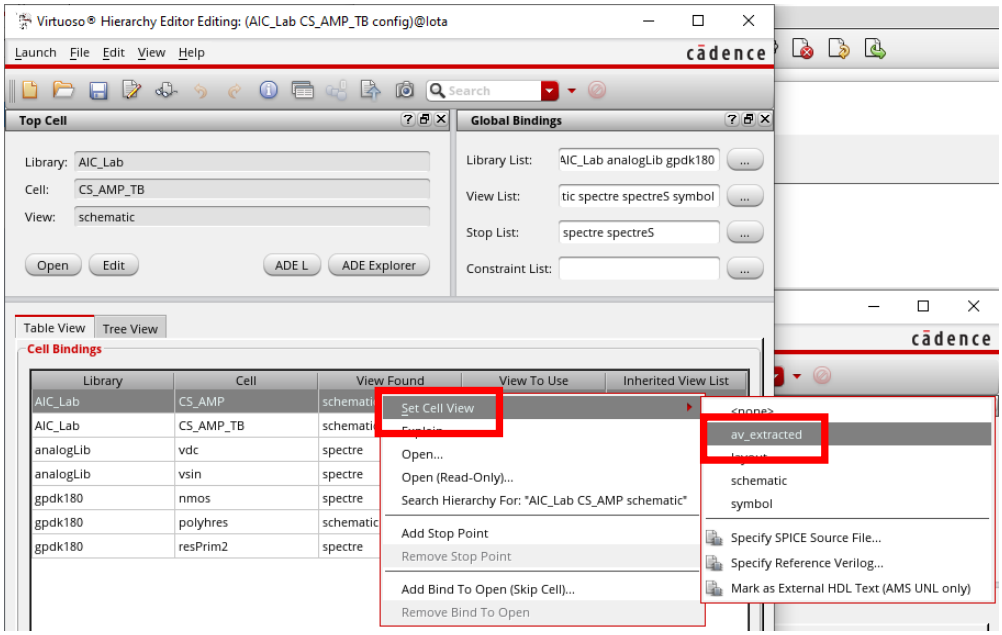




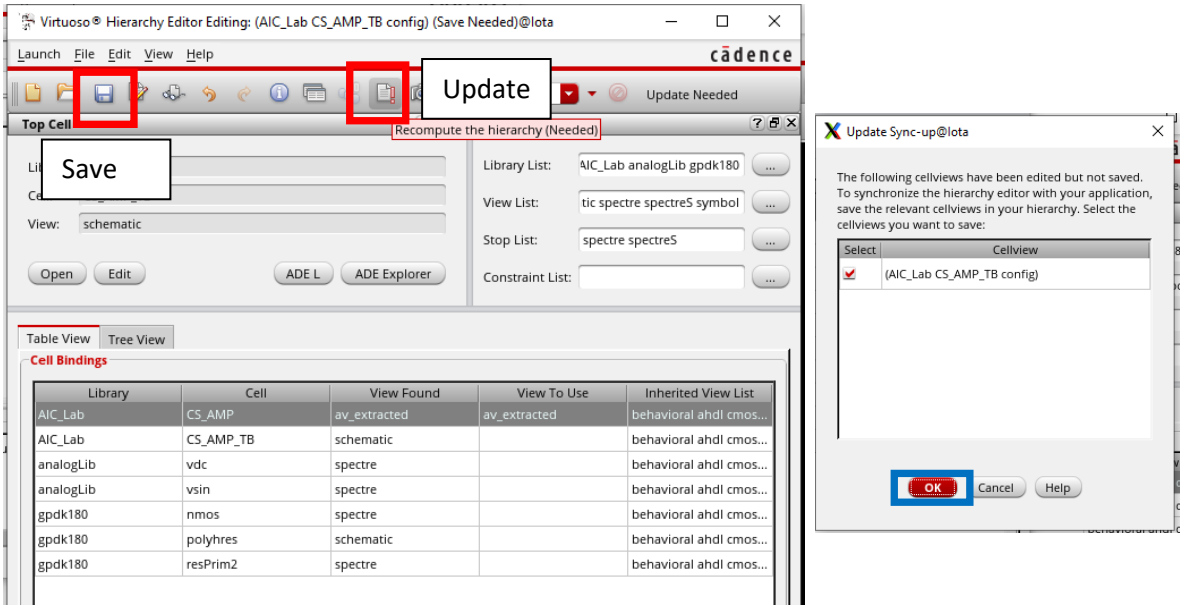
- Select following lists in the configuration window as shown in the figure below.



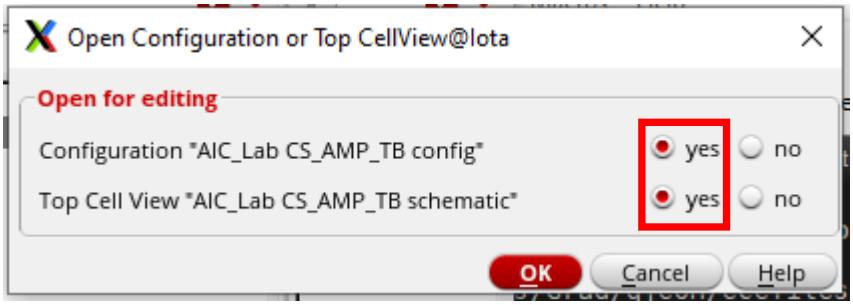
- All components in the schematic of CS_AMP_TB are listed in the table view.
- Change the CS_AMP from “schematic” to “av_extracted” view
- Select CS_AMP → “Right mouse click” → “Set Cell view” → “av_extracted”



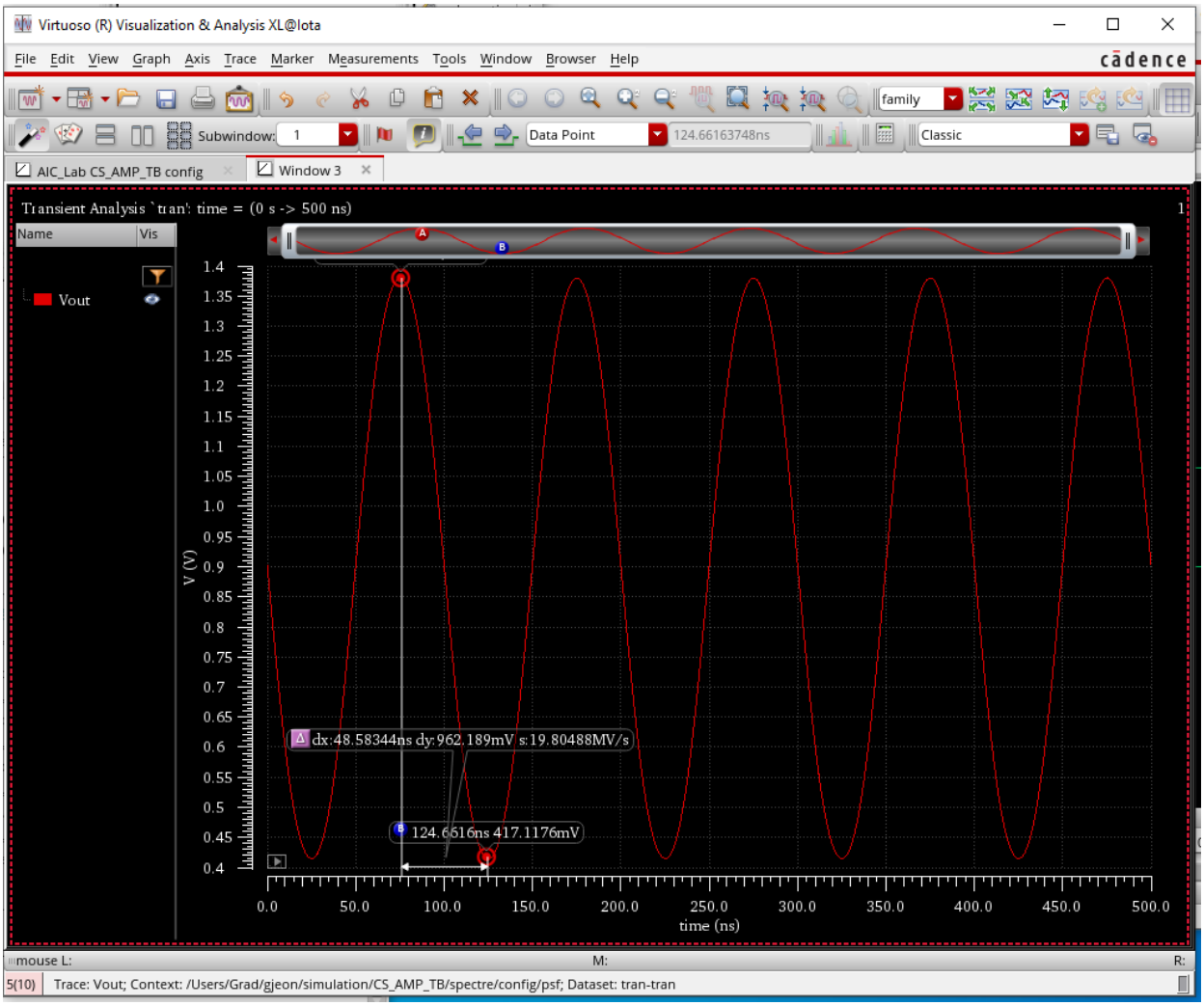
- Updates the table view by clicking the icon below and save the configuration

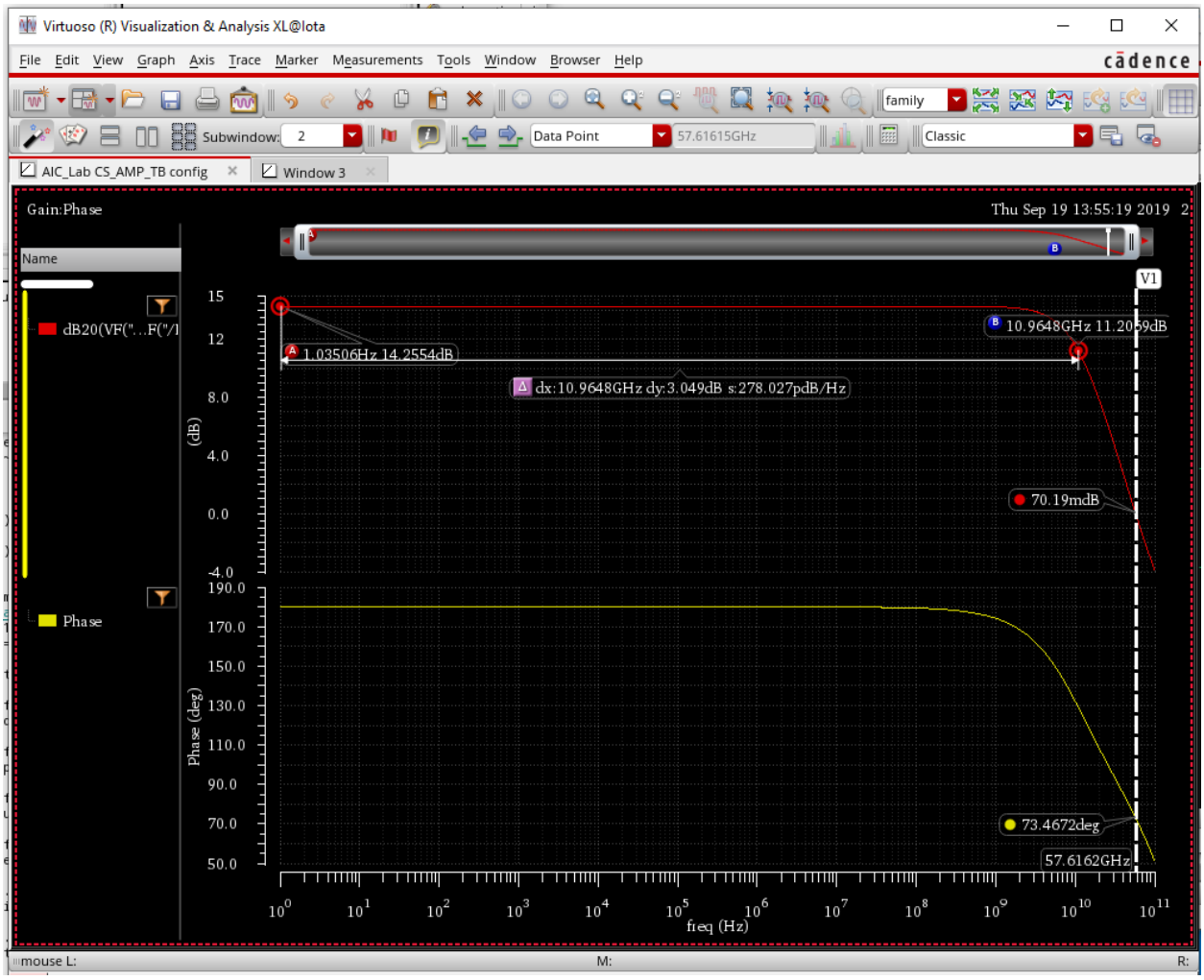


- Close the config window and re-open it
- In library manager, Select “AIC_Lab(Library)” → “config” in CS_AMP_TB



- Two windows, Config and schematic are opened
- Select “Launch” → “ADE L” in schematic window
- In ADE L window, select “Session” → “Load state”
- Run the simulation in the ADE L, select “Simulation” → “Netlist and Run”




Virtuoso (R) Visualization & Analysis XL@lota
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindow: 2
Data Point
57.61615GHz
Classic
AIC_Lab CS_AMP_TB config
Window 3
Gain:Phase
Thu Sep 19 13:55:19 2019
Name
dB20(VF("...F("/I
Phase
V1
10.9648GHz 11.2059dB
1.03506Hz 14.2554dB
dx:10.9648GHz dy:3.049dB s:278.027pdB/Hz
70.19mdB
73.4672deg
57.6162GHz
(dB)
Phase (deg)
freq (Hz)
mouse L:
M:
R: