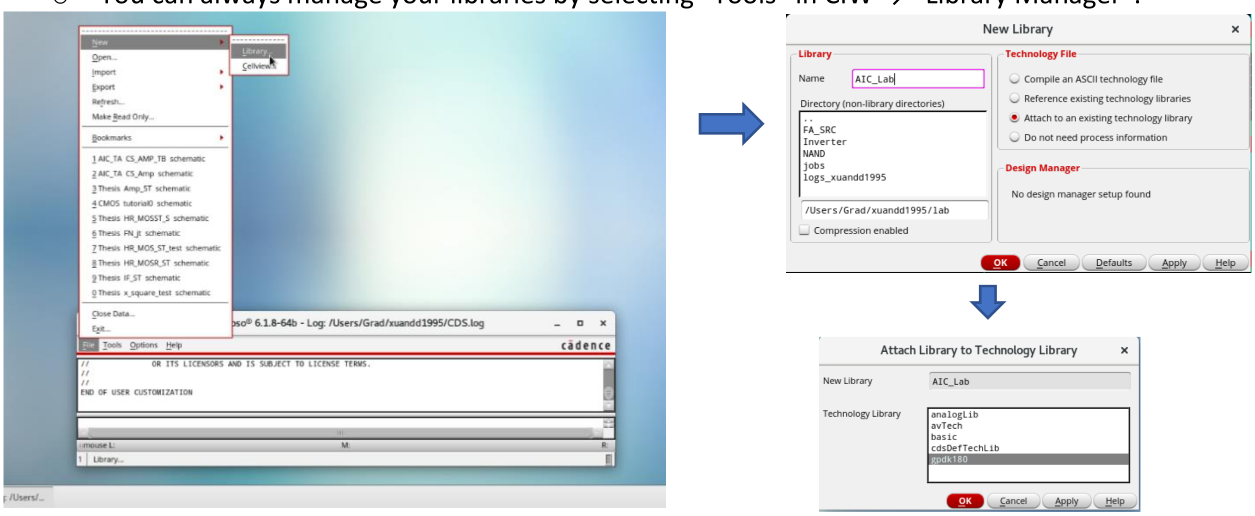
# EECE7248 Lab Tutorial: Common-Source Amplifier Schematic

Yixuan He, Gyunam Jeon, Yong-Bin Kim

This tutorial briefly introduces the circuit simulation in Cadence. A simple common-source amplifier has been built and simulated step by step using schematic entry.

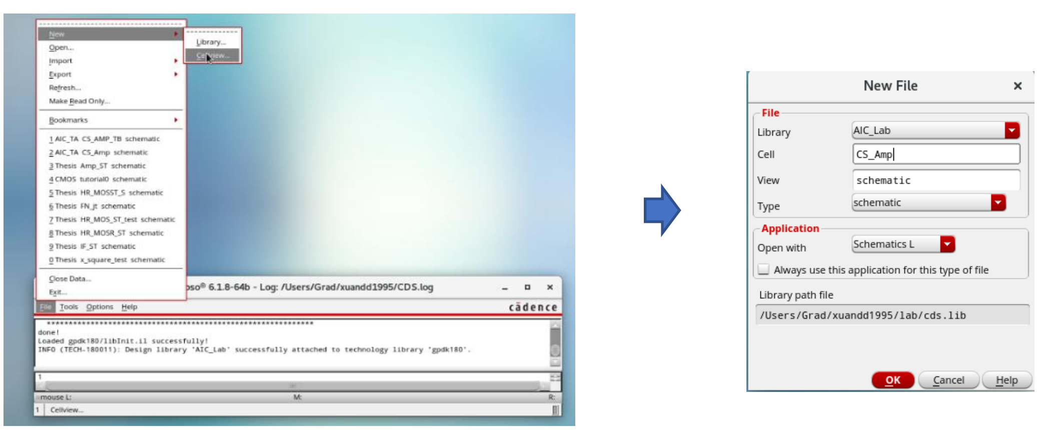
## 1. Create New Library

- Select "File" in CIW → "New" → "Library" to create a new library with an arbitrary name. *Don't forget to select "Attach to an existing technology library"!!!
- You can always manage your libraries by selecting "Tools" in CIW → "Library Manager".




## 2. Create New Cellview

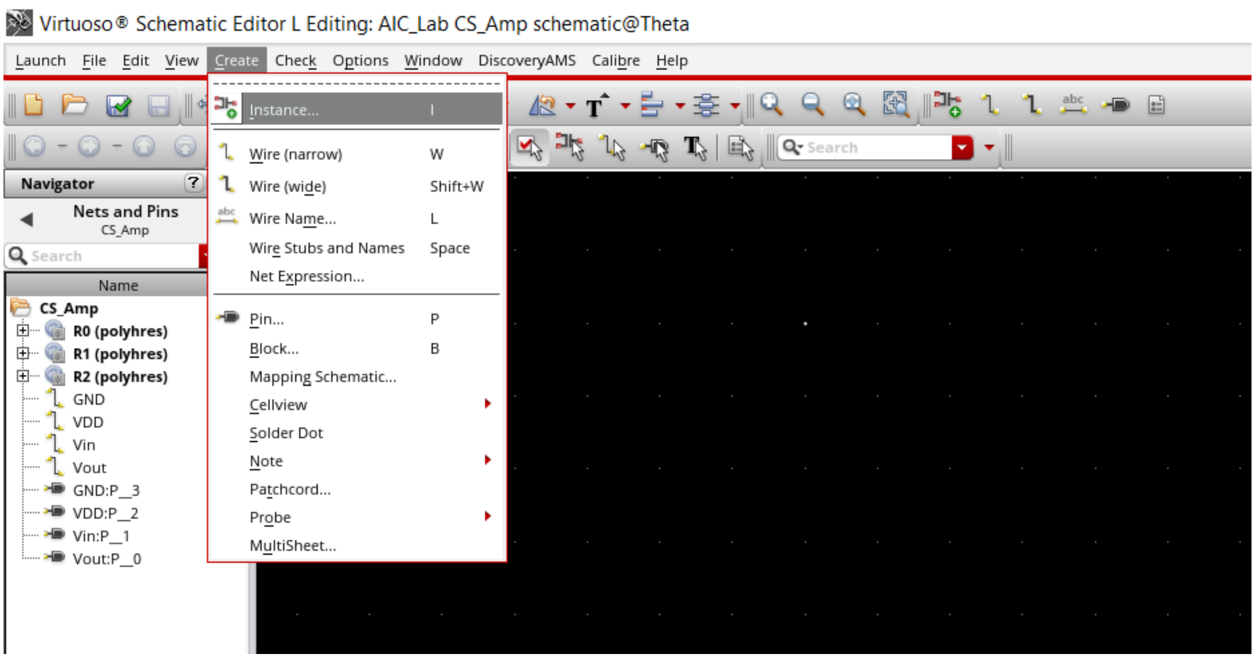
- Select "File" → "New" → "Cellview" to create a new cellview under the library you just created. A new window will show up which allows you to draw your circuit schematic.

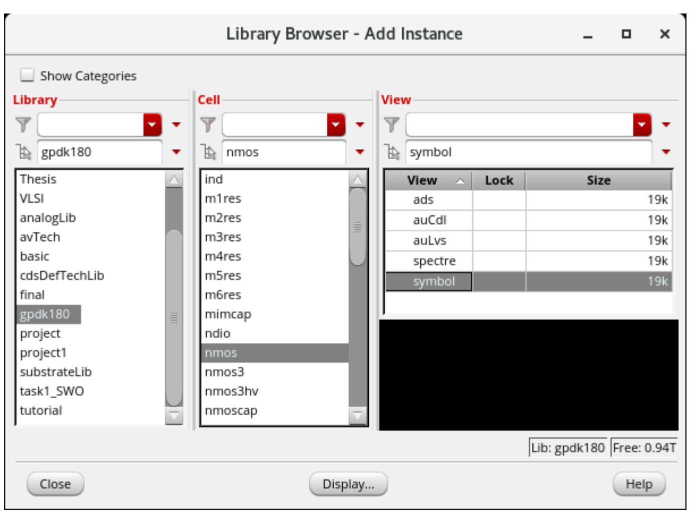


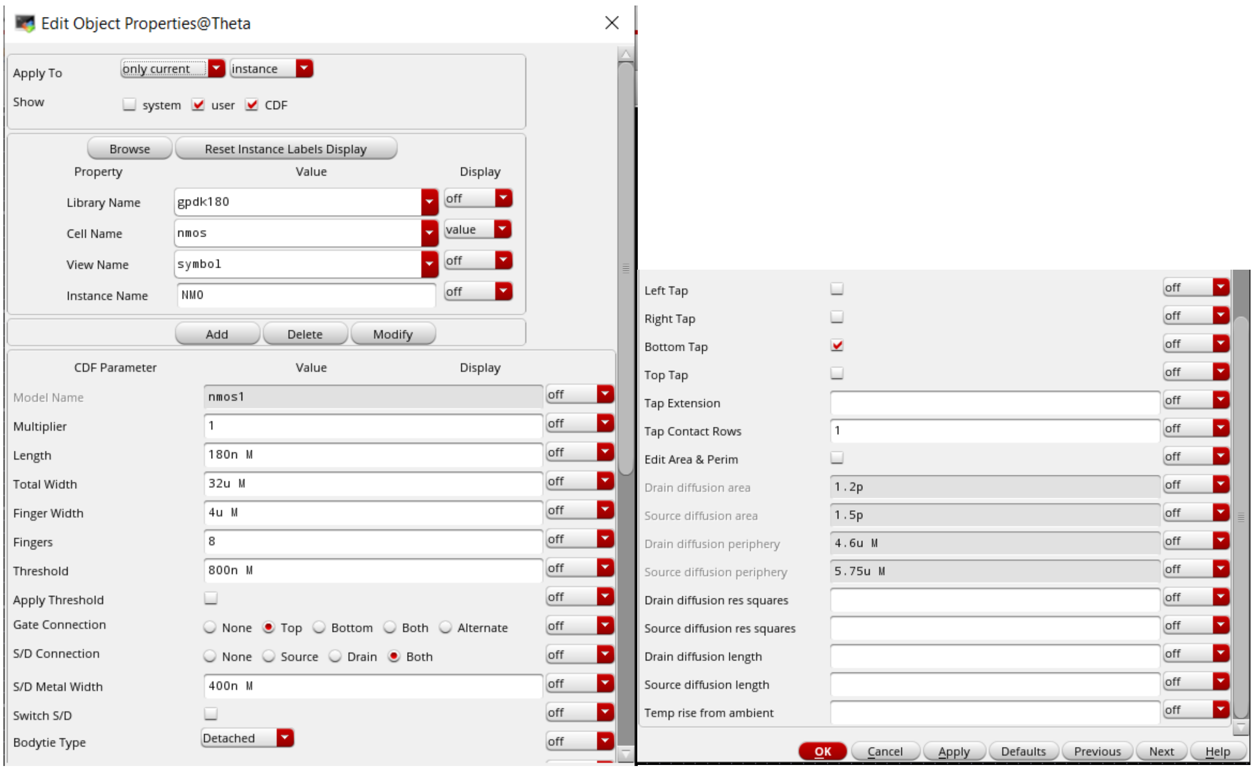
## 3. Build Schematic

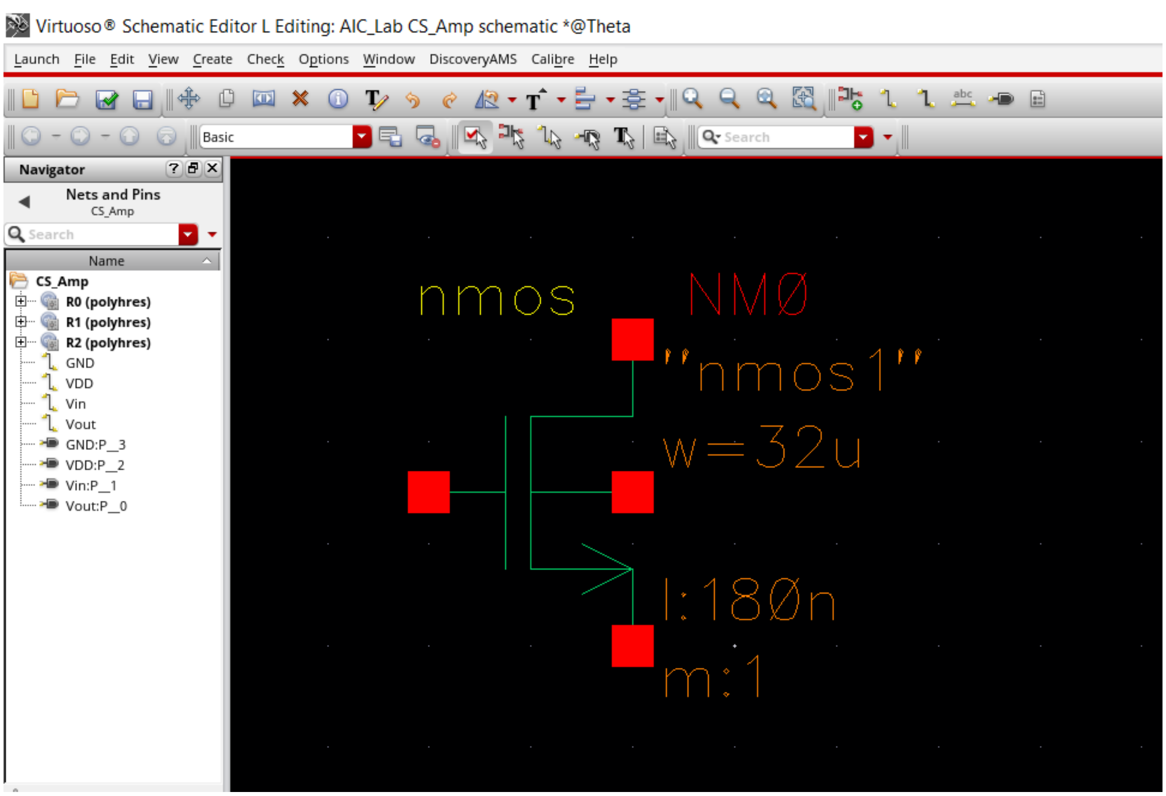
- Add instances: Select “Create” → “Instance” (or simply use shortcut: i) to open “Add Instance” window, then click “Browse”. Now you can select different instances from certain libraries and change their parameters (Select gpdk180, nmos, symbol to add a NMOS for example).
- Place the instances in the schematic window (left mouse click).
- To change parameters of a certain instance that you have placed, select that instance(left mouse click) in schematic and right click to select “Proprties”(shortcut: q).

*The screenshots below show the steps to add a NMOS transistor from gpdk180 library.

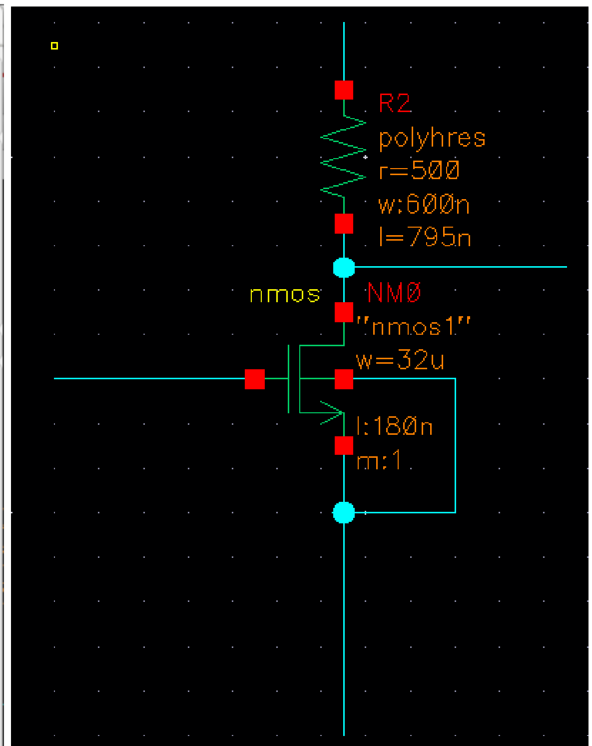


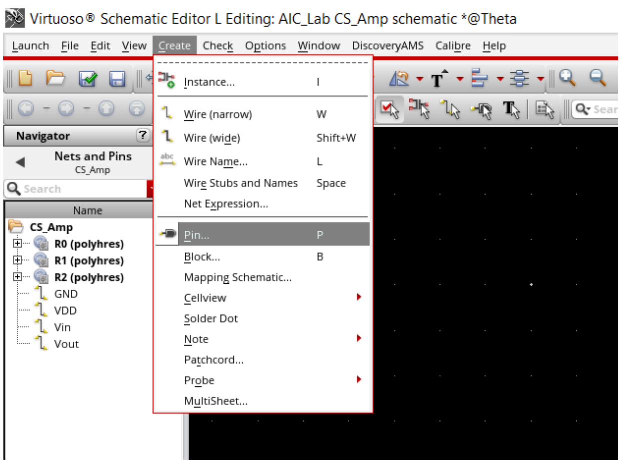

Edit Object Properties@Theta
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
gpdk180
off
Cell Name
nmos
value
View Name
symbol
off
Instance Name
NM0
off
Add
Delete
Modify
CDF Parameter
Value
Display
Model Name
nmos1
Multiplier
1
Length
180n M
Total Width
32u M
Finger Width
4u M
Fingers
8
Threshold
800n M
Apply Threshold
Gate Connection
None
Top
Bottom
Both
Alternate
S/D Connection
None
Source
Drain
Both
S/D Metal Width
400n M
Switch S/D
Bodytie Type
Detached
Left Tap
Right Tap
Bottom Tap
Top Tap
Tap Extension
Tap Contact Rows
1
Edit Area & Perim
Drain diffusion area
1.2p
Source diffusion area
1.5p
Drain diffusion periphery
4.6u M
Source diffusion periphery
5.75u M
Drain diffusion res squares
Source diffusion res squares
Drain diffusion length
Source diffusion length
Temp rise from ambient
OK
Cancel
Apply
Defaults
Previous
Next
Help

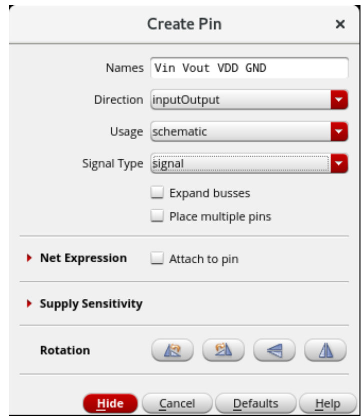

Virtuoso® Schematic Editor L Editing: AIC_Lab CS_Amp schematic *@Theta
Launch
File
Edit
View
Create
Check
Options
Window
DiscoveryAMS
Calibre
Help
Basic
Search
Navigator
Nets and Pins
CS_Amp
Search
Name
CS_Amp
R0 (polyhres)
R1 (polyhres)
R2 (polyhres)
GND
VDD
Vin
Vout
GND:P__3
VDD:P__2
Vin:P__1
Vout:P__0
nmos
NM0
"nmos1"
w=32u
l:180n
m:1

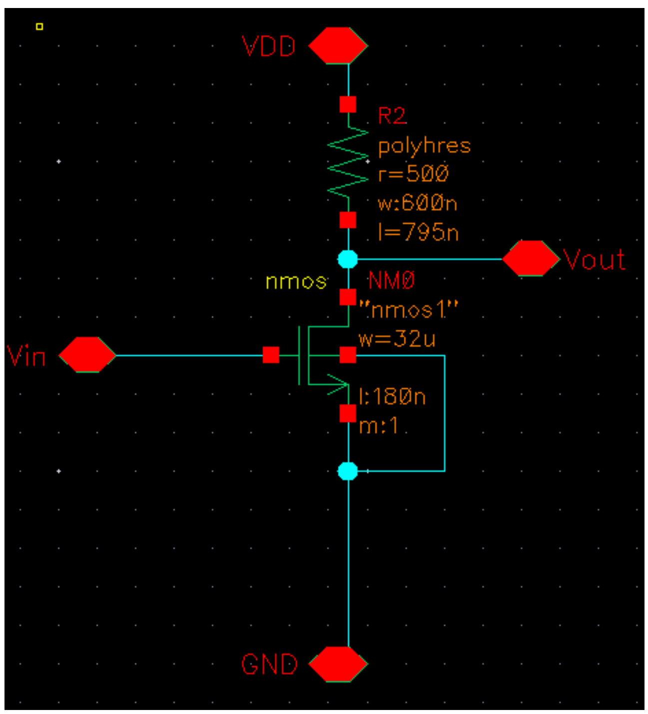
- Other instances' properties of the amplifier are listed below. You can place them into the schematic in the same way.
- Use wire (shortcut: w) to connect them together appropriately (Press "w" and select the two ports you want to connect). And the schematic is shown below.

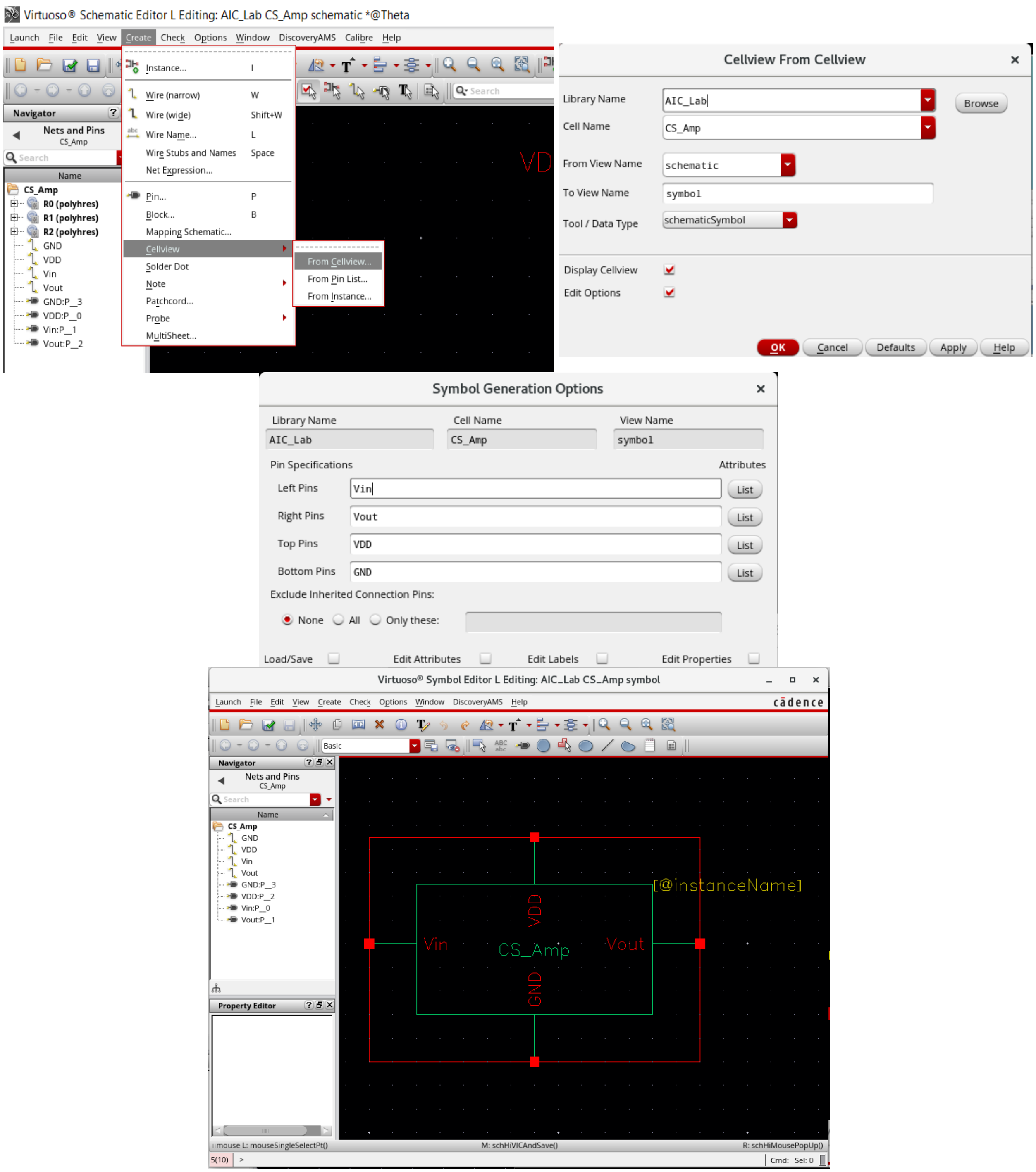
- Add pins: Select "Create" → "Pin" (shortcut: p) → enter pins' name and select "inputOutput" option → place them by left clicking on the correct net in schematic. Those pins will show up in your amplifier instance later when you create its symbol.



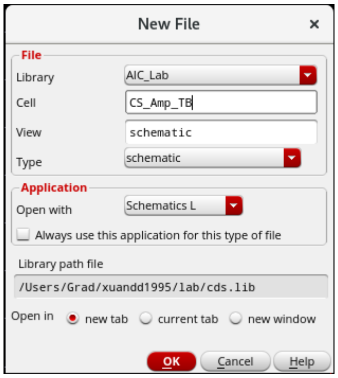



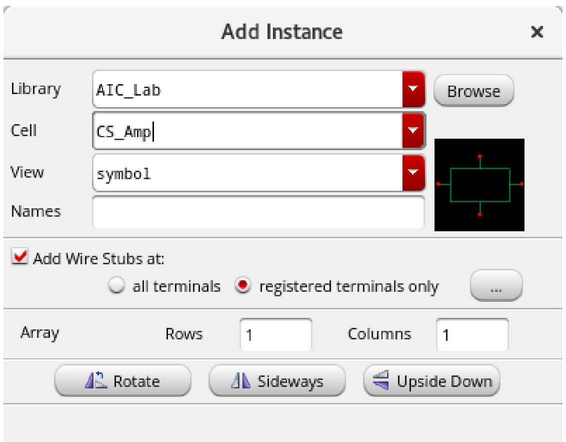
- Select “File” → “Check and Save” (shortcut: shift + x) to detect errors and save your design. Make sure you have done that before simulation.
- Create a new instance for the amplifier. After this step, your amplifier circuit will become an instance that can be found in its library. It allows you to add this amplifier as a single block in other schematic or testbench.
- As it shows below, a symbol has been created. You can change its pins, shape and name in this window. Then, check and save (shift + x) and close it after you finish all the modification.
-

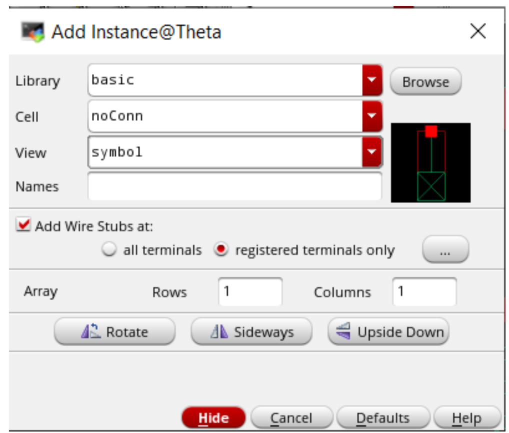


- Create a new cellview for testbench.

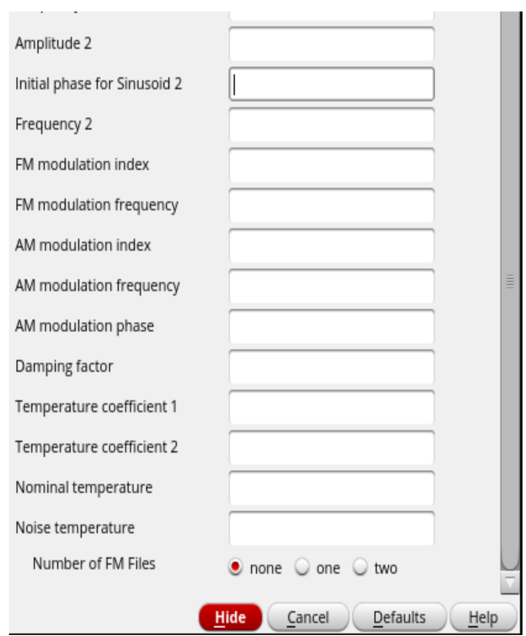


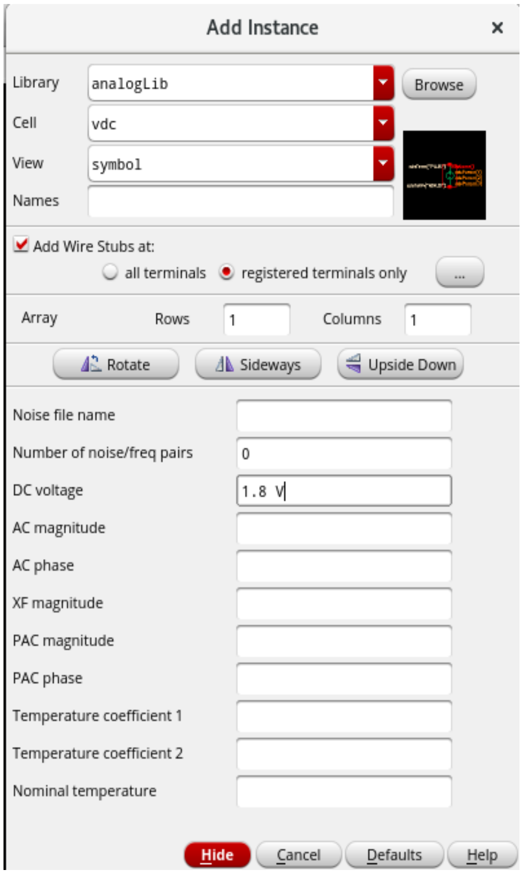

- Add following instances and connect them together. Their parameters and the final schematic are shown below.

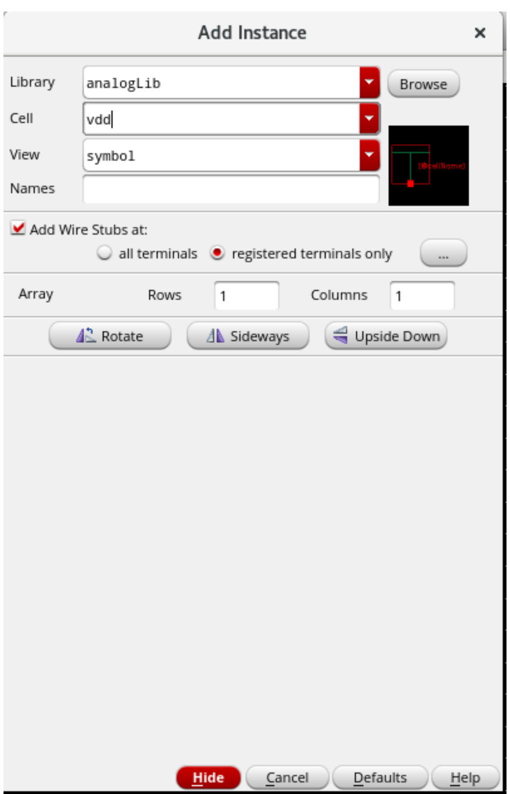


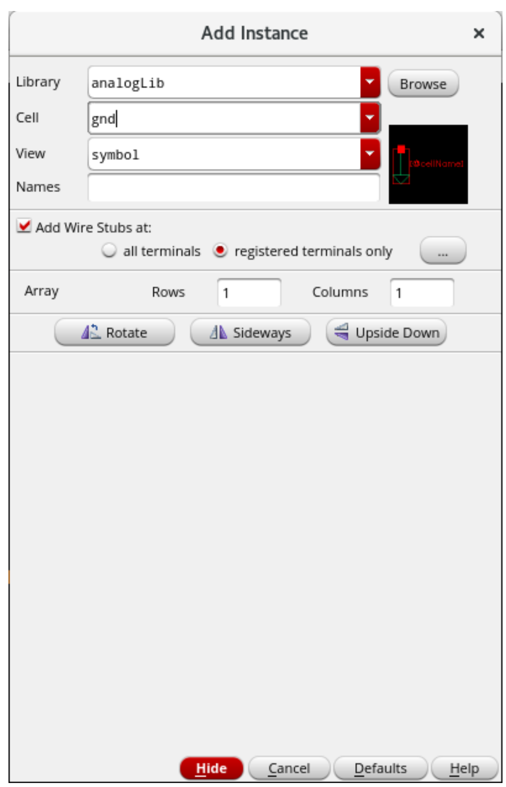





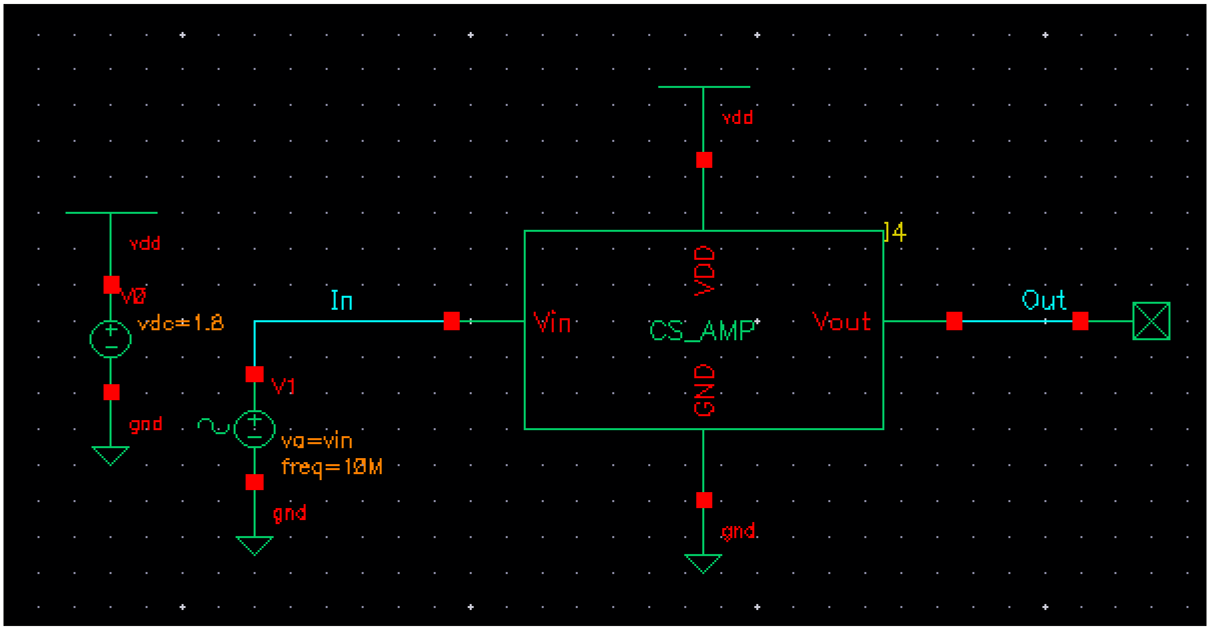



Add Instance
Library
analogLib
Browse
Cell
vdc
View
symbol
Names
Add Wire Stubs at:
all terminals
registered terminals only
...
Array
Rows
1
Columns
1
Rotate
Sideways
Upside Down
Noise file name
Number of noise/freq pairs
0
DC voltage
1.8 V
AC magnitude
AC phase
XF magnitude
PAC magnitude
PAC phase
Temperature coefficient 1
Temperature coefficient 2
Nominal temperature
Hide
Cancel
Defaults
Help


Add Instance
Library
analogLib
Browse
Cell
vdd
View
symbol
Names
Add Wire Stubs at:
all terminals
registered terminals only
...
Array
Rows
1
Columns
1
Rotate
Sideways
Upside Down
Hide
Cancel
Defaults
Help


Add Instance
Library
analogLib
Browse
Cell
gnd
View
symbol
Names
Add Wire Stubs at:
all terminals
registered terminals only
...
Array
Rows
1
Columns
1
Rotate
Sideways
Upside Down
Hide
Cancel
Defaults
Help

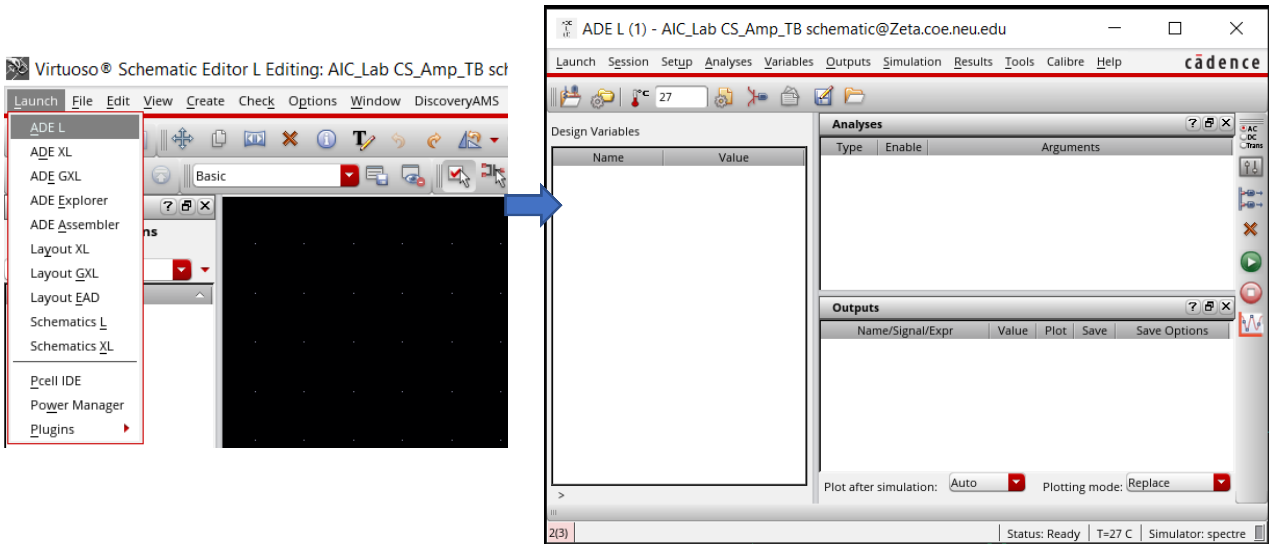
- Add labels: Select “Create” → “Wire Name” (shortcut: “l”) → enter nets’ names → place them by left clicking on the correct net in schematic. Giving two nets a same name connects them together. It’s more convenient when there are lots of wires and crossover points.

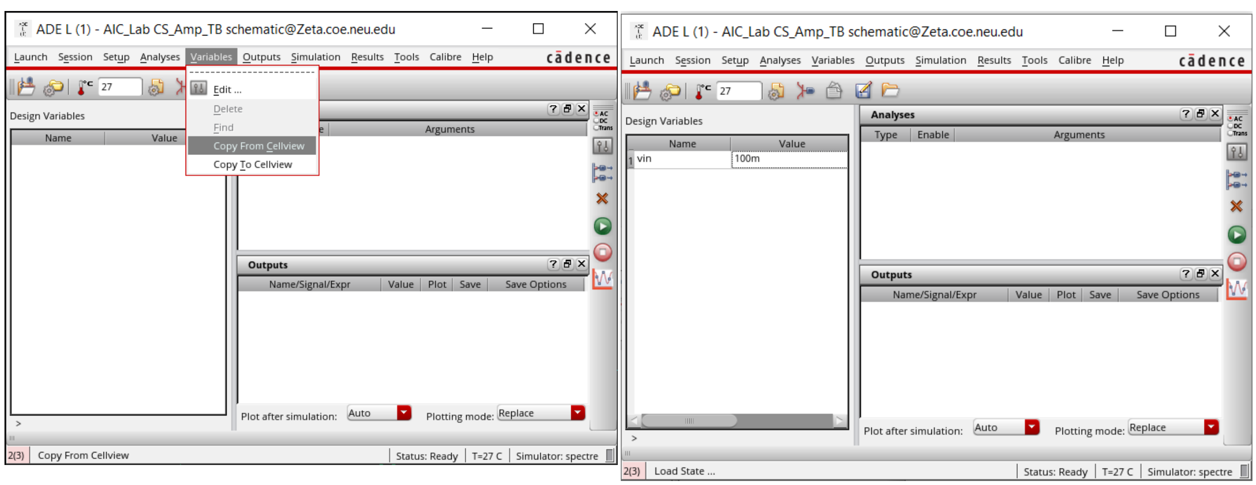


## 4. Schematic Simulation

- Select “Launch” → “ADE L” to open the simulator. It contains three main parts: “Design Variables”, “Analyses” and “Outputs”.

- Set up variables: Select “Variables” from top menu → “Copy From Cellview”. The amplitude of the input voltage source “vin” will show up here in the window. Give it a value (100mV) for simulation later.



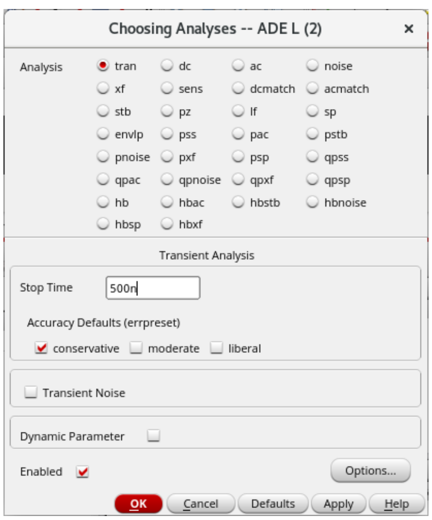
- Set up analyses: Select “Analyses” from top menu → “Choose”. The screenshots below show how to set up transient, DC and AC simulation for the amplifier.
- Set up outputs: There are two ways to get results at output.

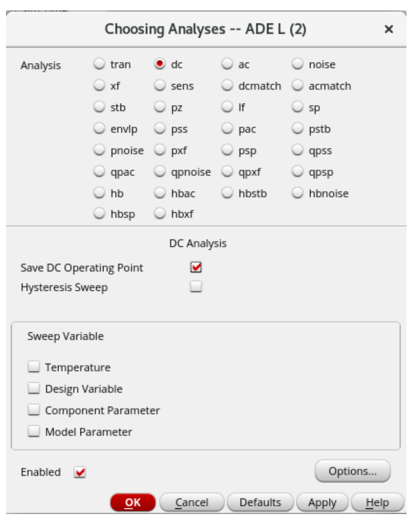
  - Option 1:

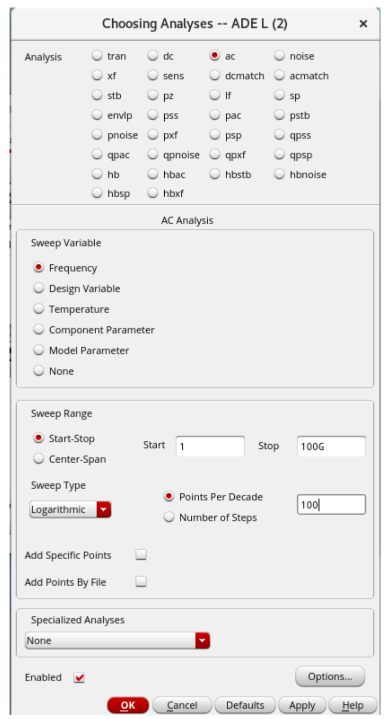
    Select “Outputs” from top menu in ADE L → “Setup”. It will open a window that lets you define the name and expression for the output. In order to get the expression, click “Open” button to open the calculator window. Select signal type and left click on the node in schematic. Its expression will show up so that you can copy it to the “Setting Outputs” window. Then click “Add” to add the output.

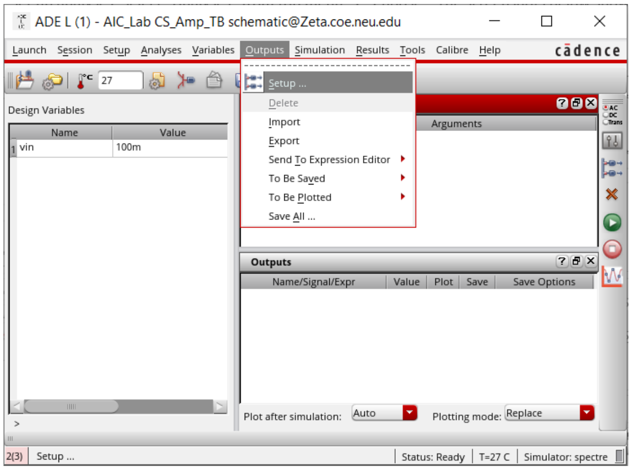
    After you add all the outputs you want, close “Setting Outputs” window and select “Simulation” → “Netlist and Run” to run the simulation (Or click the green button on the right side of ADE L window).

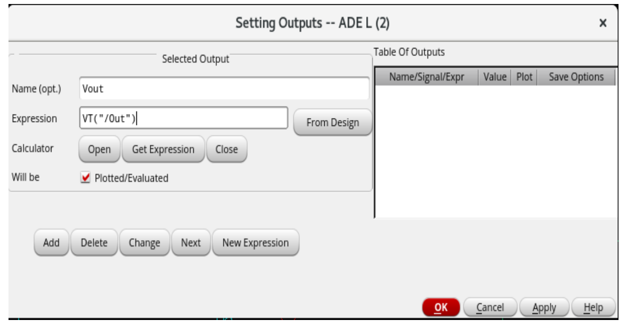
*Expression example: Transient output: VT("/Out"), AC gain: dB20((VF("/Out") / VF("/In"))),
AC phase: phaseDegUnwrapped((VF("/Out") / VF("/In"))).

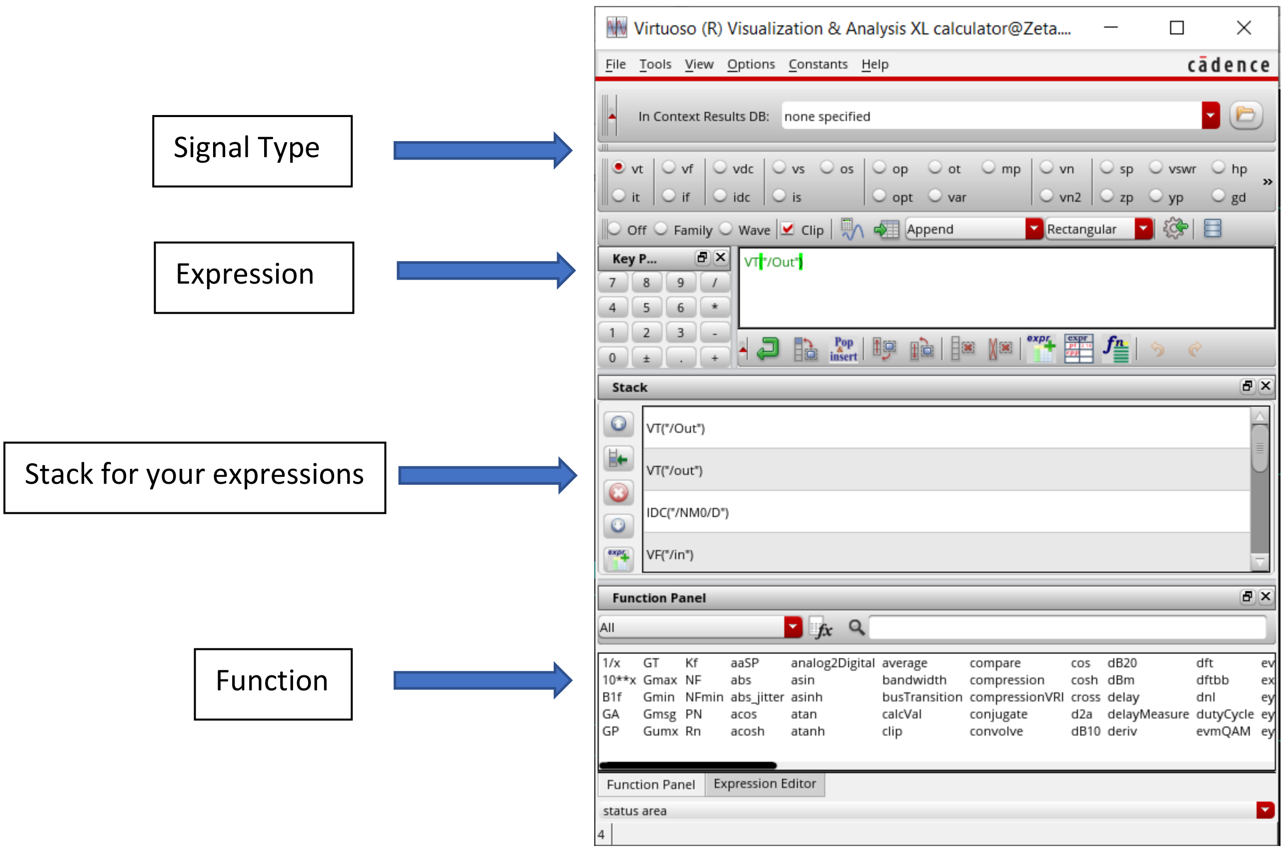




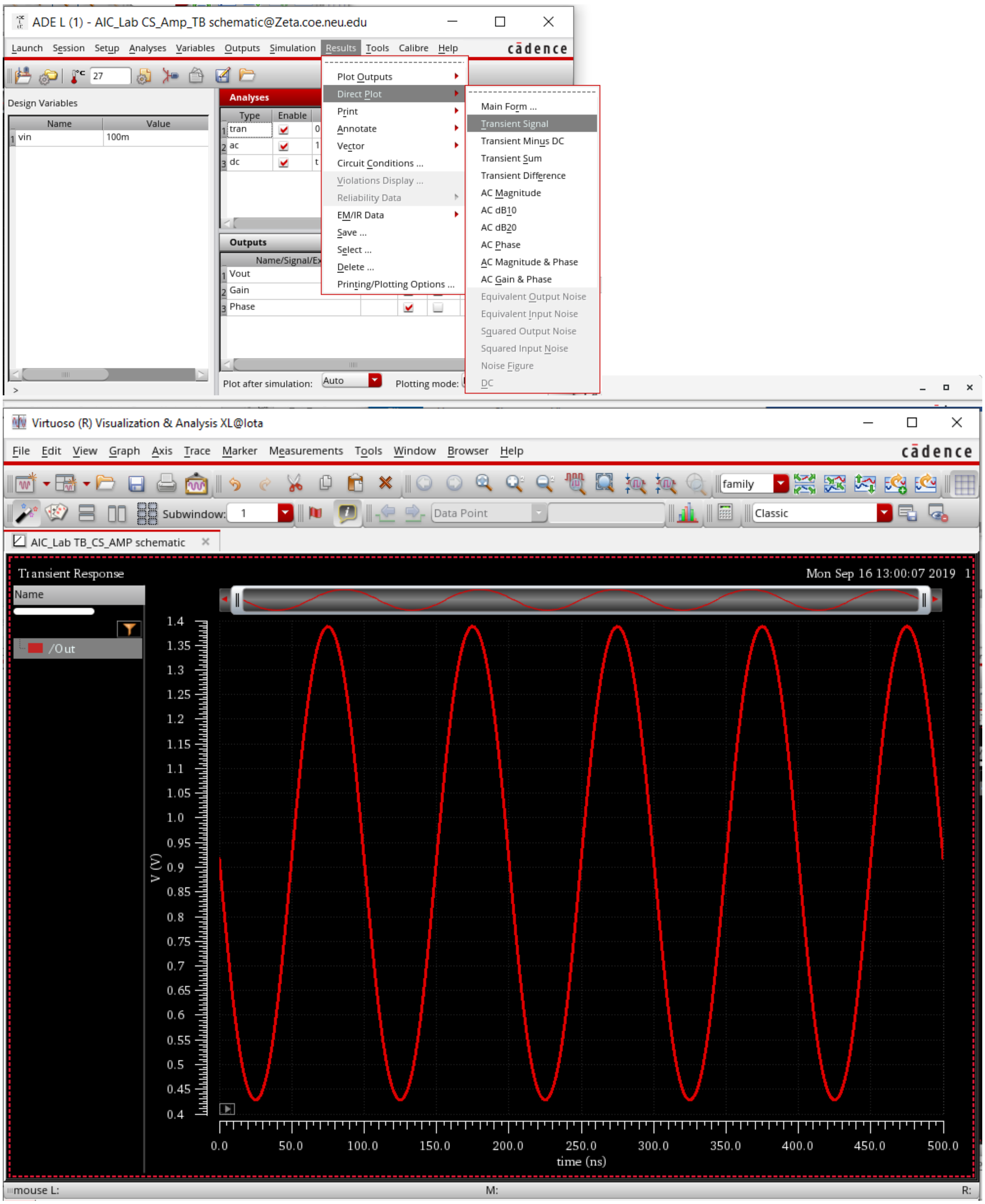




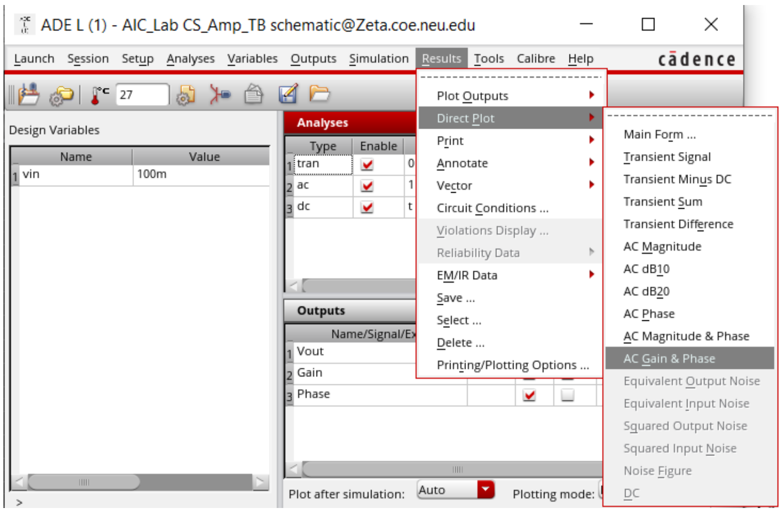

- Option 2:

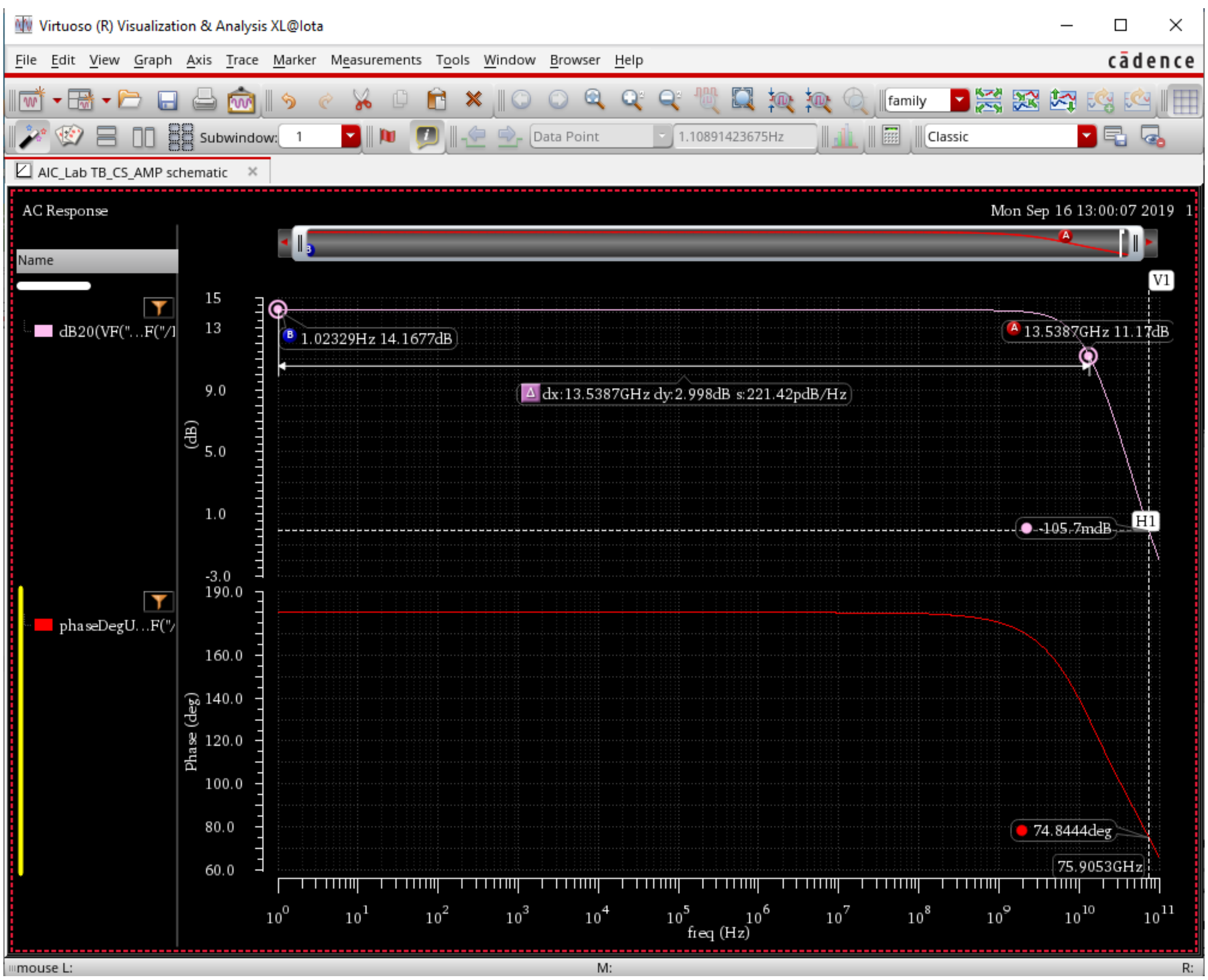
  Run the simulation first, then select “Results” → “Direct Plot” to select signal type and left click the node you want to test in schematic. The node you select will be highlighted. Now press “esc” and the simulator will automatically plot the result for you (For AC gain and phase, choose “AC Gain & Phase” → left click output net in schematic → left click input net in schematic → press “esc”).

- Simulation results:
  - Transient:

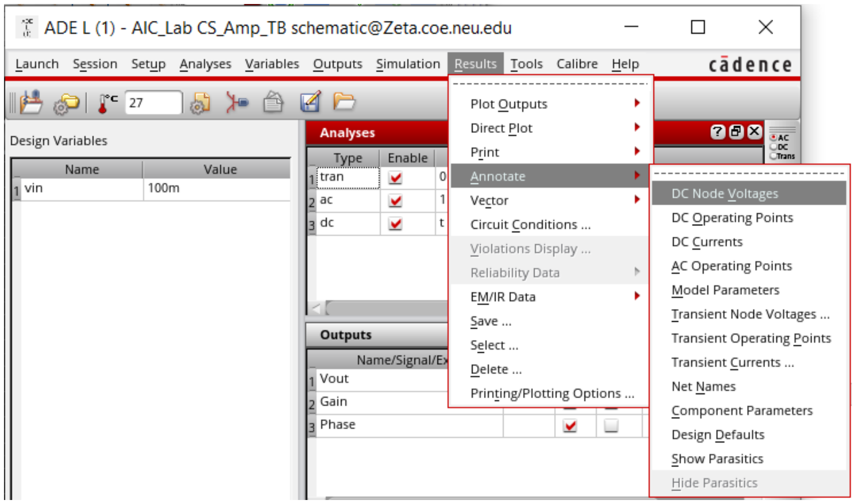


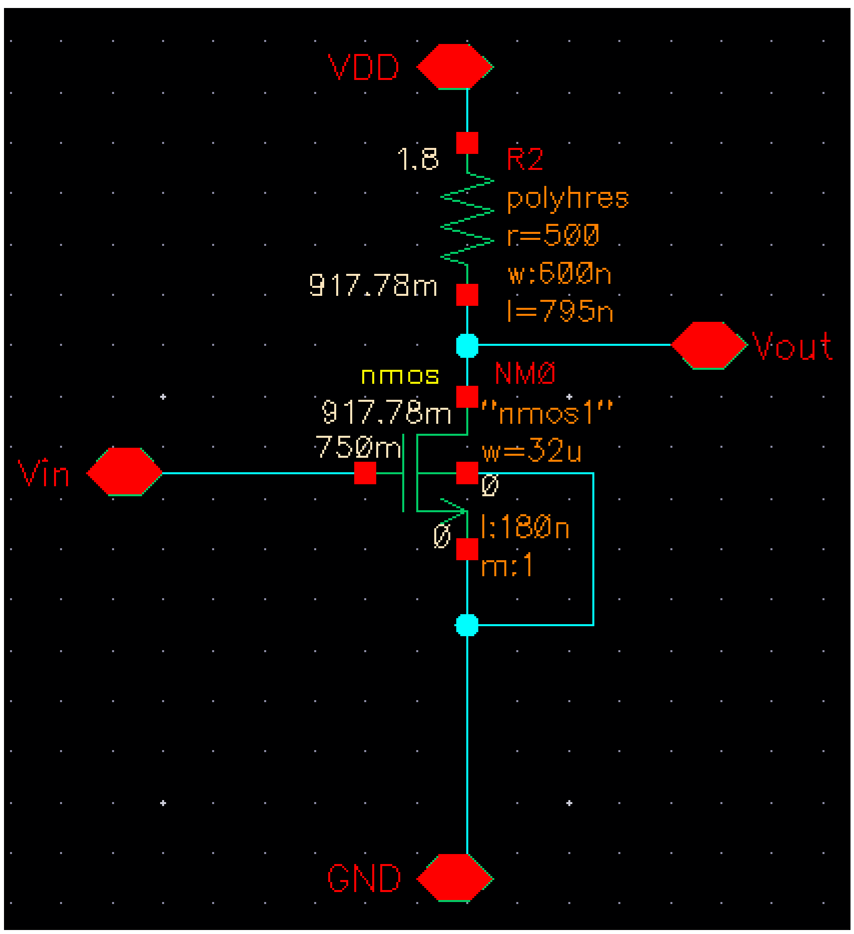
- AC gain and phase:
- Marker: Select “Marker” from top menu in result window → “Create Marker” → left click your trace in result window (shortcut: “m”). To make delta marker, select the first marker and press “d” on trace to create a delta marker. The differences between two points will display.



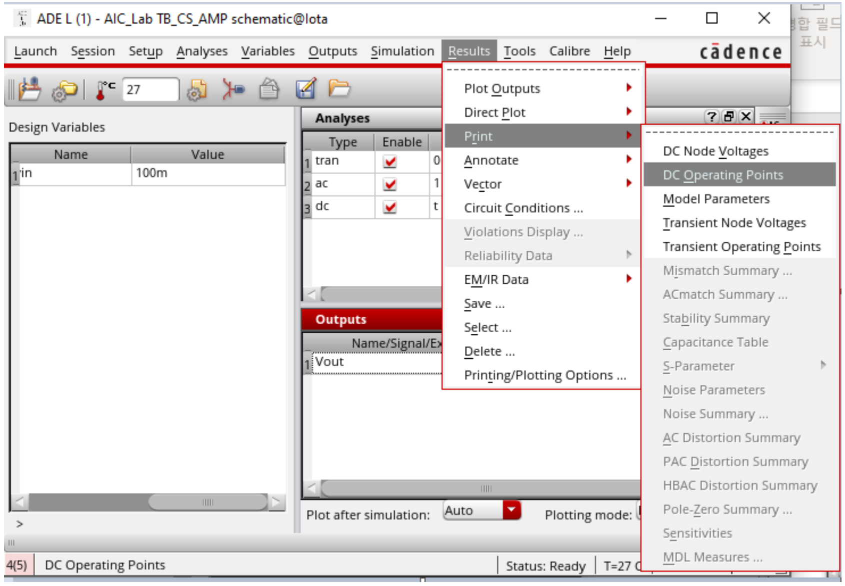



- Annotation: To make life easier, we can annotate nodes in schematic after simulation to show data like DC operating point, current, transistor parameters, etc. Just select “Results” → “Annotate” → “DC Node Voltages” (for example).



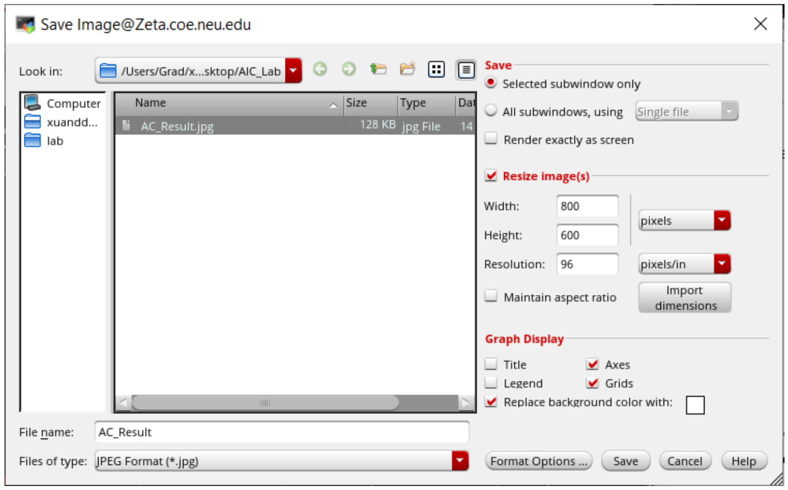



- MOSFET parameters: To check MOSFET's parameters such as gm, id, and so on, just select "Results" → "Print" → "DC Operating Points" (for example) and click the nmos symbol, NM0.




| signal | OP("/I4/NM0" "??") |
|---|---|
| beff | 90.3829m |
| betaeff | 91.8419m |
| cbb | 56.7784f |
| cbd | -15.1949f |
| cbdbi | -27.4731a |
| cbg | -7.97832f |
| cbs | -33.6051f |
| cbsbi | -8.22696f |
| cdb | -15.176f |
| cdd | 26.9587f |
| cddbi | 10.4558a |
| cdg | -11.8085f |
| cds | 25.7648a |
| cgb | -7.39078f |
| cgbovl | 212.713a |
| cgd | -11.6709f |
| cgdbi | 109.894a |
| cgdovl | 11.7808f |
| cgg | 59.679f |
| cggbi | 35.9046f |
| cgs | -40.6173f |
| cgsbi | -28.8365f |
| cgsovl | 11.7808f |
| cjd | 15.1674f |
| cjs | 25.3782f |
| csb | -34.2116f |
| csd | -92.8765a |
| csg | -39.8922f |
| css | 74.1966f |
| cssbi | 37.0377f |
| ft | NaN |
| fug | 31.966 |
| gbd | 3.57974n |
| gbs | 0 |
| gds | 349.612u |
| gm | 11.9842m |
| gmb | 3.66653m |
| gmbs | 3.66653m |
| gmoverid | 6.81107 |
| i1 | 1.75951m |
| i3 | -1.75951m |
| i4 | -170.16p |
| ib | NaN |
| ibd | -170.158p |
| ibe | -171.077p |
| ibs | -1.16536f |
| ibulk | -170.16p |
| id | 1.75951m |
| idb | 932.288a |
| ide | 1.75951m |
| ids | 1.75951m |
| ig | NaN |
| igb | 0 |
| igcd | 0 |
| igcs | 0 |
| igd | 0 |
| ige | 0 |
| igidl | 0 |
| igisl | 0 |
| igs | 0 |
| is | -1.75951m |
| isb | 1.16536f |
| ise | 1.75951m |
| isub | 170.157p |
| pwr | 1.61485m |
| qb | -34.0816f |
| qbd | -16.1218f |
| qbi | -33.9221f |
| qbs | -1.8978a |
| qd | 1.97117f |
| qdi | -4.53612a |
| qg | 46.5133f |
| qgi | 39.4948f |
| qinv | 17.637m |
| qsi | -5.56817f |
| qsrco | -14.4029f |
| region | 2 |
| reversed | 0 |
| ron | 521.611 |
| rout | 2.86032K |
| self_gain | 34.2785 |
| tk | NaN |
| type | 0 |
| ueff | 46.7781m |
| vbs | 0 |
| vdb | 917.78m |
| vds | 917.78m |
| vdsat | 150.617m |
| vdsat_marg | NaN |
| vdss | 150.617m |
| vearly | 5.03276 |
| vfbeff | -1.12088 |
| vgb | 750m |
| vgd | -167.78m |
| vgs | 750m |
| vgsteff | 198.074m |
| vgt | 197.319m |
| vsat_marg | 767.163m |
| vsb | -0 |
| vth | 552.681m |
| vth_drive | NaN |

- Save results: Select "File" from top menu in result window → "Save Image". Make sure you check the box "Replace background color with white" to make graph neat.




- Save simulation state: you can save your simulation setting by select "Session" → "Save State". The state is associated with your schematic and you can load them for simulation next time.