EECE7248 Lab #2:
Common-Drain and Common-Collector Amplifier

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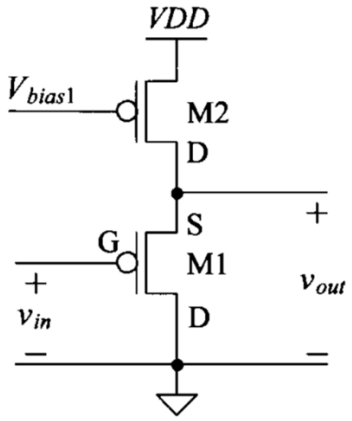
Design problem #1. Common Drain Amplifier.

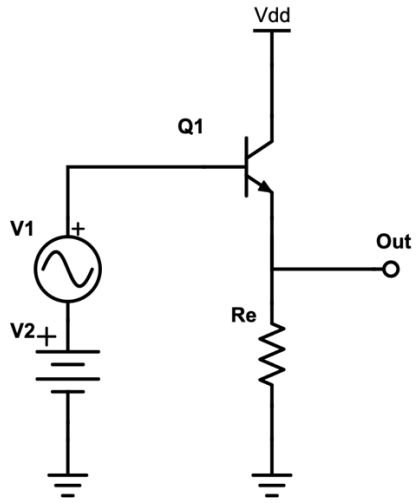
For this problem, we will design a common-drain amplifier with current source load (M2) using PMOS transistors (shown below). You have to choose the parameters to get a gain that is close to 0dB. Notice that the output load is C_L=0.2pf and the body of M1 & M2 are both connected to VDD.



1) Plot the AC gain (1Hz – 100GHz) of the amplifier in dB and mark the value at 100KHz.
2) Plot transient input & output signal and check the voltage gain comparing with the result from AC simulation.
3) Plot Z_{in} vs. frequency and mark the value at 100KHz.
4) Plot Z_{out} vs. frequency and mark the value at 100KHz.
5) What is the main problem of this structure that limits the gain? How do you solve it to improve the performance (make gain closer to 1) without adding any instance? Plot the AC gain and transient signal of your improved circuit.

Design problem #2. Common Collector Amplifier (npn with passive load, R_e)

Create new cell (schematic) in the AIC_Lab library and place the npn BJT and the resistor R_e to form the common collector amplifier.



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****** Lab report is due on 10/23 (Wed) ******