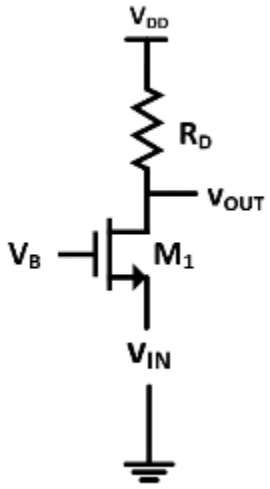
EECE7248 Lab #3:
Common-Gate and Common-Base Amplifier

Gyunam Jeon, Yixuan He, Yong-Bin Kim

Design problem #1. Common Gate Amplifier.

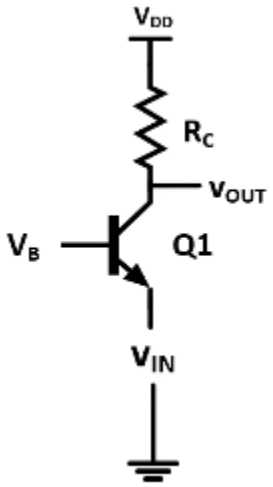
For this problem, we will design a common-gate amplifier with current source load (R_D) as shown below. You have to choose the parameters to get a **current gain that is close to 0dB**. Note that the output load is C_L=0.2pf and the body of n-MOSFET is connected to GND.



1) Plot the AC current gain (1Hz – 100GHz) of the amplifier in dB and mark the value at 100KHz.
2) Plot the AC voltage gain (1Hz – 100GHz) of the amplifier in dB and mark the value at 100KHz.
3) Plot transient input & output signal and check the voltage gain comparing with the result from AC simulation.
4) Plot Z_{in} vs. frequency and mark the value at 100KHz.
5) Plot Z_{out} vs. frequency and mark the value at 100KHz.

Design problem #2. Common Base Amplifier (npn with passive load, R_e)

Create new cell (schematic) in the AIC_Lab library and place the npn BJT and the resistor Rc to form the common base amplifier. You have to choose the parameters to get a **current gain that is close to 0dB.**



1) Plot the AC current gain (1Hz – 100GHz) of the amplifier in dB and mark the value at 100KHz.
2) Plot the AC gain (1Hz – 100GHz) of the amplifier in dB and mark the value at 100KHz.
3) Plot transient input & output signal and check the voltage gain comparing with the result from AC simulation.
4) Plot Z_{in} vs. frequency and mark the value at 100KHz.
5) Plot Z_{out} vs. frequency and mark the value at 100KHz.

****** Lab report is due on 11/6 (Wed) ******