Programming Larrabee: Beyond Data Parallelism

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Agenda:

- What do parallel applications need?
- How does Larrabee enable parallelism?
- How does Larrabee support data parallelism?
- How does Larrabee support task parallelism?
- How can applications mix parallel methods?
Architecture Convergence

Larrabee

- Multi-core
- Multi-threading
- Single Thread

IA: Highly Programmable

GPU: High Parallelism

CPU programmability & GPU parallelism
Programming Larrabee

• Larrabee supports “braided parallelism”:  
  – GPU-style data-parallelism, mixed with  
  – Multi-core task parallelism, mixed with  
  – Streaming pipe parallelism, mixed with  
  – Sequential code (still often necessary)  

• Larrabee can submit work to itself  

• Larrabee supports the IA architecture  

Larrabee lets applications mix the kinds of parallelism they need
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Larrabee Block Diagram

- Cores communicate on a wide ring bus
  - Fast access to memory and fixed function blocks
  - Fast access for cache coherency
- L2 cache is partitioned among the cores
  - Provides high aggregate bandwidth
  - Allows data replication & sharing
• Separate scalar and vector units with separate registers
• Vector unit: 16 32-bit ops/clock
• In-order instruction execution
• Short execution pipelines
• Fast access from L1 cache
• Direct connection to each core’s subset of the L2 cache
• Prefetch instructions load L1 and L2 caches
Vector Unit Block Diagram

• Vector complete instruction set
  – Scatter/gather for vector load/store
  – Mask registers select lanes to write, which allows data-parallel flow control
  – Masks also support data compaction

• Vector instructions support
  – Memory operand for most instructions: full speed when data in L1 cache
  – Free numeric type conversion and data replication while reading from memory
  – Rearrange the lanes on register read
  – Fused multiply add (three arguments)
  – Int32, Float32 and Float64 data
Key Differences from Typical GPUs

• Each Larrabee core is a complete Intel processor
  – Context switching & pre-emptive multi-tasking
  – Virtual memory and page swapping, even in texture logic
  – Fully coherent caches at all levels of the hierarchy

• Efficient inter-block communication
  – Ring bus for full inter-processor communication
  – Low latency high bandwidth L1 and L2 caches
  – Fast synchronization between cores and caches

Larrabee: the programmability of IA with the parallelism of graphics processors
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Data Parallelism Overview

- **Key ideas of data parallel programming**
  - Define an array (grid) of data elements
  - Run same program (kernel) over all the elements
  - Share memory between groups within the grid
  - Basically just nested parallel "for" loops

- **Strengths**
  - Good utilization of SIMD processing elements (VPU)
  - Hides long latencies (memory or texture accesses)

- **Limitations**
  - Works best for large, homogenous problems
  - Work efficiency drops with irregular conditional execution
  - Work efficiency drops with irregular data structures
Larrabee Data Parallelism: Strands

Each strand is the kernel running on one data element.

Each strand maps onto one (or more) VPU lanes.

Strands must support different conditional execution.
**Larrabee Data Parallelism: Fibers**

*Fiber: SW-managed context (hides long predictable latencies)*

- 16-wide vector unit
- 16-wide vector unit

More Fibers running (typically 2-10, depending on latency to cover)

SW cycles among fibers groups of strands) to cover latency
Larrabee Data Parallelism: Threads

**Cores:** Each runs multiple threads

**Thread:** HW-managed context (hide short unpredictable latencies)

**Fiber:** SW-managed context (hides long predictable latencies)

16-wide vector unit

More Fibers running (typically 2-10, depending on latency to cover)

More Threads (up to 4 per core, share memory via L1 & L2 caches)
Data Parallelism Summary

• Implementation hierarchy (your names may vary)
  – Strand: runs a data kernel in one (or more) VPU lane(s)
  – Fiber: SW-managed group of strands, like co-routines
  – Thread: HW-managed, swaps fibers to cover long latencies
  – Core: runs multiple threads to cover short latencies
  – Note: we use “thread” and “core” in micro-processor sense

• Comparison to GPU data parallelism
  – Same mechanisms as used in GPUs, except...
  – Larrabee allows SW scheduling (except for HW threads)

**Larrabee: uses many-core IA architecture to execute data parallel workloads**
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Task Parallelism Overview

• Think of a task as an asynchronous function call
  – “Do X at some point in the future”
  – Optionally “… after Y is done”
  – Light weight, often in user space

• Strengths
  – Copes well with heterogeneous workloads
  – Doesn’t require 1000’s of strands
  – Scales well with core count

• Limitations
  – No automatic support for latency hiding
  – Must explicitly write SIMD code
Larrabee Task Parallelism: Tasks

Task: SW-managed context

Scalar code
Auto-vectorizing compiler, C++ vector classes, or vector intrinsics

16-wide vector unit

... 

More tasks enqueued, waiting to run
**Larrabee Task Parallelism: Threads**

- **Cores**: Each runs multiple threads

  - **Thread**: HW-managed context (hide short unpredictable latencies)

  - **Task**: SW-managed context
    - Scalar code
    - Auto-vectorizing compiler, C++ vector classes, or explicit vector code
    - 16-wide vector unit

  - ... More tasks enqueued, waiting to run

  - ... More Threads (up to 4 per core, share memory via L1 & L2 caches)
Examples of Using Tasks

• Applications
  – Scene traversal and culling
  – Procedural geometry synthesis
  – Physics contact group solve
  – Data parallel strand groups
    – Distribute across threads/cores using task system
    – Exploit core resources with fibering/SIMD

• Larrabee can submit work to itself!
  – Tasks can spawn other tasks
  – Exposed in Larrabee Native programming interface
Larrabee Native Programming

- Internal projects include tools and compilers
- C and C++:
  - std C libs: printf(), malloc(), etc.
  - Data pointers, function pointers, recursion, etc.
- Threading: spawn P-Threads or use tasks
- Full software control when needed
  - Thread affinity, assembly code, etc.
  - Access to fixed function units

Larrabee: supports fully general purpose task parallel programming
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Applications Can Be Complex

• May need many kinds of parallel code
  – GPU-style data-parallelism
  – Multi-core task parallelism
  – Streaming pipe parallelism
  – And even some sequential code

• May also need
  – Self-scheduling (data-dependent new work)
  – Irregular data structures

• Example? The rendering pipeline
  – All in software in Larrabee, except for texture filtering
  – Works due to support for irregular computation
Larrabee’s Binning Renderer

- Binning pipeline
  - Reduces synchronization
  - Front end processes vertices
  - Back end processes pixels
  - Bin FIFO between them

- Multi-tasking by cores
  - Each orange box is a core
  - Cores run independently
  - Other cores can run other tasks, e.g. physics
Back-End Rendering a Tile

- Orange boxes represent work on separate HW threads
- Three work threads do Z, pixel shader, and blending
- Setup thread reads from bins and does pre-processing
- Combines task parallel, data parallel, and sequential
Pipeline Can Be Changed

• Parts can move between front end & back end
  – Vertex shading, tessellation, rasterization, etc.
  – Allows balancing computation vs. bandwidth

• New features can be added
  – Transparency, shadowing, ray tracing etc.
  – Each of these need irregular data structures
  – They benefit from mix of tasks and data-parallel
  – Also helps to be able to “repack” the data

• Graphics pipeline is just an example
  – These methods apply to many parallel applications
Application Scaling Studies


Programming Larrabee: Beyond Data Parallelism
“Choose the Right Tool”

• Use the 3D rendering pipeline
  – How you always have (or create your own)

• Use data parallelism
  – Parallel ‘for’ loop
  – Hide latency by switching to work from other elements

• Use task parallelism
  – Asynchronous function call
  – Hide latency with in-task reuse and asynch memory ops

• Use sequential code
  – Tie it all together
  – Communicate with host at higher level of abstraction

Flexible & programmable for many applications
Summary

• Larrabee lets applications mix the kinds of parallelism they need
• Larrabee provides the programmability of IA with the parallelism of GPUs
• Larrabee uses the many-core IA architecture to execute data parallel workloads
• Larrabee supports fully general purpose task parallel programming
• Larrabee is flexible & programmable for many applications
Larrabee: Beyond Data Parallelism

• Questions?

• See also
  – s08.idav.ucdavis.edu for slides from a Siggraph2008 course titled “Beyond Programmable Shading”
  – www.intel.com/idf -- click “content catalog” & search for “Larrabee:” to find a Larrabee presentation
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