Processor Memory Networks Based on Steiner Systems

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Task-Specific Processor

- Input:

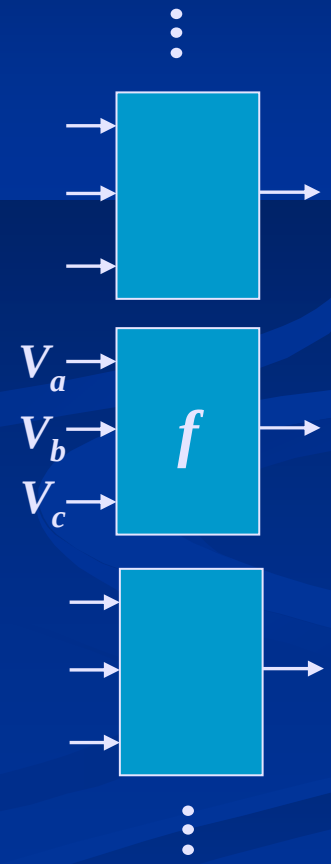
  Vectors V_1, V_2, … V_k

- Query:

  *Which set of **t** vectors maximizes $f(V_a, V_b, \ldots)$?*

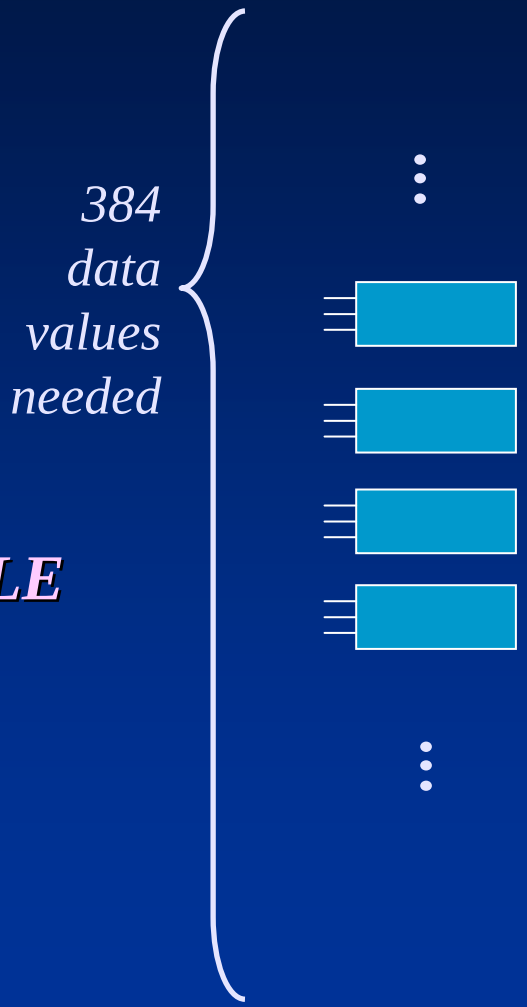
- Architecture:

  Parallel PEs on FPGA coprocessor



Problem: Input Bandwidth

- Assume ~128 PEs
  - × *3 X inputs per PE*
  - *= 384 values per cycle*
  - × *4 bits per value*
  - *= 1536 bits per cycle*
- Wide-word solution: ***INFEASIBLE***
  - *400-ported RAM?*
  - *Data fetched faster than host can load it*



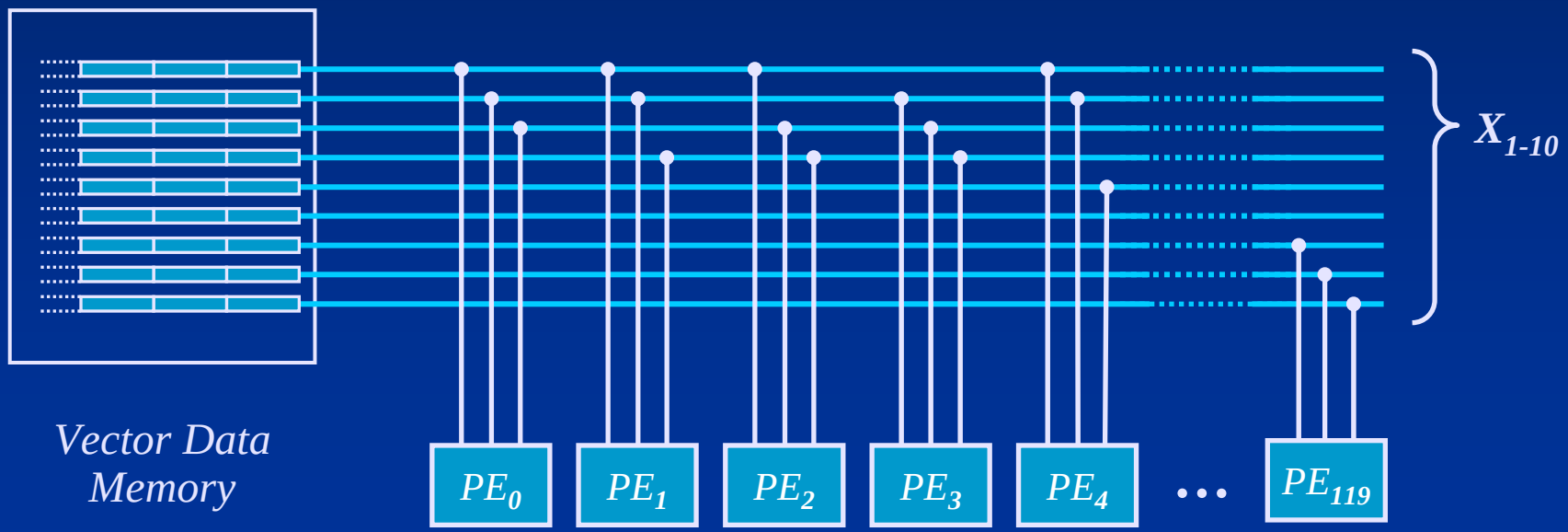
Distribution Network

- *X* memory: ***k*** data values supply $\binom{k}{3}$ PEs.

  k = 9 ⇒ 84 PEs, 252 PEs *X* inputs, **28× reuse**

  k = 10 ⇒120 PEs, 360 PEs *X* inputs, **36× reuse**

- Generates all size-3 subsets of ***k*** data values

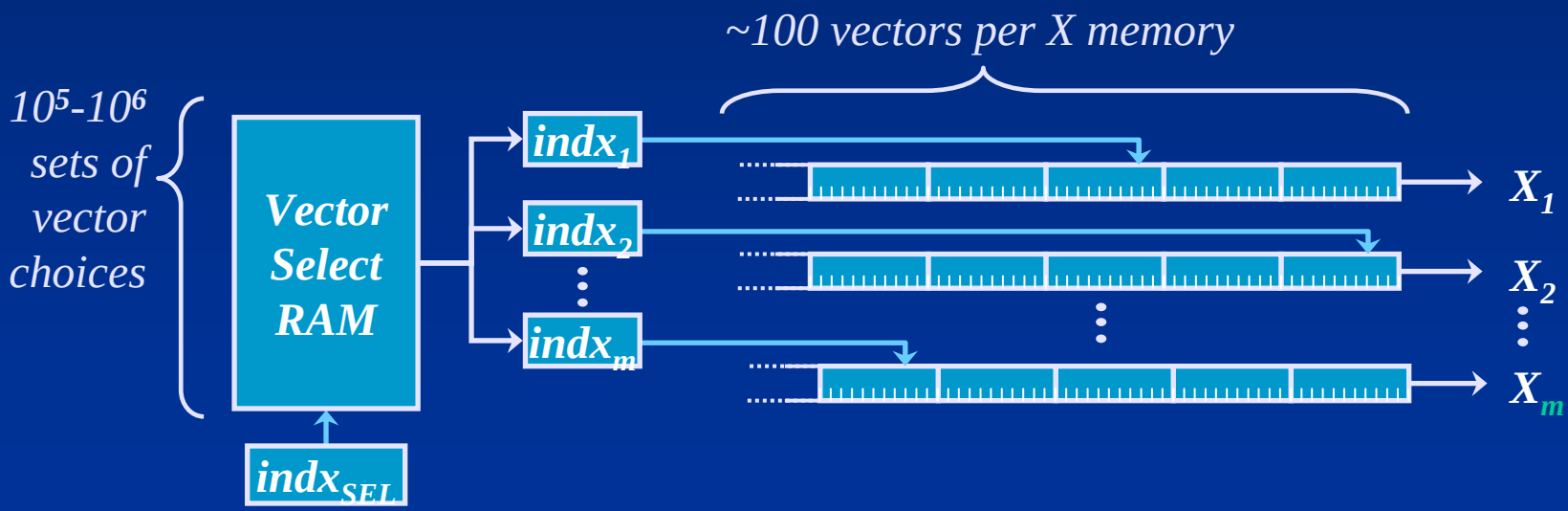


Vector Data Memory

- Steiner system $S(v, k, t)$

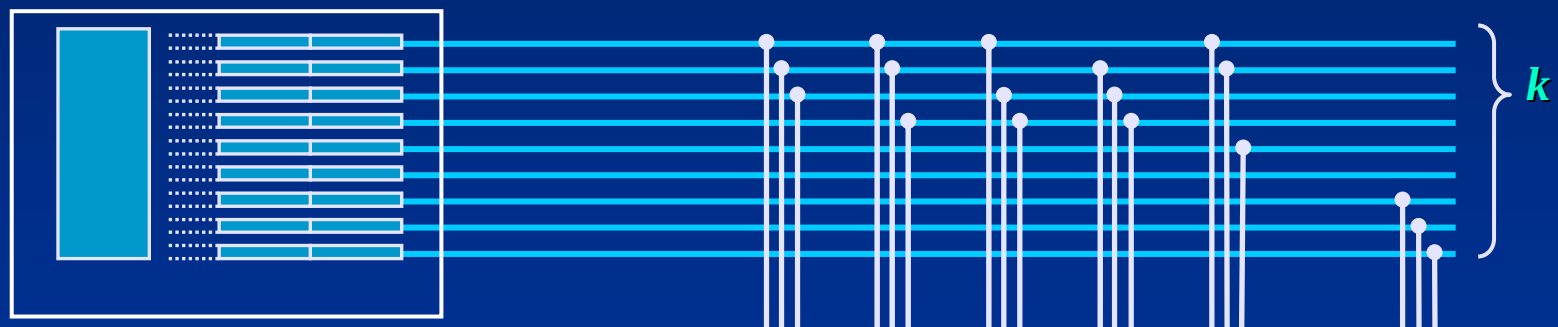
  *Divide **v** objects into subsets of size **k**, so that every size-**t** subset is in just one size-**k** subset.*

- $t = 3$ (triplets), $k =$ X memories, $v =$ total genes
- Host selects vector sets $\{m_1, m_2, \ldots\}$ via RAM content



Memory and Data Distribution

- Two-level data reuse
  - *Temporal reuse by Vector Select Ram*
  - *Spatial reuse by Distribution Network*
- Reloaded 10^5-10^6 times
- Whole VDM duplicated
  - *Double buffering*
  - *Separates reload, reading*



Vector data memory (VDM)

*Divide **v** objects into subsets of size **k** …*

*… so that every size-**3** subset is in just one size-**k** subset*

Conditions for Success

Resource Balancing

(multipliers per chip*) / (multipliers per CIR)	=	# CIR
(vector length) × (DPS cycle time)	=	DPS time
(DPS time) / (CIR time)	=	DPS / CIR
(DPS / CIR) × (# CIR)	=	# DPS
$\max_m \binom{m}{3} \leq$ (# DPS)	=	# X memories
$\binom{m}{3}$ / (# DPS)	=	combinatoric efficiency
min[(DPS time) / (DPS/CIR), CIR time]	=	vector time
(# DPS × combinatoric efficiency) / (vector time)	=	result rate

*Assumed to be limiting resource