NASIC: Nanoscale Application-Specific ICs and Architectures

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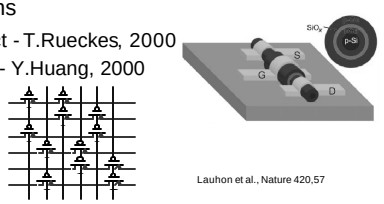
Background

- Carbon nanotubes (CNTs) - C.Dekker,1999
- Silicon nanowires (SiNWs) - A.M.Morales,1998
- Nanojunctions
  - Diode effect - T.Rueckes, 2000
  - FET effect - Y.Huang, 2000
- Nanogrid

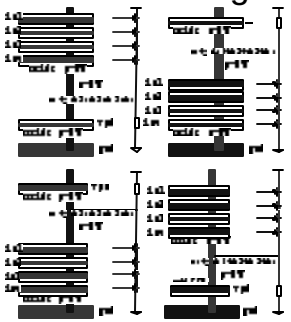


Lauhon et al., Nature 420,57

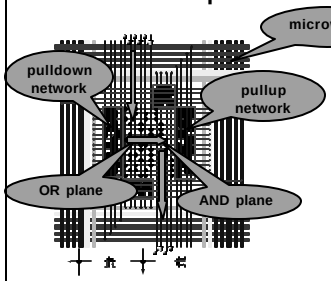
Motivation

- We develop circuits and architectures based on carbon nanotubes and silicon nanowires
- A key objective is to preserve density advantages of nano architectures compared to MOS in presence of fabrication and topology constraints
- We make an initial evaluation at system level

Nanoscale Logics

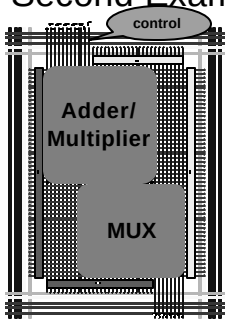


First example: 1-bit Full Adder



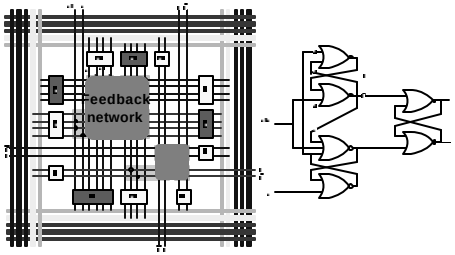
- Complementary inputs/outputs
- 2-level OR-AND logic
- Pullup/pulldown network

Second Example: 2-bit ALU

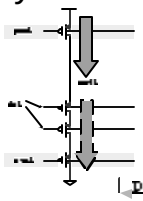


- Cascading of 2-level logic
- The results are selected by the multiplexer
- Building multiple logic blocks together can improve area utilization

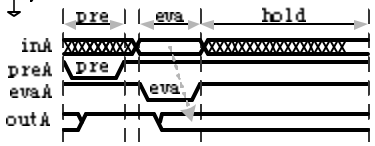
Bad Area Efficiency in Sequential Circuits: 1-bit D-Flipflop



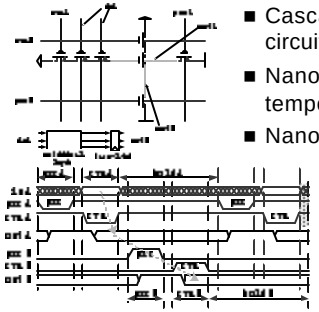
Dynamic Circuits



- Dynamic circuits: we use it for pipelined structures and temporary storage (shown next)
- Precharge-Evaluate-Hold phase
- Hold phase for cascading

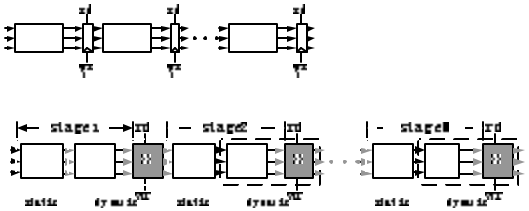


Nano-Latch

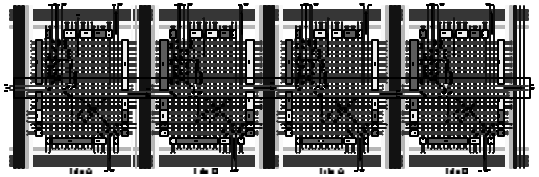


- Cascaded dynamic circuits -> NanoLatch
- Nano-Latch: idea for temporary storage
- Nano-Latch is implicit

Pipelined structure



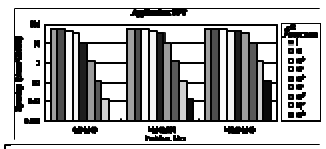
Interconnection



- Neighbored Tiles are connected by NWs
- Only minor modifications are needed to interconnect neighbored nanotiles
- Global interconnections are provided by MWs

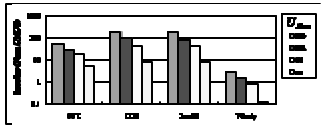
Initial System-Level Evaluation

Tools: we use SimpleFit (C.A.Moritz, et al 2001, IEEE Trans Par&Distributed Systems) extended for our circuit and nanodevice assumptions



Assumptions

	CMOS	Nano
Technology	30nm	4nm pitched NW 90nm pitched MW
Chip area	1.8cm^2	1.8cm^2
# of transistors	10^9	2.42×10^{11}



	CMOS	Nano
Technology	30nm	4nm pitched NW 90nm pitched MW
Chip area	1.8cm^2	1.8cm^2
# of transistors	10^9	variable

Conclusion

- Nanodevices have great density advantage over MOS technology, but fabrication (such as high defect density) and topology constraints may break down this advantage
- Based on our fabric architecture and initial study, even under conservative assumptions, nanoscale systems could still have significant advantages over MOS systems
- Taking physical layer aspects into consideration when designing nano architectures is key