		The CoGenT Project			
	: A Class-based Machine escription Language	 Co-generation of Comp 	piler and Simulator Tools		
Trek Palmer Jointly with: Ed Walters Tim Richards Faculty: Prof. Eliot Moss Prof. Chip Weems January 30, 2004		 Uses a single set of specifications to produce: Compiler back-end components Register allocators Code generators Code generators Instruction schedulers System tools Assemblers / Disassemblers Debuggers Simulators Functional/Instruction-accurate Cycle-based 			
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Why CoGenT?		Why a commo	Why a common machine description?		
 Hand-crafting compiler and simulator components is: Time-consuming Error-prone 		Compiler research requ Architecture research r	 Compiler research requires fast & accurate simulators Architecture research requires optimized compiler backends 		
 Current availal 	ble simulators are:				

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- Difficult to modify
- Difficult to port
- Difficult to instrument
- Difficult to optimize

- Common language:
 - Eliminates redundancy
 - Simplifies MD compiler
 - Assures syncronization of simulator and compiler
- Previous work solves only some of these problems

CoGenT High Level Architecture

- Two Representations
 - Description language (CMDL)
 - Fully specified, tree-based IR
- Front-end tools
 - Receive partially specified input from users
 - Generate complete IR descriptions
- Back-end tools

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- Receive complete descriptions
- Generate system tools and code

The CoGenT Language - CMDL

CMDL

- Specification language for:
 - Instruction set syntax
 - Instruction set semantics
 - Machine store descriptions
- C/Java-inspired syntax
- Elements of other machine description languages
- Allows partial descriptions (details filled in by tools)
- Allows class heirarchies to aid description

CoGenT Structure



Bits: The only principal type

- Everything is bits
- Single bits are valid
- Bit Arrays are also allowed
 - Defined by length
 - Multidimensional arrays are supported
- References provide named sub-regions
- Type modifiers express abstract qualities

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Туре М	odifiers and Declaratior	<u>15</u>		Examples	
 Current Modifiers: Signedness: unsigned/signed Endianness: big/little Mutability: overlay/field Handling conflicts Type declarations using type = 		 These type identifiers are equivalent: Posix: uint32_t CoGenT: big unsigned bit[32] These type declarations are equivalent: typedef uint32_t unsigned int type uint32 = big unsigned bit[32] References: uint32 foo; bit hi @ foo[0]; bit lo @ foo[31]; 			
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	<u>Endianness</u>			Subranges	
 Endianness specifies meaning of indexing Example: bit[2] foo = 0b10; Big Endian foo[0] = 1 Little Endian foo[1] = 1 Bits reordered through assignment Indexing converted through coercion 		 Named ranges on types (rather than instances) Example: big unsigned bit[32] ieee32fp; subrange sign = bit @ ieee32fp[0]; subrange exponent = unsigned big bit[8] @ ieee32fp[1]; No recursive subranges Different signedness and endianess allowed 			
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<u>Classes</u>	Constraints		
 Data + Methods Simple single inheritance No references Restricted form of inclusion Useful for specifying orthogonal instruction sets 	 CoGenT classes allow constraints on members For parsing, a constraint specifies an expected value For emitting, a constraint specifies a 'magic' constant 		
Trek Palmer CMDL 13	Trek Palmer CMDL 14 Example, continued		
Our friend, the PowerPC add immediate (addi) instruction $ \underbrace{14 RT RA SI 31}_{16} $ • All PPC instructions have 6-bit opcode field • addi is a D-Form instruction	<pre>class ppc { unsigned big bit[32] ppc_inst; unsigned big bit[6] OPCD @ ppc_inst[0]; } class d-form extends ppc { unsigned bit bit[5] RA @ ppc_inst[11]; } class addi extends d-form { unsigned big bit[5] RT @ ppc_inst[6]; unsigned big bit[16] SI @ ppc_inst[16]; }</pre>		

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CMDL

CMDL

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<u>Semantics</u>			Mixins			
 Instructions also have semantics Semantics are class methods Use C-style operators Additional, useful operators added (sign-extend, etc.) 			 Allows overloading without actually overloading Convenient for orthogonal instruction groups For instance, getaddr() mixin getAddrByWord requires (disp) { getaddr(disp) { return (bit[32])disp<<2; } } mixin getAddrByByte requires (disp) { getaddr(disp) { return (bit[32])disp<<2; } } mixin getAddrByByte requires (disp) { getaddr(disp) { return (bit[32])disp; }			
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	<u>Status + Goals</u>					
Base language	spec. stable (we even have a m	anual!)				
 Prototype parse 	r implementation nearly comple	ete				
 Front-end analysis in progress 						
 Microarchitecture description spec in progress 						
● http://ali-www.cs	s.umass.edu/cogent/index.htm					
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