

## Motivation

## The FIFO Approach

eProposed by Palacharla \& Smith [ISCA 97]
EFixed number and size of FIFOs
©Combined in-order \& out-of-order issuing
©Dependent instructions are inserted into a single FIFO
©Instructions are issued from FIFOs in parallel
©Only the instruction at the head of each FIFO is visible to the arbitration logic
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Performance and power trends

- Many complex architectural features are included
$\oplus$ These features consume power regardless of usage
(e. Adjustable datapath resources to match the application's needs
e. Focus on issue logic since it consumes a large portion of overall power dissipation
$\phi$ For instance, it was projected that the 21464 issue logic would account for $46 \%$ of the total power

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| Limitations of Fixed FIFO Scheme |  |  |
| :---: | :---: | :---: |
| ©A single configuration works well for some benchmarks, but not for others |  |  |
| ©High ILP: use more, or smaller FIFOs |  |  |
| ©Low ILP: use few FIFOs |  |  |
| ©Change number and size of FIFOs dynamically according to program needs |  |  |
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How Do We Decide When to Switch?
(e)Assumption: short term past behavior is a good indicator of behavior in the near future
©How do we keep track of "program needs"?
4 Keep track of statistics while a program is running
©Help decide the optimal configuration eWe use an array of monitors

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Conclusions
eIssue queue is a major contributor to power PFlexible schemes so we do not hamper performance
eDynamically reconfigurable, FIFOstructured issue queue can save power with negligible performance impact

