A Design Method for Paralleling Current Mode Controlled DC–DC Converters

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***Abstract*—This paper proposes a new current sharing method. It is based on current mode controlled dc–dc converters and achieves the current sharing by forcing all inner current loops to have the same current reference. Meanwhile, this method decouples control loops from the voltage regulation and current-sharing regulation instead of adding control loops as in traditional master–slave methods. Therefore, the large signal performance is good while its stability is guaranteed. Further, unlike multi-module methods, the modularity of single dc–dc converter is retained. Design rules and small signal analysis are presented. The advantages of the proposed method are verified by experimental results.**

***Index Terms*—Current-sharing regulation, current mode controlled (CMC), dc–dc converter, master–slave method.**

I. Introduction

PARALLEL power systems have seen widespread applications due to their benefits in redundancy, thermal management, efficiency and modularity. Typically, parallel power systems are designed so that the stresses among the paralleled dc–dc converters are balanced. This is commonly achieved by current-sharing control.

Among the many proposed schemes [1]–[8], the master-slave method is widely utilized [3]–[8] because of its good voltage regulation, modularity and simplicity. In this approach, the paralleled converters share information on output current through a current sharing bus; one converter is chosen as the master converter to ensure the voltage regulation, and others, the slave converters, try to keep their output currents to be the same as the master's by regulating their voltage reference through (additional) current-sharing control loops.

Because of the added current-sharing control loops, the parallel system with master-slave method becomes a multi-input, multi-output system. Therefore, the design and analysis requires sophistication [9], [10]. As a result, in system design, the bandwidth of the current-sharing control loop is kept much lower than that of the voltage control loop of the converter in order to guarantee the stability of the parallel system [5], [9], [11], [12]. However, this design rule results in a slow dynamic performance of the current sharing, and ongoing research is attempting to address these problems [13], [14].

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On the other hand, it is widely known that the current source behavior of the inner current loops of current mode controlled (CMC) dc–dc converters can be used to obtain current sharing [15], [16]. For example, when multiple dc–dc converters are paralleled, all inner current loops can be forced to share one voltage loop [17]–[19]. Ongoing research focuses on improving robustness by adding third common output filter [18] or by introducing an additional control loop [20], [21]. However, these approaches have the disadvantage of losing the modularity of the dc–dc converters. Alternatively, [6] uses the source/sink capacity imbalance of UC3843 to force all converters to share the same inner current reference. However, the UC3843's on the slaves are saturated, and therefore, so are their voltage control loops.

This paper recognizes both the benefits and limitations of master-slave methods and the methods using the inherent current source properties of CMC converters. We propose a new master-slave current sharing design using the inner current source of CMC converters. It includes two parts: loop design and saturation prevention. In the loop design procedure, all inner current references are sent to a current sharing bus, and one reference is chosen as the master. Then all inner current loops take the master value as their reference to achieve current sharing by modifying the sensed current signal. Therefore, only the voltage control loop of the master is active in voltage regulation while those in the slaves are decoupled from the system. However, those voltage control loops in the slaves will saturate because of different references, and this implies performance degradation when the master fails. Therefore, the second part of the method is saturation prevention: to make those voltage loops have the same inner current reference as the master. Hence, the voltage loops of slaves actively act as backups for the master voltage loop.

Specifically, the current sharing approach in this paper has the following features.

1) The proposed method is a master-slave method, and the current sharing bus is a minimum-master bus.
2) The proposed method uses the inner current loop of the CMC converter to achieve current sharing. Therefore, the current sharing response speed is fast and of the order of the speed of the inner current loop of an individual converter.
3) The proposed method achieves current sharing by modifying the sensed current signal. Thus, no additional current sensing circuit is needed.
4) The proposed method decouples the voltage control loops of slave converters from the parallel system. This makes

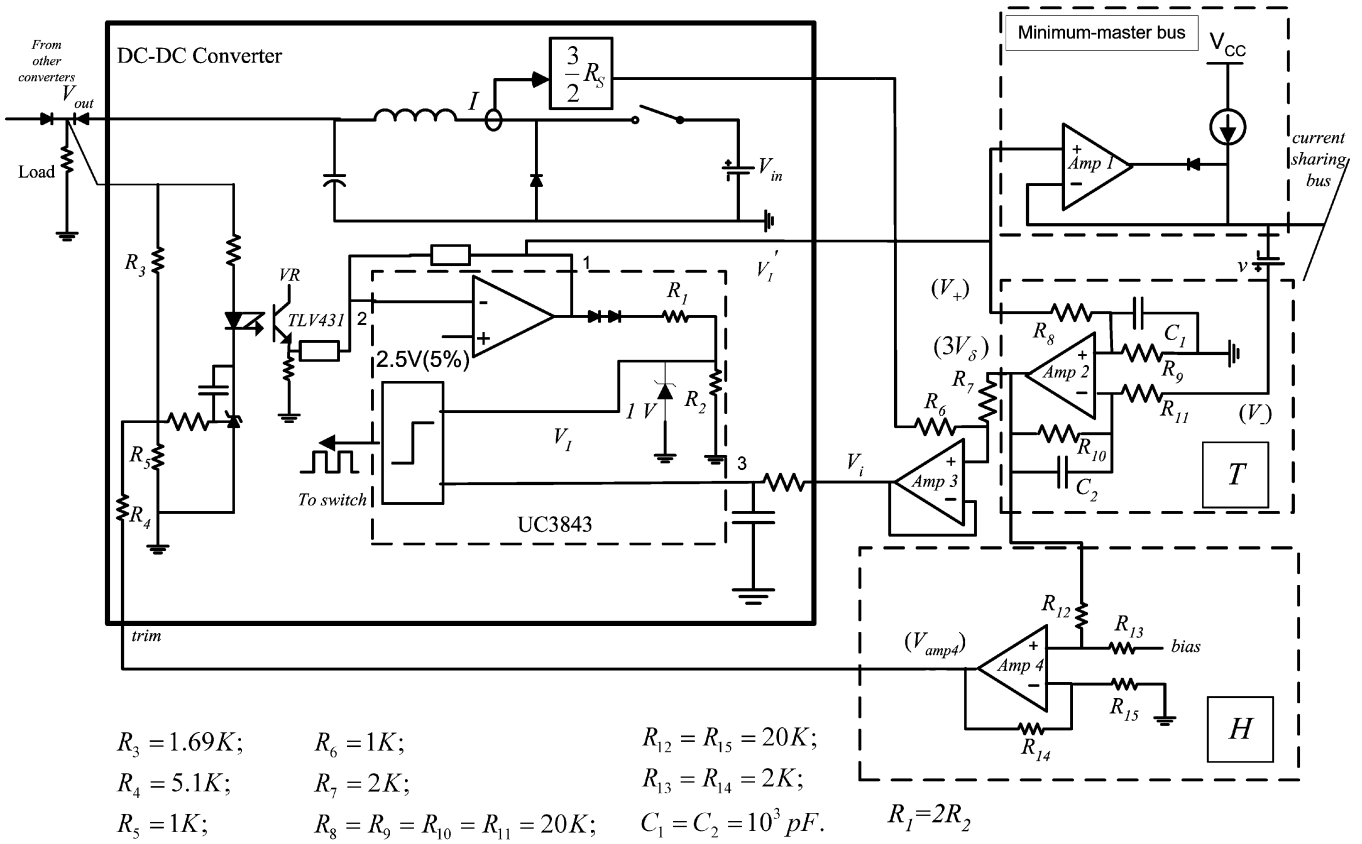

Fig. 1. Simplified schematic of proposed current sharing method.

the stability analysis of the entire paralleled system similar to the stability analysis of an individual dc–dc converter. Therefore, the system design is simple.

5) Unlike traditional current sharing methods using inner current loops of CMC converters, modularity of each single converter is maintained and no controller in the converters is in saturation.
6) The proposed method is implemented by using off-the-shelf dc–dc converters with current mode PWM controllers, UC3843.
7) Because the proposed method does not need additional current sharing loops, the implementation is simple and saves cost and space.

The implementation of the method is presented in Section II based on current mode PWM controller, UC3843. The operation of master and slave converter is shown in Section III. A small signal model and design rules are presented in Section IV. This method is implemented by using off-the-shelf dc–dc converters in Section V. Experimental results verify the proposed design. Conclusions are given in Section VI. Detailed small signal analysis is given in Appendix.

II. Implementation Description

The implementation of the method is shown in Fig. 1. The dc–dc converter used is a peak current mode controlled converter with UC3843, and the amplifiers used are rail-to-rail single supply op amps. Specifically, each block has function as follows.

DC–DC Converter: The solid box represents a peak current mode controlled dc–dc converter with input voltage, V_{in}, and load. A buck converter is shown as the power train. Many dc–dc converters use synchronous rectification, and barrier diodes are commonly used for parallel design. As shown in Fig. 1, barrier diode is placed between the output and the load, and remote sense is used to compensate the voltage drop on the barrier diode and distribution lines. R_4 is the voltage trim resistor. Later it will be shown that only the trim resistor network and the outer voltage loop gain are needed for the system design while the other details such as the parameters of the power train and controller are not critical.

There are different current sensing methods, and, for simplicity, it is assumed that the inductor current I is sensed, and R_S is the gain of the current sensing function. (Usually, it is the value of the current sensing resistor or the sample resistor at the output of the current transformer.) Originally, the output of R_S is connected to V_I and used as an input to UC3843, which is represented in a dashed box. $V_{\rm I,ref}$ is the inner current reference while the output of *pin 1* of UC3843, $V'_{\rm I,ref}$, is proportional to $V_{\rm I,ref}$ with the bias of the voltage drop on the two diodes [22]. Therefore, in normal operation, the output of *pin 1* can also be viewed as the current reference. Specifically

$$V'_{\rm I,ref} = 3V_{\rm I,ref} + 2V_{diode} \tag{1}$$

where V_{diode} is the forward voltage drop on the diode, and the number of 3 comes from voltage division and the relation between R_1 and R_2 in Fig. 1.

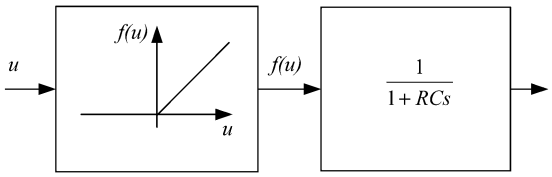

Fig. 2. Function of T.

However, (1) is only true in normal operation because $V_{\rm I,ref}$ is limited to 1 V by the Zener diode paralleled with R_2.

Originally, the sensed current signal is $I \cdot R_S$. In the proposed method as shown in Fig. 1, the current sensing gain is modified to $(3/2)R_S$ in order to maintain the current signal at V_I, which will be shown later.

Minimum-Master Bus: The minimum-master bus consists of *Amp 1*, the diode at its output, the current sharing bus and the current source. Therefore, the minimum voltage to *Amp 1* will appear on the bus. In Fig. 1, the converter with the minimum current reference is the master. That is

$$V_{bus} = V'_{I,ref,master} \tag{2}$$

where V_{bus} is the voltage of the current sharing bus and $V'_{I,ref,master}$ is $V'_{\rm I,ref}$ of the master. Details of the minimum-master bus can be found in [8], which also includes hot-swap circuits.

The voltage signal of the current sharing bus is forwarded to the input of function block T through a small voltage bias in Fig. 1. The small voltage bias, given as v, is used to improve the noise immunity and to prevent bus competition. Therefore, there is

$$V_- = V_{bus} + v \approx V_{bus}. \tag{3}$$

In following analysis, v will be ignored if not specified.

Function Block T: In Fig. 1, if $V+$ is larger than $V-$, function block T is simply a low-pass filter. However, all amplifiers in Fig. 1 are single supply op amps, and their lowest output voltage is zero. Therefore, T is a nonlinear function, as shown in Fig. 2.

The function $f(u)$ in Fig. 2 is a piecewise-linear function (the nonlinear part of T) and can be represented as

$$f(u) = \begin{cases} u & u > 0 \\ 0 & \text{else.} \end{cases} \tag{4}$$

where $u = V_+ - V_-$. V_+ and V_- are the inputs to the positive input and the negative input of *Amp 2*, respectively.

On the other hand, because in Fig. 1, $R_8 \sim R_{11}$ have the same value and $C_1 = C_2$, the low-pass filter is the right block in Fig. 2 where $R = R_8$ and $C = C_1$.

Finally, the inputs to T are the outputs of *pin 1*, $V'_{\rm I,ref}$, of UC3843's, and (1) shows its relation with inner current reference $V_{\rm I,ref}$. Specifically, the positive input to *Amp 2* is

$$V_+ = 3V_{\rm I,ref} + 2V_{diode} \tag{5}$$

where $V_{\rm I,ref}$ is the inner current reference of the converter. From (1) and (3), the negative input to *Amp 2* is

$$V_- = V_{bus} + v = 3V_{I,ref,master} + 2V_{diode} + v \tag{6}$$

where $V_{I,ref,master}$ is the inner current reference of the master and v is a small dc bias.

Therefore, if $V_+ > V_-$ and v is ignored, at steady state

$$Output\ of\ T = V_+ - V_- = 3V_\delta - v \approx 3V_\delta. \tag{7}$$

Here, V_δ is defined as the difference between $V_{\rm I,ref}$ of the converter and $V_{I,ref,master}$.

Amp 3: Amp 3 with R_6 and R_7 is an addition function. With the values in Fig. 1, there is

$$V_I = I \cdot R_S + V_\delta \tag{8}$$

where $I \cdot R_S$ is the current signal in the original converter. Equation (8) explains the reason the current sensing function is modified to $(3/2)R_S$ in the proposed method in Fig. 1.

Function Block H: Function Block H is a proportional function. With the value of resistors in Fig. 1, there is

$$V_{amp4} = \frac{R_{14}}{R_{15}} 3V_\delta + bias \tag{9}$$

where *bias* is for matching the steady state output voltage.

Therefore, H will adjust the output voltage of the converter by regulating *trim* pin based on the output of V_δ. It will prevent the voltage loops of the slaves from saturation, as will be explained later. In real applications, H is almost always needed for voltage limiting, due to the output range limit of the components, which will be shown in the implementation in Section V.

III. Operation

A. Operation of the Slave

When current mode controlled dc–dc converters are paralleled directly without current sharing regulation, the inner current loops will have different reference values due to the tolerance on components and references. Suppose there are two same peak current mode controlled converters directly paralleled. One converter has a higher inner current reference of $V_{I,ref,slave}$, while another has a lower inner current reference of $V_{I,ref,master}$. Fig. 3(a) shows the current signal waveform, V_I, of the converter with $V_{I,ref,slave}$, which is fed to the *pin 3* (*CS*) of UC3843 in Fig. 1. In addition, $V_{I,ref,slave}$ is the solid line and $V_{I,ref,master}$ is the dashed line. The difference between the two references is V_δ, as in (7), and V_δ can be viewed as the reason for the current imbalance among the converters. That is

$$V_{I,ref,slave} = V_{I,ref,master} + V_\delta. \tag{12}$$

Current sharing can be obtained by equalizing the peak values of output currents in the application of peak current mode controlled converters. Therefore, the proposed method achieves current sharing by forcing the peak values of the current signal to be equal. Assume that $V_{I,ref,master}$ and $V_{I,ref,slave}$ hold constant. Fig. 3(b) shows the current signal waveform of the converter with $V_{I,ref,slave}$, which is the slave converter in the implementation of Fig. 1. Fig. 3(b) shows that the sensed current signal has a bias value V_δ. In fact, in Fig. 1, V_I is the sum of the real current signal of the output inductor

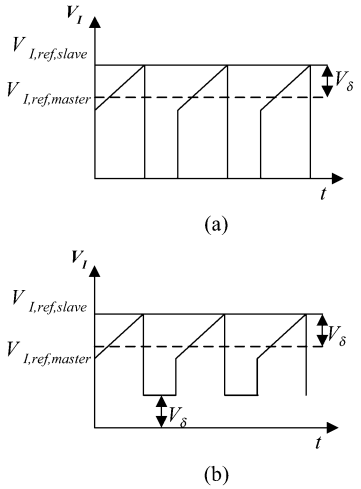

Fig. 3. (a) Current signal in a paralleled converter without current sharing. (b) Current signal in the slave converter with proposed method ($V_{I,ref,master}$ current reference of the master;$V_{I,ref,slave}$: current reference of the slave).

and V_δ, as shown in (8). Therefore, with (8) and (12), the peak value of the real current signal is

$$I_{peak} = \frac{(V_{I,ref,slave} - V_\delta)}{R_S} = \frac{V_{I,ref,master}}{R_S}. \quad (13)$$

Equation (13) shows that the real output current of the slave has the same peak value as that of the master, and thus current sharing is achieved when the inductors and current sense gains are the same among the converters.

Therefore, this method forces all inner loops to have the same output current peak value by modifying the sensed current signal. It can also be viewed as an indirect way to set the inner current references to the value of the master converter's. As a result, only the voltage control loop of the master converter is working effectively.

The above analysis assumes that all inner current references hold constant. However, in real applications, the voltage compensators of the slaves will try to regulate their own output to force the true output currents to meet their own inner references. So the current references of slaves, which are the output of the voltage compensators, tend to go into saturation. The function block H is used to prevent this from occurring.

The output of H, which is connected to the *trim* pin of the converter, regulates the voltage reference of the converter to reduce V_δ. V_{bias} is a constant voltage to match the dc point of the output. Therefore, H prevents the voltage control loops of the slave converters from saturating. We call this control loop the minor loop. Obviously, the minor loop does not participate in current-sharing control directly in normal operation. Meanwhile, it will be shown later that, if the bandwidth of the minor loop is sufficiently lower than that of the voltage control loop of the converter, the reference regulation is decoupled from the voltage regulation. That is, voltage loop bandwidth/ regulation is unaffected if H is properly selected.

Therefore, this method "removes" the voltage loops of slaves to achieve current sharing instead of adding another current-sharing loop. As a result, there is no tradeoff between the stability and bandwidth of current sharing loop design, and the parallel system will have good large signal performance.

On the other hand, because the design for saturation prevention is not directly related to the current sharing, the proposed method divides the parallel design procedure into two *independent* and easier solved problems. The first is to maintain current sharing. The second, independent problem is to keep all control loops in the system working normally. As a result, system design becomes simple. Meanwhile, the inner current sources have higher crossover frequencies than that of the voltage loops, and it implies that the parallel system will have fast voltage and current sharing dynamic response.

IV. Analysis and Design

Although the proposed method is a master-slave method, the known analysis method in [3]–[5], [9], [10] cannot be used because there is no additional current sharing control loop in the implementation, as shown in Fig. 1. Therefore, this section first presents a small signal model of the proposed method based on a macro model of CMC converters. Then design rules are proposed based on this model. It shows that the stability analysis of the proposed method is straightforward and justifies that the proposed method has fast current sharing response speed.

System Model: A dc–dc converter can be modeled as a controlled voltage source with output impedance [10]. Further, the inner loop of the CMC converter can be modeled as a current source. This leads to a small signal model of a CMC converter as shown in Fig. 4(a). Using the notation of [10], B is the transfer function from the voltage sense point to the comparison point with *ref*. In the simplest case, B is a scaling factor from a resistor network. A_V is the transfer function of the voltage controller in the converter. The block 1/3 is the proportion between $V'_{\rm I,ref}$ and $V_{\rm I,ref}$ in Fig. 1.

Referring to Fig. 4(a), the output of transfer function A_V, given as x, is the inner current reference, which corresponds to *pin 1* of UC3843. The dashed box represents the inner current loop and it is a voltage controlled current source. F_I is the transfer function from small signal inner current reference $\hat{V}_{\rm I,ref}$ to small signal inductor current $\hat{I}$ when the current loop is closed. (For peak current mode control, the inner current reference $V_{\rm I,ref}$ in Fig. 1 is the peak value of the output current, so is I. Therefore, although they correspond to $\hat{V}_{\rm I,ref}$ and $\hat{I}$, respectively, there is a difference between the variables.)

Z_O is the output impedance of the inner current loop and is sometimes approximated as the impedance of the output capacitor bank. Therefore, for a single module, the outer voltage loop, T_V, is

$$T_V = \frac{1}{3} A_V B F_I Z \quad (14)$$

where $Z = Z_O \,//\, Load$. In most cases, the impedance of the load can be ignored compared with that of Z_O. That is

$$T_V \approx \frac{1}{3} A_V B F_I Z_O. \quad (15)$$

Based on the current source model, the model of the proposed method is shown in Fig. 4(b). For simplicity, only two converters are shown, and the effects of the barrier diode and impedance of the distributed lines are ignored. Because the proposed method modifies the current signal at the comparison point with the (peak) inner current reference $V_{\rm I,ref}$, from the point of view of

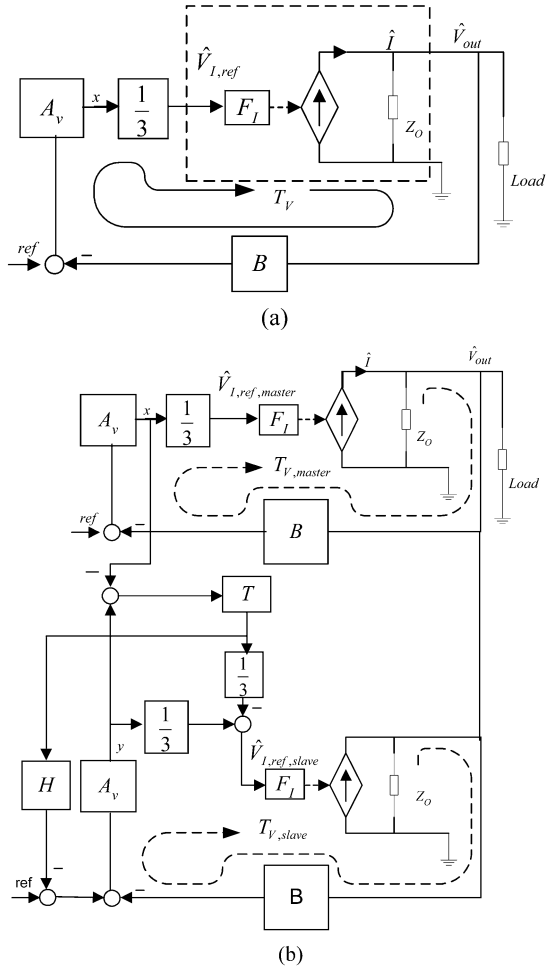

Fig. 4. Model of (a) a current mode controlled converter and (b) proposed method.

small signal, it can also be viewed as modifying $\hat{V}_{\rm I,ref}$. Meanwhile, this method is a master-slave method, and any converter can obtain the current sharing bus and be the master. However, when the master position is established and the system is in steady state, from the point of view of small signal, the system is the same as the dedicated master-slave system. Therefore, dedicated master-slave structure is used in system modeling. In Fig. 4(b), the upper converter is the master module, and the lower is the slave module.

Design Considerations: From the schematic, the minor loop in the proposed method is similar as the current sharing control loop in traditional master-slave methods: Both methods have control loops to regulate the *trim* pin [5], [9], [12]. However, the control goal in the proposed method is different. In the traditional master-slave methods, the current sharing control loop regulates the *trim* pin in order to change the converter's output voltage and then to achieve current sharing. On the other hand, as shown before, the minor loop in the proposed method is used to prevent loop saturation, and it does not directly participate in current sharing. Therefore, the issue on slow current response in traditional master-slave methods in [5], [9], [11], [12] does not exist in the proposed method.

On the other hand, in both traditional master-slave methods and the proposed method, it is desired that the regulation on *trim* pin does not conflict with the output voltage regulation (of the outer voltage loop in the converter). Therefore, the design rule for current sharing control loop in traditional methods in [5], [9], [11], [12] can be used in design minor loop gain. That is, the minor loop gain should have a much lower crossover frequency compared with the voltage loop gain.

Meanwhile, the minor loop gain is

$$T_{\rm minor} = HTA_V \tag{16}$$

where A_V is part of the converter and T is part of the current sharing circuit. A_V and T are designed based on other specifications and are always stable. Therefore, in order to have the minor loop gain has much lower crossover frequency, there is

Design Rule 1: H is a (sufficiently) small gain.

Therefore, when H is a small gain, small signal analysis can be conducted and the minor loop is decoupled from the outer voltage control loop. (In real design, the trimming range of H should also be considered.) So, in the rest of the paper, H is ignored in small signal analysis, i.e., $H \approx 0$.

On the other hand, as shown before, the current sharing is achieved by making the inner current sources of all converters have the same reference, $x/3$. Meanwhile, in Fig. 4(b), the current reference to the inner current source of the slave module is

$$\hat{V}_{I,ref,slave} = \frac{[y - T(y-x)]}{3} \tag{17}$$

and it is desired that

$$\hat{V}_{I,ref,slave} = \hat{V}_{I,ref,master} = \frac{x}{3}. \tag{18}$$

Therefore, we have Design Rule 2:

Design Rule 2: The dc gain of T is 1 (in order to guarantee steady state current sharing).

In fact, it is ideally derived $T = 1$. That is, in the ideal case,

$$T_{\rm V,master} = \frac{1}{3} A_V B F_I N \frac{Z}{N} = T_V \tag{19}$$

where N is the number of paralleled dc–dc converters, and $T_{\rm V,master}$ is the outer voltage loop gain of the master with the outer voltage loop of slaves closed.

In the ideal case, for a slave converter, the output of its voltage controller, y, does not appear in its inner current reference, $\hat{V}_{I,ref,slave}$, as shown in (18). That is

$$T_{\rm V,slave} = 0 \tag{20}$$

where $T_{\rm V,master}$ is the outer voltage loop gain of the slave with the outer voltage loop of the master and those of other slaves closed.

Therefore, in the ideal case, the voltage control loops of the slaves are decoupled from voltage control, and only the master participates in the voltage regulation by adjusting its inner current reference. In fact, this ideal system is similar to a multi-module converter, which has only one voltage control loop [17]–[19].

However, in real applications, it is desired that the noise on the current sharing bus be filtered out. Thus, T is almost always designed as a low-pass filter in the linear region. For example, capacitors C_1 and C_2 are added to behave as a low-pass filter in Fig. 1. As a result, the performance of the system will deviate

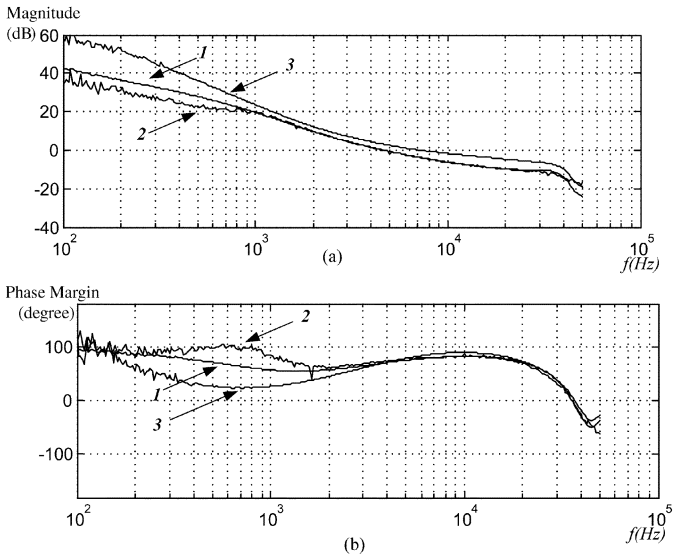

Fig. 5. Loop gain of the outer voltage control loop of the master converter with that of slave closed Curve 1 is the predicted $T_{\mathrm{V,master}}$ based on (21) when the effects of H is ignored; Curve 2 is the measured $T_{\mathrm{V,master}}$; Curve 3 is the ideal prediction of $T_{\mathrm{V,master}}$ based on (19). (a) Magnitude in dB. (b) Phase margin in degree.

from the ideal case. As the Appendix derives, when two converters are in parallel, we actually obtain

$$T_{\mathrm{V,master}} = \frac{\frac{1}{2}T_V(1+T)}{1+\frac{1}{2}T_V(1-T)}. \tag{21}$$

When two converters are paralleled as shown in Figs. 4(b), Fig. 5 shows the predicted $T_{\mathrm{V,master}}$ based on both (19) and (21). In the ideal case of (19), $T_{\mathrm{V,master}}$ equals T_V of the stand-alone converter. Curve 3 is the prediction based on the measured result of the individual converter. The "noise" comes from the measurement on the individual converter using the method of [24]. This leads to prediction errors between Curve 3 (ideal prediction) and Curve 2 (experimental measurement). As shown in Fig. 5, $T_{\mathrm{V,master}}$ has smaller gain than T_V, and the phase margin curve changes little.

However, around the crossover frequency, the predicted $T_{\mathrm{V,master}}$ using (21) and the experimental measurements almost exactly match. The phase margin is precisely predicted to be 76.3 degrees and the (correct) crossover frequency is predicted to be 4.67 KHz. At low frequency, because H is ignored in analysis, the predicted result deviates some from the measured one. However, we are concerned with the behavior near the crossover frequency for stability analysis, and the prediction can still be used for stability analysis.

V. Experimental Results

In order to evaluate the performance of the proposed method, a parallel system with two dc–dc converters is built. The dc–dc converters are commercially available 36–72 V/3.3 V converters. They are peak current mode controlled forward converters using the UC3843 each with output current rating of 15 A. Meanwhile, the *trim* pin has been intentionally regulated to have a severe current imbalance if the converters are directly paralleled. Current transformer is used for current sensing in the converter.

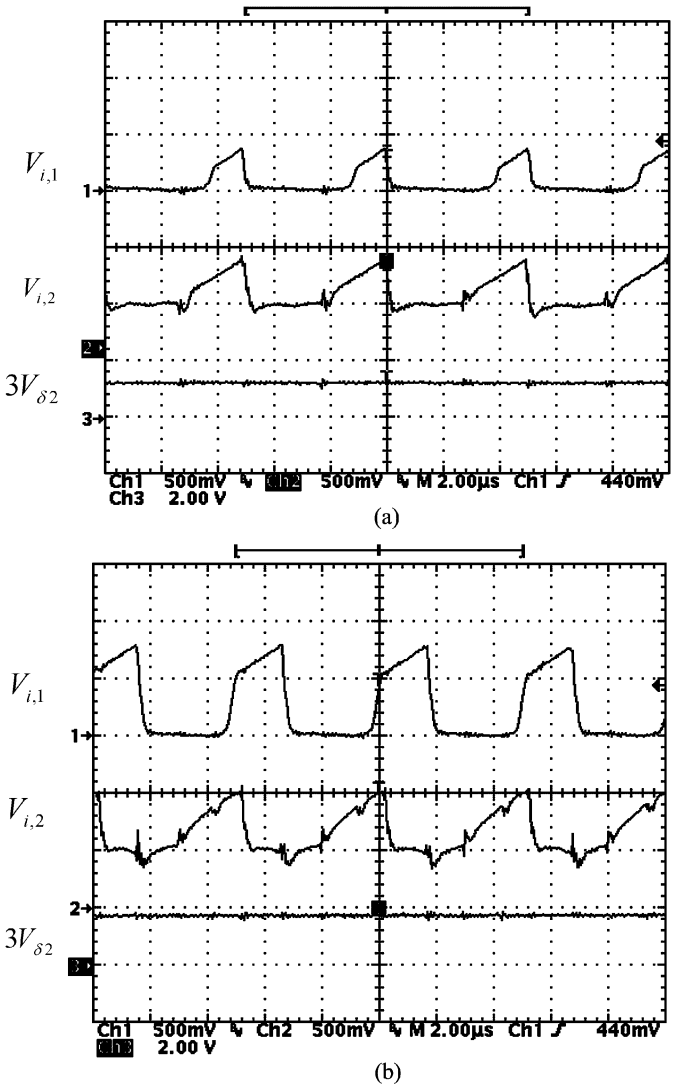

Fig. 6. Measured waveform (a) Output current: total, 10 A; Module 1, 4.9 A; Module 2, 5.1 A (b) Output current: total, 22 A; Module 1, 14.5 A; Module 2, 7.5 A (Channel 1: current signal of Module 1, $V_{i,1}$; Channel 2: current signal of Module 2, $V_{i,2}$; Channel 3: output of *Amp 2* of Module 2, $3V_{\delta 2}$).

In Fig. 1,

$$H \approx \frac{R_{14}}{R_{15}}\frac{R_3}{R_4} = 0.033 \tag{22}$$

which is sufficiently small for the design.

Two-Step Design: In order to show that this method consists of two relatively independent tasks, first H is disconnected from the system. The experimental results are shown in Fig. 6. In Fig. 6(a), the load is 10 A. The output current of Module 1 is 4.9 A, and that of Module 2 is 5.1 A. $V_{i,2}$ is the current signal (see Fig. 1) of Module 2. It has a dc bias, which equals to 1/3 of the output of its *Amp 2*, $3V_{\delta 2}$. It shows that current sharing is achieved by modifying the current signal, as explained in Fig. 3.

However, without H, the voltage control loop of the slave will try to regulate the inner current reference to meet its own voltage reference. Therefore, at high load, the dc bias will become so high that its current reference $V_{1,ref}$ will be locked at 1 V because of the Zener diode (see Fig. 1).

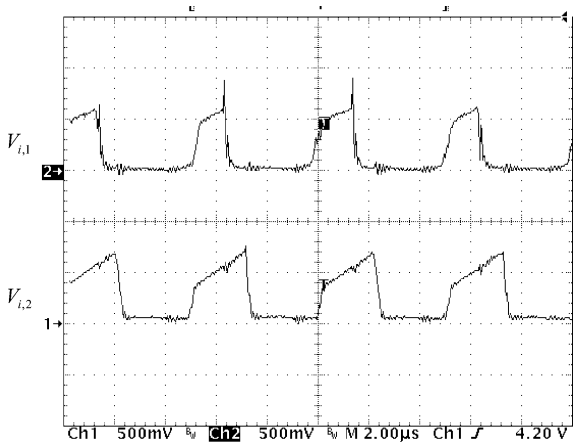

Fig. 7. Measured waveform of output current: total output 22 A; Module 1, 10.7 A(master); Module 2, 11.3 A (slave) (Channel 2: current signal of Module 1, $V_{i,1}$ Channel 1: current signal of Module 2, $V_{i,2}$).

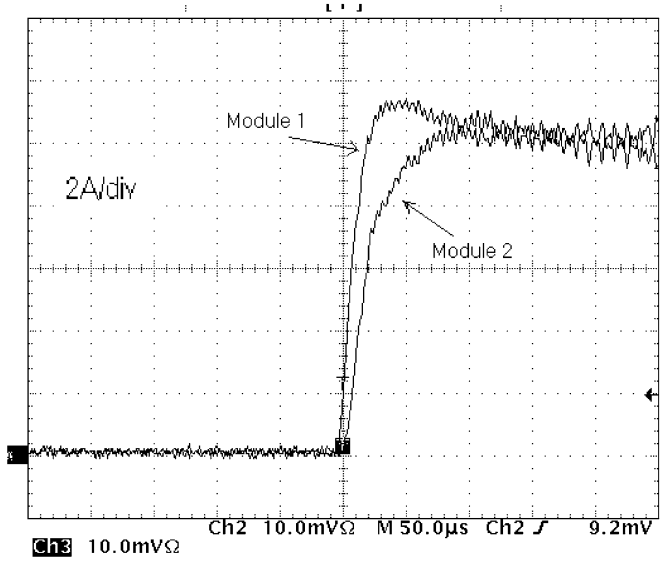

Fig. 8. Step response (0–20 A) of the output current.

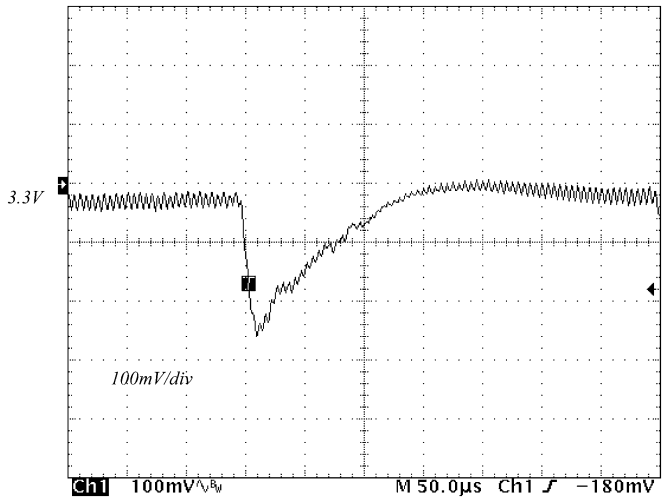

Fig. 9. Step response (0–20 A) of the output voltage.

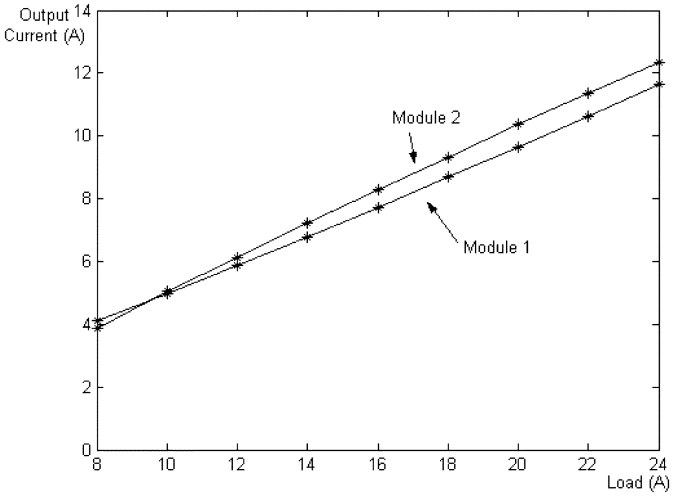

Fig. 10. Steady state current sharing for different loads.

Fig. 6(b) shows the voltage limit. In this case, the load is 22 A. The output current of Module 1 is 14.5 A, and that of Module 2 is 7.5 A. The peak value of current signal of Module 2 is locked at 1 V. Meanwhile, its dc bias equals to 1/3 of the output of its *Amp 2*, $3V_{\delta 2}$.

In this case, the current sharing is lost due to the Zener diode in UC3843. Therefore, in this application with UC3843, minor loop is necessary to prevent voltage control loops of slaves from saturating and to guarantee the current sharing at high load.

Fig. 7 shows the waveform after H is connected. The load current is still 22 A. The output current of Module 1, the master, is 10.7 A, and that of Module 2, the slave, is 11.3 A. It shows that the dc bias in Fig. 7 is reduced to around 50 mV due to the regulation of the minor loop, and both modules are working normally. Meanwhile, the dc bias is the result of low gain of H.

Large Signal Performance: In order to test its large signal performance, a load stepping from 0 to 20 A is applied, as shown in Fig. 8. The time scale is 50 μs/div Therefore, the dynamic response of the current sharing is very fast for a parallel system: less than 150 μs for this experiment. For comparison, in the benchmark circuit we built with UC3907, the current sharing setting time is more than 2 ms, which is more than ten times slower. The output voltage during the step load from 0 to 20 A is shown in Fig. 9.

Steady State Current Sharing: Fig. 10 shows the current sharing at steady states. This method obtains current sharing by equalizing the reference to the inner current sources of converters. For the peak current mode control, the parameter tolerance, such as the inductance difference of the output filter, will result in current sharing error [23]. However, such error is normally acceptable from the point view of system design.

Finally, the analysis above shows that only the current sensing gain R_S, voltage feedback resistor network, the trim resistor of the converter and the loop gain are needed for system design. Therefore, this method is simple and can be easily used by system designers.

VI. Conclusion

This paper proposes a new current sharing method. The method utilizes the inner current source property of CMC dc–dc converters to achieve the current sharing. Meanwhile,

the modularity of the converter is maintained, and the control loops within all dc–dc converter work normally. The system design is simple because the method decouples control loops from the voltage regulation and current-sharing regulation instead of adding additional control loops as in the traditional method. As a result, the dynamic performance is guaranteed in both the large and small signal sense. This is supported by experimental results.

Finally, this method uses minimum-master bus in order to incorporate the structure of UC3843. In fact, maximum-master bus can also be implemented with the same methodology.

APPENDIX
STABILITY ANALYSIS WHEN T IS LOW-PASS FILTER

Because T is almost always designed as a low-pass filter, the conclusion from the ideal case, (19), may not be true in real application. For example, the low-pass filter will introduce phase lag in the control loop. This appendix will analyze the stability of the proposed method with T as a low-pass filter. For simplicity, Fig. 4(b) of two converters in parallel is studied.

First, the minor loop gain is

$$T_{\text{minor}} = HTA_V \tag{A1}$$

where A_V is a transfer function of the voltage controller in a well-designed dc–dc converter and stable. Meanwhile, it has been shown that H is a small gain. Therefore, when T is a low-pass filter with dc gain of 1, the minor loop can still be decoupled from the voltage control loop. As a result, H can still be ignored in following small signal analysis.

When the influence of H is ignored, the outer voltage control loop gain of the slave with that of the master closed is

$$\begin{aligned} T_{\text{V,slave}} &= \frac{\frac{1}{3}A_V B F_I \frac{Z}{2}(1-T)}{1+\frac{1}{3}A_V B F_I \frac{Z}{2}(1+T)} \\ &= \frac{\frac{1}{2}T_V(1-T)}{1+\frac{1}{2}T_V(1+T)} \end{aligned} \tag{A2}$$

where, in Fig. 1

$$T = \frac{1}{1+RCs} \tag{A3}$$

and T still has a dc gain of 1. The outer voltage control loop gain of the master with that of the slave closed is

$$\begin{aligned} T_{\text{V,master}} &= \frac{\frac{1}{3}A_V B F_I \frac{Z}{2}(1+T)}{1+\frac{1}{3}A_V B F_I \frac{Z}{2}(1-T)} \\ &= \frac{\frac{1}{2}T_V(1+T)}{1+\frac{1}{2}T_V(1-T)}. \end{aligned} \tag{A4}$$

Obviously, $T_{\text{V,slave}}$ and $T_{\text{V,master}}$ should have enough phase margin to guarantee the stability of system. It should be noted that above results ignore the influence of H.

With the parameters in Fig. 1, the crossover frequency of T is set close to the crossover frequency of T_V. From (A2), there is $|T_{\text{V,slave}}| < 1$ at all frequency range. That is, $T_{\text{V,slave}}$ is always stable. In fact, the magnitude of $T_{\text{V,slave}}$ is a very small number considering $|T(S)| \approx 1$ at low frequency, and its effects can be ignored.

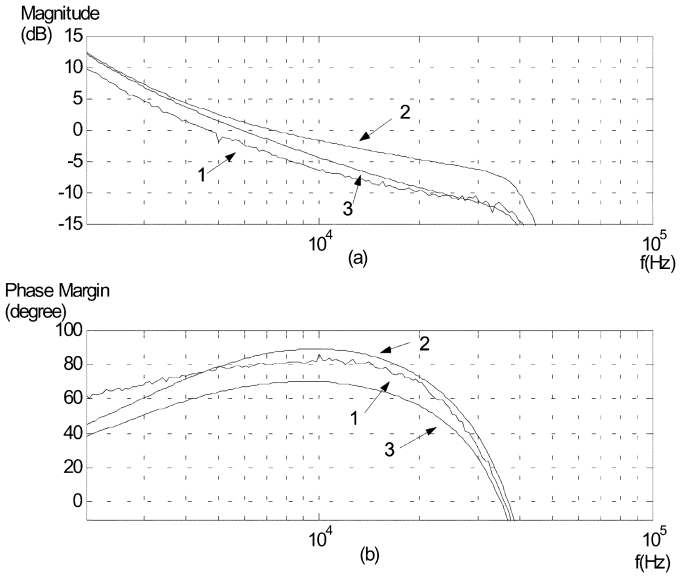

Fig. 11. Comparison of loop gains Curve 1 is $T_{\text{V,master}}$; Curve 2 is the individual T_V of the stand-alone converter; Curve 3 is the calculated result of (A4) when the denominator is ignored (a) magnitude in dB and (b) phase margin in degree.

On the other hand, it is $T_{\text{V,master}}$ that is affected by T noticeably and shall be studied quantitatively. One possible small signal analysis method is to build the small signal model of individual converter and to obtain T_V. Then $T_{\text{V,master}}$ is calculated with the knowledge of T. However, the small signal model is suspected because of necessary ideal assumptions and approximations in modeling. Further, in parallel system design, the dc–dc converters are viewed as components:A_V has been well designed and is available in most cases. Therefore, it is desired that A_V be used directly.

In this research, the prediction method in [24] is used for small signal analysis. First, A_V is measured, and small signal transfer function is calculated based on (A4) with the model of T, e.g., (A3). The prediction results are shown in Fig. 5.

It is worth noting that, in Fig. 4(b), the low-pass filter is between the current reference x and the inner current source of the slaves and will introduce a phase lag in the power train. This may reduce the phase margin of the outer voltage loop. Fortunately, there is the same low-pass filter in the outer voltage control loop of the slave. That is, when the low-pass filter in the master cannot be ignored, the same low-pass filters in the slaves cannot be ignored. At that time, the low-pass filter in the slave will counteract the detrimental effect of the low-pass filter in the master.

Fig. 11 verifies this conclusion by the comparison: Curve 1 is the typical T_V while Curve 2 is $T_{\text{V,master}}$. Curve 3 is the calculated result if the effects of the outer voltage control loop in the slave are omitted. It shows that the phase margin of the real loop gain of the master, Curve 2, is improved by the feedback loop in the slave. It is almost the same as that of single converter. However, the crossover frequency is lowered a little bit. Therefore, the proposed design method can easily guarantee stability. Further, with the proposed small signal model, the output impedance of the parallel system can also be calculated with the similar methods in [3], [10], [11].

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