Accurate Loop Gain Prediction for DC–DC Converter Due to the Impact of Source/Input Filter

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***Abstract*—This paper presents methods to accurately predict loop gains in dc–dc converters when arbitrary impedance is added to the input of a dc–dc converter. A step-by-step procedure is presented to implement the methods, which can also be developed in a CAD tool. Online evaluation is also presented. Experimental data verify the proposed approach.**

***Index Terms*—CAD, dc–dc converters, filter, impedance, stability.**

I. Introduction

FIG. 1(a) is a typical application of a switching mode dc–dc converter. The output impedance of the source is Z_S. The dc–dc converter has a built-in input filter, and, in some applications, an external input filter is required to meet electromagnetic interference (EMI) requirements. The input filter may deteriorate the performance of the dc–dc converter, and its impact on dc–dc converters has been studied based on small signal models [1]–[5].

On the other hand, from the point of view of the dc–dc converter in Fig. 1(a), the source impedance and external input filter can be lumped together as one impedance, Z. Likewise, when a dc–dc converter is used in a distributed power system (DPS), as shown in Fig. 1(b), Z can be used to lump the output impedance of the input filter, the output impedance of the source, Z_S, the impedance of other loads, $Z_{L1}, \ldots, Z_{Ln}$, and the impedance of the distribution lines [6].

Therefore, in system design, when a power supply customer adds the additional Z to the input side, the customer needs to know the impact of the impedance on the performance of the dc–dc converter. Until a few years ago, most design rules for DPS were based on impedance ratios, Z_S/Z_L [1], [7]–[10] or, similarly, admittance [11]. These methods recognize that the stability of a converter is not influenced when the impedance ratio is sufficiently small. Thus, criteria known as forbidden regions are created that restrict the permitted values of the impedance ratio in the complex plane. However, these rules were known to be conservative, and different forbidden regions are proposed to improve the conservativeness [8]–[11]. Furthermore, these design rules tend to only guarantee the stability of the system and do not indicate performance information,

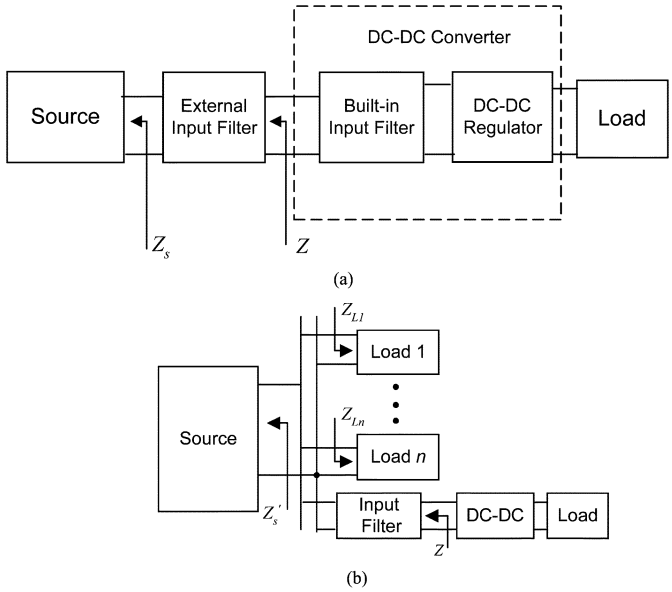

Fig. 1. Typical dc–dc converter applications (a) in general form (b) in distributed power system.

such as changes in bandwidth or gain/phase margins of loop gains. As a result, sometimes the customer/user have to ask the power supply manufacturer to directly test performance of the converter of their specified system. The manufacturer normally must perform these experiments (not the customer), since they require loop gain measurements and the "breaking" of the converter's internal circuitry.

Recently, a new approach has been proposed to determine partial (source converter only) performance characteristics in DPS [12]–[15]. Instead of trying to prevent interactions between the different converters in Fig. 1, this approach focuses on how to precisely predict the influence of the interaction and prevents only detrimental interactions through proper control loop design. The approach first obtains nominal small signal data of the dc–dc converter without the additional load impedance. Given these nominal data, which are easily obtained, it is possible to predict changes of the loop gain when impedance is added to the load. Because the approach is only predicting changes in performance, instead of attempting to model the entire system performance, the results have been shown to be extremely accurate. Thus, conservative restrictions of [7]–[11] can often be removed, leading to new design rules for source converters in a DPS [14] and for target impedance design [12], [13], [15]. However, its major shortcoming is that the design and modeling methods are only applicable to the source converter in a DPS.

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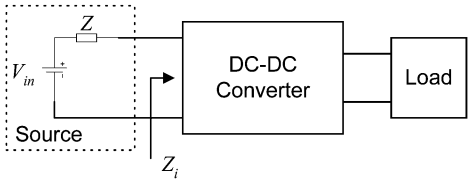

Fig. 2. DC–DC converter with arbitrary source.

Presently, there exists no method to accurately predict the loop gain of a dc–dc converter for arbitrary source impedance, other than actually measuring the loop gain with the source impedance. However, this normally requires breaking open the dc–dc converter and cannot be performed by the customer. Thus, only the manufacturer of the converter is able to measure the loop gain. The purpose of this paper is to demonstrate that with only a few nominal measurements of the converter, it is possible to accurately predict the loop gain for any source impedance without directly measuring the loop gain of the dc–dc converter when the source impedance is attached. In essence, this paper extends the methodology of [12]–[14] to predict the impact of external impedance placed on the input of the dc–dc converter. The theoretical/analytical foundation of the proposed prediction method is more complicated than that in [12]–[14]. It relies on the combination of two-port system models with impedance interaction principles [7]. Similar to [12]–[14], the approach is based on nominal data to predict loop gain T_Z for arbitrary Z. The user only needs to generate the frequency characteristics of Z. Therefore, there is no need to break any internal circuitry of the dc–dc converter, and the results are NOT conservative because they predict performance instead of creating general stability conditions. Moreover, the proposed method can be simply implemented in step-by-step procedures or a CAD tool. The CAD tool, relying on nominal measurements of the converter supplied by the manufacturer, automatically calculates T_Z for the desired converter. Besides performance prediction, the method can also be used for on-line evaluation of T_Z for an existing system.

Section II of this paper presents the prediction formula for loop gains. Section III shows the applications of the prediction formula, which includes step-by-step procedures and on-line evaluation. Section IV extends the method to predict other small signal properties in the converters such as audio susceptibility and output impedance. The experimental results verify the method in Section V. Conclusions are given in Section VI. The details of the theoretical derivation, which represent a principle contribution of this research, are shown in Appendix.

II. Performance Prediction

The systems in Fig. 1 can be redrawn using Thevenin equivalent circuits to be in the general form of Fig. 2. In this figure, Z_i is the input impedance of the converter, and Z is the lumped impedance in Fig. 1. Let T_Z denote any loop gain in the converter when there is impedance Z at the input. The loop gain T_Z can be the outer voltage loop, the inner current loop, or any other arbitrary loop gain. Because of the impact of Z, T_Z may not satisfy original performance specifications.

Therefore, the problem can be described as (refer to Fig. 2) follows.

Suppose nominal (without Z) small signal performance of the dc–dc converter is known. Determine the new loop gain T_Z, when Z is added.

Once T_Z is known or predicted, it is possible to guarantee relative stability conditions such as phase margin and gain margin of the loop gain, without using conservative design rules.

Specifically, for the system in Fig. 2, let Z_i and Z be as shown. Define T_∞ to be any loop gain when Z is infinite, and T_0 is the same loop gain when Z is zero. When a converter is designed, Z_i, T_∞ and T_0 are determined and will not be changed by Z. Therefore, Z_i, T_∞ and T_0 are called as nominal values.

Assume the nominal values are known or supplied by the manufacturer. Then for any value of Z, the specified loop gain of the dc–dc converter becomes (see Appendix A)

$$T_Z = \frac{(1+T_\infty)\left(1+\frac{Z_i}{Z}\right)}{1+\frac{Z_i}{Z}\frac{1+T_\infty}{1+T_0}} - 1. \tag{1}$$

Notice that the right-hand side of (1) relies on Z and on known nominal values of the dc–dc converter that are independent of Z. Therefore, if the manufacturer provides Z, T_∞ and T_0, it is a simple calculation to compute T_Z. A simple CAD tool has been designed to perform this calculation. Furthermore, it is realistic to expect that the manufacturer is willing to supply these nominal values: Already power supply companies have made similar data available to telecommunication customers to determine the influence of additional capacitor banks added to the load in order to meet the target impedance [12]–[18].

How to Obtain Nominal Values?: Critical to implementation of (1) is the ability to obtain the nominal values of several small signal transfer functions: the nominal impedance, Z_i, is the input impedance of the dc–dc converter, which can be measured directly. By definition, T_0 is the loop gain when Z is zero (in the small signal sense). That is, T_0 is a loop gain (outer voltage, inner current or any other) measured with an ideal voltage source. An approximation of T_0 can be obtained by measuring the loop gain when the input of the converter is directly supplied by a low impedance voltage source. This is verified in (1) by letting $Z = Z_S \ll Z_i$ and solving for $T_z(\approx T_0)$.

Determining T_∞, though, is sometimes not so simple because T_∞ is the loop gain when Z is infinite (in the small signal sense). That is, T_∞ is the loop gain measured with an ideal current source as input. However, dc–dc converters are designed for voltage source inputs and may even be unstable when connected directly to a current source. Therefore, the manufacturer must derive T_∞ indirectly: a voltage source with known impedance is used to supply the input voltage of a dc–dc converter. The loop gain T_Z, along with the source impedance Z, is then measured. Z_i and T_0 are measured as previously described. Then (1) is used to solve for T_∞.

Alternatively, T_∞ and T_0 can be obtained, without approximation, by using (1). Assume two voltage sources with different output impedance Z_A and Z_B are used to supply the converter, respectively. Then the loop gains T_A and T_B under the different additional impedance are measured. With the knowledge of Z_i,

it is easy to use (1) to calculate T_∞ and T_0. Specifically, there are

$$T_0 = 1 - \frac{(1-T_A)(1-T_B)(\beta_A-\beta_B)}{(1-T_B)(1+\beta_A)-(1-T_A)(1+\beta_B)} \quad (2)$$

$$T_\infty = 1 - \frac{(1-T_A)(1-T_B)(\beta_B-\beta_A)}{(1-T_B)\beta_B(1+\beta_A)-(1-T_A)\beta_A(1+\beta_B)} \quad (3)$$

where $\beta_A = (Z_i/Z_A)$ and $\beta_B = (Z_i/Z_B)$. A CAD program has been developed to perform this calculation, as described in Section V.

Although indirect, this approach has proved to be accurate. Moreover, an important benefit of the approach is that these nominal measurements need to be taken only once. That is, the small signal behavior of the converter is characterized (by the manufacturer) once without additional Z, and then it is possible to accurately predict the new T_Z for arbitrary Z without taking additional loop gain measurements inside the converter.

III. Applications

A. Step-by-Step Procedure

The step-by-step procedure of the prediction formula can now be given. The general approach is similar to the approaches in [12]–[14], since the procedure is to first obtain nominal measurements and then to input the measurements into a CAD program to predict new loop gains. On the other hand, the algorithm below requires additional measurements and has more complicated prediction formula than [12]–[14], as Appendix A shows.

Step 1) Take sample measurements of nominal small signal behavior.

As discussed above, obtain the nominal input impedance, Z_i, and the nominal loop gains, T_0 and T_∞, of the dc–dc converter for sample load and line conditions. Specifically, we measure for high line/low load, high line/medium load, high line/low load, medium line/low load, low line/medium load, and low line/ low load. Hence, we are attempting to characterize the nominal dc–dc converter behavior without the knowledge of Z. The nominal values can be supplied by the manufacturers of the dc–dc converter.

Step 2) Import measurement data into software program.

Step 3) In software, calculate T_Z with the prediction formula

$$T_Z = \frac{(1+T_\infty)\left(1+\frac{Z_i}{Z}\right)}{1+\frac{Z_i}{Z}\frac{1+T_\infty}{1+T_0}} - 1.$$

Experimental data of input impedance, Z_i and the nominal outer loop gains, T_0 and, T_∞ are already known (for specific line conditions) and may be imported into the software program. We are interested in understanding the effects of the impedance Z on the new loop gain T_Z. Hence, a software program (we use MATLAB) calculates the loop gain for any possible Z, using the above formula to predict T_Z. With this new loop gain, the program can then easily calculate the phase margin, crossover frequency, and gain margin of T_Z. The user has the option to vary Z by software, or to input measured Z of an actual system.

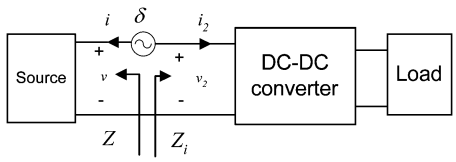

Fig. 3. Online evaluation.

B. On-Line Evaluation

Notice that (1) uses the ratio of nominal impedance and the output impedance of the source for prediction. Therefore, instead of obtaining nominal impedance and the output impedance of the source separately, we can measure the ratio directly.

Fig. 3 shows an on-line measurement method. A small signal perturbation, δ, is injected between the source and the converter. There are

$$Z = \frac{v}{i}; \quad Z_i = \frac{v_2}{i_2}.$$

Meanwhile, because $i = -i_2$, there is

$$\frac{Z_i}{Z} = -\frac{v_2}{v} \equiv \text{impedance ratio } \beta$$

and (1) can be written as

$$T_Z = \frac{(1+T_\infty)(1+\beta)}{1+\beta\frac{1+T_\infty}{1+T_0}} - 1. \quad (4)$$

Therefore, for an existing system, (4) can be used for performance evaluation. The inner circuit is not needed to be broken to measure the loop gains. Instead, only a perturbation injected into the distribution line and measurement outside the module is needed. Details of setup of similar on-line evaluation can be found in [13].

IV. Further Discussions

The output impedance of the source will also change other small signal properties such as audio susceptibility and output impedance [1]–[5]. These properties can also be predicted with a similar prediction formula (see Appendix B). Let H_Z represent either audio susceptibility or output impedance. Then when additional Z is added to the input

$$H_Z = \frac{H_\infty + \frac{Z_i}{Z}H_0}{1+\frac{Z_i}{Z}} \quad (5)$$

where Z_i is the input impedance of the dc–dc converter similar to before. H_∞ represents the audio susceptibility or output impedance when Z is infinite, and H_0 represents the audio susceptibility or output impedance when Z is zero. Equation (5) can also be implemented in prediction or on-line evaluation. It is worth noting that the nominal impedance in either (1) or (5) is the same. Therefore, no matter which small signal property is considered, the same impedance ratio is used, which simplifies the application of prediction and on-line evaluation.

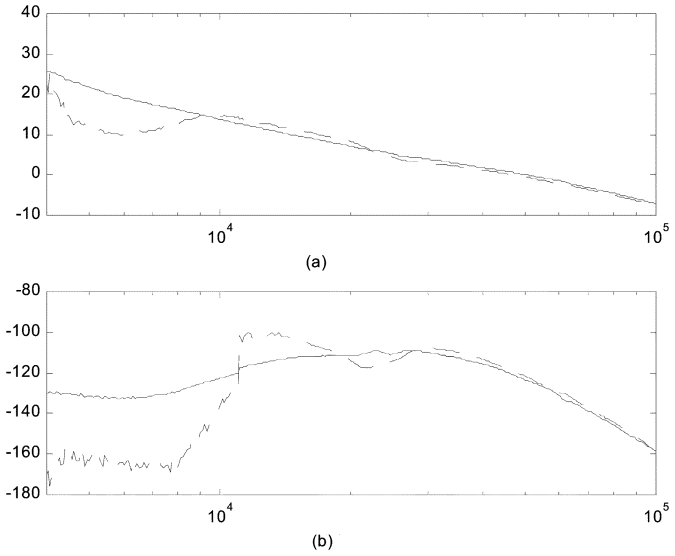

Fig. 4. Nominal loop gains T_∞ (dash) and T_0 (solid) of the outer voltage loop of the tested POL converter (a) magnitude in dB versus frequency in Hz (b) phase in degree versus frequency in Hz.

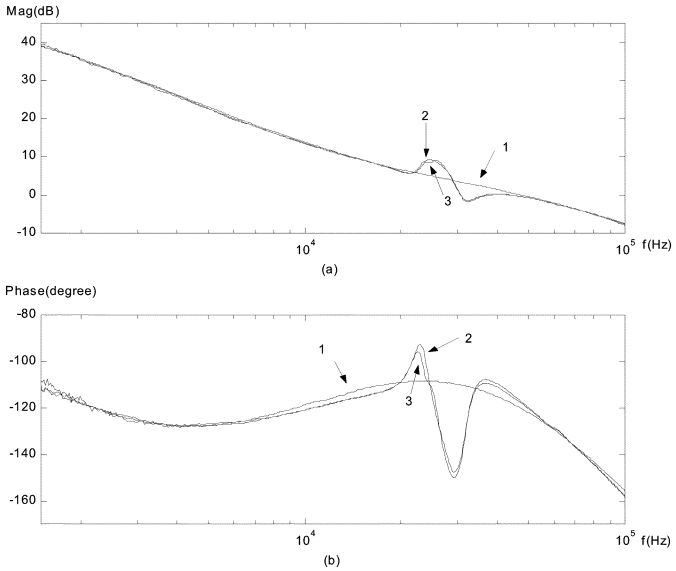

Fig. 5. Measured and predicted outer loop gains of the tested POL converter (a) magnitude in dB and (b) phase in degree curve 1 is the outer loop gain under specified design condition; curve 2 is the measured outer loop gain with HP6030A; curve 3 is the predicted outer loop gain with HP6030A.

The nominal values can be obtained by the same procedure of (1). Especially, when Z is infinite, $H_\infty = 0$ for audio susceptibility analysis. Therefore, for audio susceptibility, (5) can be simplified as

$$H_Z = \frac{Z_i H_0}{Z + Z_i} \tag{6}$$

which is the same results as [1]–[3]. Appendix B describes the general theory/approach for predicting general performance transfer functions in dc–dc converters.

V. Experimental Results

A point-of-load (POL) dc–dc converter is designed to verify the proposed method. This converter is a current mode controlled converter and has 3.3-V input and 1.9-V output. In the design phase, the source is specified as an off-the-shelf 48-V/3.3-V forward current mode converter. Fig. 4 shows the nominal loop gains, T_∞ and T_0, of the POL's outer voltage loop. With the forward converter as its source, the tested POL converter has outer loop gain with phase margin 59.7° and crossover frequency 47.50 KHz. Fig. 5 shows the outer-loop gain of the POL converter (Curve 1) under these circumstances.

Suppose it is desired to determine the outer-loop gain of the POL converter when it is directly supplied by a HP6030A dc power supply. Curve 2 in Fig. 5 is the measured outer loop gain, while Curve 3 is the predicted outer loop gain by (1). The figure shows that the outer loop gain of the POL converter with HP6030A has a substantial phase and gain change around the crossover frequency, which points out a noticeable performance degradation. Specifically, the phase margin is changed to 38.2° and the crossover frequency is changed to 30.74 KHz. On the other hand, the predicted and measured loop gains are nearly superimposed upon each other in Fig. 5. The predicted phase margin is 37.1°, and the predicted crossover frequency is 30.70 KHz. The method used to predict T_Z is the same as given in Section III. The user is only required to input Z (the impedance of HP6030A) into the developed program. Software then provides T_Z, along with its crossover frequency and phase margin by using (1). As Fig. 5 indicates, the method is accurate. (The figures illustrate a frequency range from 1 to 100 KHz in order to magnify the frequency range of interest, i.e., where the crossover frequency resides.)

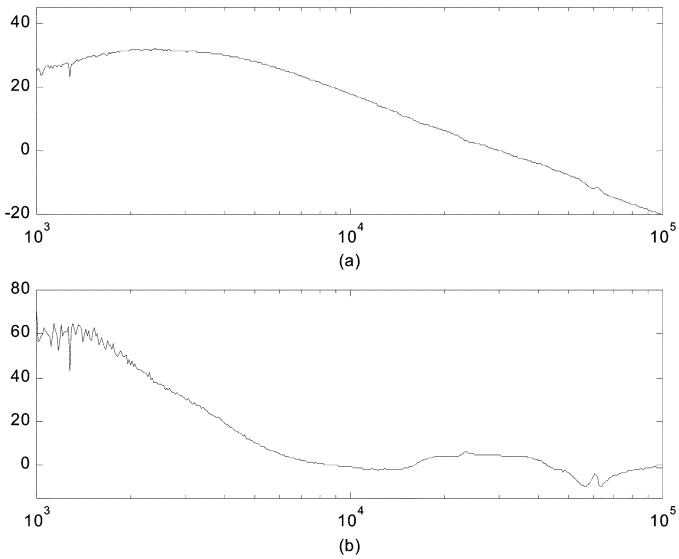

Fig. 6. Measured negative impedance value $(-\beta)$ (a) magnitude in dB versus frequency in Hz and (b) phase in degree versus frequency in Hz.

The loop gain can also be calculated by (2) with the impedance ratio $\beta = (Z_i/Z)$. Fig. 6 shows the impedance ratio. In the conservative design rules [1], the change of small signal properties of a converter is negligible when β is large, i.e., if the magnitude of the output impedance of the source is much smaller than that of the input impedance of the converter. Fig. 6 shows that, at low frequency range (below 5 KHz), the design rules of [1] are satisfied. Therefore, the loop gain changes little

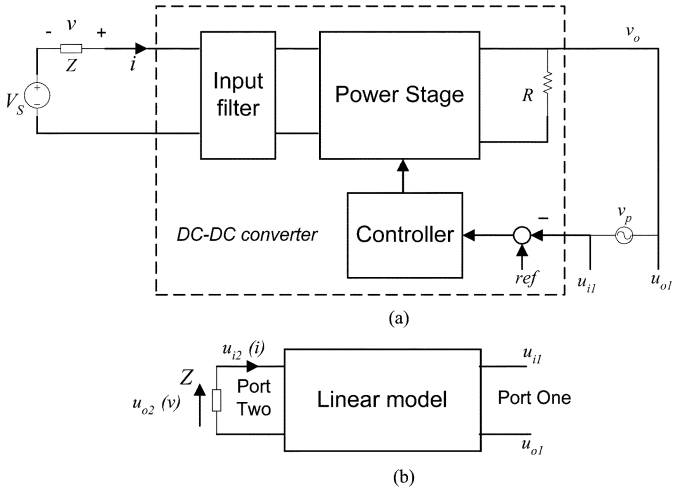

Fig. 7. (a) Impact of source, Z, on the outer loop gain and (b) two-port linear model for (a).

in Fig. 5 in this low frequency range, and the design rules can be viewed as a conservative approximation of (1).

VI. Conclusion

Loop gain prediction of dc–dc converters due to source/input filters is discussed. It is shown that, given any nominal loop gain and some other nominal measurements, it is possible to accurately predict new loop gains when arbitrary impedance is added to the input of the converter. A step-by-step method is presented to implement the procedure. The approach does not require the breaking of any internal circuitry in the converter. On-line evaluation is also possible. The prediction method is also extended to other small signal properties. Experiments validate the proposed approach.

Appendix A
Prediction of Change of Loop Gains

A dc–dc converter is designed as a stand-alone system, and its performance is guaranteed under the specified source condition. However, in real applications, the output impedance of the source may not meet the requirements, and the impedance interaction between the converter and the source will change the converter's performance [7]. Such performance change shall be studied. Fig. 7(a) shows a dc–dc converter with arbitrary source. The output impedance of the source is given as Z

Fig. 7(a) shows the outer loop gain measurement as an example. (Any loop gain will satisfy the below theoretical deviation.) A small signal perturbation V_p is injected into the outer control loop, and the ratio of u_{i1} and u_{o1} is the loop gain. Usually a feedback loop gain is represented as its open loop transfer function with additional negative sign and termed as T. Therefore, the outer loop gain in Fig. 7(a) is $T = -(u_{o1}/u_{i1})$.

When the loop gains of the dc–dc converter are studied, the converter is set at an operating point and based on its small signal linear model. Therefore, Fig. 7(a) can be simplified as a two-port linear system, as shown in Fig. 7(b). Port One represents the loop gain of the converter, which is shorted in normal operation. u_{il} and u_{ol} are the input and output of the loop gain, respectively, as shown in Fig. 7(a). Port Two represents the input of the converter: u_{i2} is a current into the converter, i, and u_{o2} is voltage across the input, v. Therefore, the transfer function from u_{i2} to u_{o2} is the input impedance of converter. Define

$$\begin{pmatrix} u_{o1} \\ u_{o2} \end{pmatrix} = \begin{pmatrix} A_1 & A_2 \\ B_1 & B_2 \end{pmatrix} \begin{pmatrix} u_{i1} \\ u_{i2} \end{pmatrix} \tag{A1}$$

where

$$A_1 = \left.\frac{u_{o1}}{u_{i1}}\right|_{u_{i2}=0} \tag{A2}$$

$$A_2 = \left.\frac{u_{o1}}{u_{i2}}\right|_{u_{i1}=0} \tag{A3}$$

$$B_1 = \left.\frac{u_{o2}}{u_{i1}}\right|_{u_{i2}=0} \tag{A4}$$

$$B_2 = \left.\frac{u_{o2}}{u_{i2}}\right|_{u_{i1}=0} \tag{A5}$$

u_{i1} and u_{i2} and are the independent input signals, while u_{o1} and u_{o2} are the output signals. If the two inputs are nonzero, the output will be a superposition of response to the two inputs.

Therefore, the impact of Z on the loop gain can be described as:

For a two-port linear system, as shown in Fig. 7(b), Port One represents a loop gain, which is shorted at normal operation of the system. When an impedance Z is attached to Port Two of the system, what is the loop gain $T_Z = -(u_{o1}/u_{i1})$?

Obviously, when an impedance, Z, is placed across Port Two of the linear system, as shown in Fig. 7(b), there is

$$u_{o2} = -Zu_{i2}. \tag{A6}$$

Substitute (A6) into (A1), and there is

$$T_Z \equiv -\frac{u_{o1}}{u_{i1}} = -A_1 \frac{1 + \frac{1}{Z}\frac{A_1B_2 - A_2B_1}{A_1}}{1 + \frac{1}{Z}B_2}. \tag{A7}$$

Therefore, T_Z can be easily predicted if the parameters in (A1) are known. Theoretically, the parameters in (A1) can be obtained by setting one input zero. However, for a dc–dc converter, those parameters are very difficult to be measured in experiments. Therefore, instead of obtaining the parameters directly, it will be better if (A7) is represented by other parameters that can be measured easier.

Further, performance degradation originates from impedance interaction. Especially, in Fig. 7(b), the change of the loop gain is due to the interaction of Z and the input impedance of Port Two. Therefore, it is helpful to predict the performance change by the impedance interaction directly. Meanwhile, the input impedance of the converter is the input impedance of the converter in its normal operation, and it can be measured directly.

Based on above analysis, it is possible to define the following quantities, which only depend on the parameters of (A1).

1) *Nominal Impedance*, Z_i

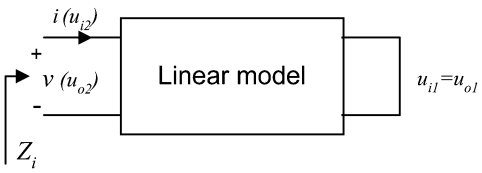

Fig. 8. Nominal impedance when port one is shorted (loop gain).

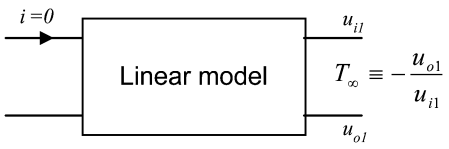

Fig. 9. Open loop gain, T_∞.

The input impedance of Port Two is determined by the parameters of the system and the input signal at Port One. Define the input impedance of Port Two as nominal impedance when the Port One resembles the normal operation of the system, which is shorted for feedback loop gains, as shown in Fig. 8. That is

$$u_{i1} = u_{o1}. \tag{A8}$$

Substituting (A8) into (A1), the nominal impedance is

$$Z_i \equiv \frac{u_{o2}}{u_{i2}} = B_1\frac{A_2}{1-A_1} + B_2 = \frac{B_2 + A_2B_1 - A_1B_2}{1-A_1}. \tag{A9}$$

2) *Open Loop Gain*, T_∞

Define the loop gain (of Port One) as open loop gain, T_∞, when the additional impedance Z is infinite. In this case, the input of Port Two is zero, as shown in Fig. 9 That is

$$u_{i2} = 0. \tag{A10}$$

Putting (A10) into (A1) leads to

$$T_\infty \equiv -\frac{u_{o1}}{u_{i1}} = -A_1. \tag{A11}$$

When the input of Port Two is current, zero input means leaving Port Two open. Further, if the system has dc bias, the input of Port Two should be a constant current, and, in small signal sense, Port Two is left open.

3) *Closed Loop Gain*, T_0.

Define the loop gain (of Port One) as closed loop gain, T_0, when the additional impedance Z is zero. In this case, the output of Port Two is zero, as shown in Fig. 10 That is

$$u_{o2} = 0. \tag{A12}$$

Substituting (A12) into (A1), there is

$$T_0 \equiv -\frac{u_{o1}}{u_{i1}} = -A_1 + \frac{A_2B_1}{B_2}. \tag{A13}$$

When the output of Port Two is voltage, zero output means shorting Port Two. Further, if the system has dc bias, the output of Port Two should be a constant voltage, and, in small signal sense, Port Two is shorted.

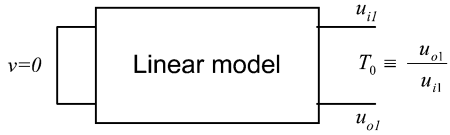

Fig. 10. Closed loop gain, T_0.

Adding one on both sides of (A7) gives

$$\begin{aligned} T_Z + 1 &= -A_1\frac{1+\frac{1}{Z}\frac{A_1B_2-A_2B_1}{A_1}}{1+\frac{1}{Z}B_2} + 1 \\ &= A_1\frac{\left(\frac{1}{A_1}-1\right)+\frac{1}{Z}\frac{B_2-A_1B_2+A_2B_1}{A_1}}{1+\frac{1}{Z}B_2} \\ &= (1-A_1)\frac{1+\frac{1}{Z}\frac{B_2+A_2B_1-A_1B_2}{1-A_1}}{1+\frac{1}{Z}B_2}. \end{aligned} \tag{A14}$$

Substituting (A9), (A11) and (A13) into (A14) leads to

$$T_Z = \frac{(1+T_\infty)\left(1+\frac{Z_i}{Z}\right)}{1+\frac{Z_i}{Z}\frac{1+T_\infty}{1+T_0}} - 1. \tag{A15}$$

Here, Z_i, T_∞ and T_0 are termed as nominal values because they are determined by the system itself.

When (A15) is directly used in applications.

1) The nominal impedance, Z_i, is the input impedance of the converter in normal operation, and it can be measured directly. Moreover, although different loop gains mean different models for a system, they have the same nominal impedance. (This is still true for the results in Appendix B.)
2) Equation (A15) uses Z_i and Z in calculation, which are the causes of performance changes, i.e., impedance interaction [1], [7] causes performance degradation. The explicit dependence on (Z_i/Z) in (A15) brings intuition into the analysis and simplifies design and analysis.
3) Equation (A15) uses the ratio of Z_i and Z in calculation, and it can be applied directly on on-line evaluation.
4) Z usually affects more than one loop gain of the system. The affected loop gains have the same nominal impedance. Therefore, the designer can use sensitivity analysis to determine which loop gain tends to be affected by the parameter derivation of the impedance interaction. This information may improve the design of the system.
5) Equation (A15) is not limited on predicting the impact of the source impedance on loop gains of dc–dc converters. In fact, it is a general result that can be applied to the loop gains of any linear system with an additional impedance.

APPENDIX B
PREDICTIONS OF AUDIO SUSCEPTIBILITY AND IMPEDANCE

Sometimes it is necessary to consider the impact of additional impedance on other properties, such as audio susceptibility and output impedance. In these cases, the transfer function of Port One in Fig. 7 is the audio susceptibility or the output impedance, and the input of Port One is zero in normal operation of the system.

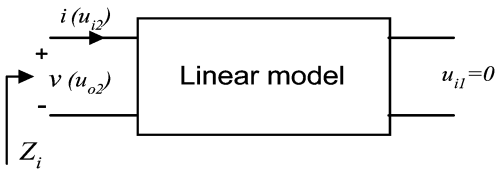

Fig. 11. Nominal impedance when port one is left open.

First the nominal values must be defined. Nominal impedance is still defined as the input impedance of Port Two when the Port One resembles the normal operation of the system. However, unlike the results in Appendix A, the input of Port One is zero in normal operation, as shown in Fig. 11 That is

$$u_{i1} = 0. \tag{A17}$$

Substituting (A17) into (A1), the nominal impedance is

$$Z_i = B_2. \tag{A18}$$

It is worth noting that although the nominal impedance in (A9) and (A18) are in different forms, they are actually equal. Both are the input impedance of Port Two in the normal operation of the system. The reason for the different forms is that, even for the same system, transfer functions have different meaning in (A1).

Similar to the definition of open loop gain, T_∞, and closed loop gain, T_0 in Appendix A, open gain H_∞ and closed gain H_0 is defined. The results are the same as (A11) and (A13) without the additional negative sign. That is

$$H_\infty \equiv \frac{u_{o1}}{u_{i1}} = A_1 \tag{A19}$$

$$H_0 \equiv \frac{u_{o1}}{u_{i1}} = A_1 - \frac{A_2 B_1}{B_2}. \tag{A20}$$

When additional impedance is place across Port Two, as shown in Fig. 7, the transfer function of port One is (A7). That is

$$H_Z \equiv \frac{u_{o1}}{u_{i1}} = A_1 \frac{1 + \frac{1}{Z}\frac{A_1 B_2 - A_2 B_1}{A_1}}{1 + \frac{1}{Z} B_2}. \tag{A21}$$

Substituting (A18)–(A20) into (A21) leads to

$$H_Z = \frac{H_\infty + \frac{Z_i}{Z} H_0}{1 + \frac{Z_i}{Z}}. \tag{A22}$$

In this appendix, two-port modeling is used as a basis to derive the final results. This methodology has seen widespread applications in different fields, and the methodology in the appendix resembles Middlebrook's extra element theorem (EET) [19]. However, different from the EET, the proposed method relies on transfer functions that can easily be measured and have direct meaning for dc–dc converters. In some sense, the results in this appendix can be viewed as an alternative experimental extra element theorem that is suitable for on-line implementation and evaluation when applied to power electronic systems.

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