Self-Driven Synchronous Rectification Scheme for Wide Range Application of DC/DC Converters with Symmetrically Driven Transformers[1]

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Abstract: Synchronous rectifiers are widely used in low voltage and high current DC/DC converters to reduce conduction power loss. For popular and reliable topologies, such as Half-bridge, Push-pull and Phase-shifted Full-bridge, the application of self-driven synchronous rectification has design challenges due to the existence of dead times. Existing solutions are not suitable for wide input voltage ranges. This paper presents a new self-driven scheme which properly combines the signal from the transformer and output inductor to drive the MOSFETs. This method provides a suitable solution for wide range input application, since the risk of exceeding the gate voltage rating is greatly reduced. The synchronous rectifier is driven during all the conduction period, and thus greatly reduces the power loss. The influence of the leakage inductance in practical application is also analyzed. Experimental results based on a 36-75V input, 2.5V/30A output prototype are shown to verify the proposed scheme.

I. INTRODUCTION

Synchronous rectification is an important technique to reduce the conduction loss for low output voltage converters [1-6]. Due to the demands of low supply voltage and high current for power converters, it is hard to achieve an efficiency over 90% by utilizing Schottky Diodes, since forward voltage drops of more than 0.3V can cause too much loss. Small-package MOSFETs, on the other hand, have on-resistances of the order of milli-ohms.

Presently, synchronous rectifiers (SR's) are widely utilized in both isolated and non-isolated DC/DC converters. However, this paper focuses in isolated topologies. Typically, there are two kinds of driving strategies for isolated converters: self-driven methods that obtain the driving signal directly from the secondary side of the transformer, and control-driven algorithms that drive MOSFETs by using signals from the controller.

It is important to choose proper driving methods for synchronous rectifiers primarily because of two factors: Firstly, because the MOSFETs cannot block reverse current automatically like diodes, the timing of the driving signal must be designed carefully to turn on and turn off the synchronous rectifiers properly. Secondly, in order to really improve the efficiency of the converter, deadtimes and transition times of the SRs should be as short as possible. Since, the concept of a synchronous rectifier is to utilize MOSFETs instead of diodes, the ideal result is to drive the MOSFETs during their entire conduction period.

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An obvious advantage of self-driven methods is that there is no need to worry about the isolation problem for the driving transformers, especially when the isolation requirement between the input and output is very high. Also, it is easier to generate a driving signal, since it is taken directly from the secondary side of the power transformer. For those topologies with no deadtime operation, such as Active-clamped Forward, Flyback and Asymmetrical Half-bridge, there is no problem for the implementation of self-driven synchronous rectifiers. However, some very popular and reliable topologies, such as Half-bridge, Push-pull and Phase-shifted Full-bridge, have deadtimes in their transformer waveforms. Special attention must be paid to turn on MOSFETs during deadtimes when using self-driven method. Therefore, it is an important challenge to create suitable self-driven SR methods for these topologies. (Deadtime is defined as the time interval in which there is no direct energy connection/flow from input to output. For these isolated buck derived topologies, the deadtime is the (1-D)T interval where D is the duty ratio, i.e., when the primary switches are off, and no energy is applied to the primary transformer.)

To address some of these issues, recent research proposes [3-4] that an additional winding to the transformer may be connected to the gates of both SRs, and one diode can be paralleled between the gate and the source of each SR. These methods depend heavily on the transformer design. Further, the coupling between windings is very critical. A good solution for self-driven SR is to add a regulated voltage on the secondary side of the symmetrically driven transformer to help drive the MOSFETs [5]. This method can effectively extend the conduction period of the MOSFETs to the deadtimes. However, this method is still not suitable for a wide range input voltage. Because the auxiliary voltage and the voltage signal from the auxiliary winding of the transformer are added together to drive the MOSFETs, the driving signal has the risk of exceeding the maximum gate voltage rating of the MOSFETs when the input voltage has a wide range variation. This causes some difficulties for the design of auxiliary windings. Section II of this paper further explains this.

To solve the above mentioned challenges, this paper presents a new self-driven synchronous rectification scheme which is suitable for topologies with symmetrically driven transformer, such as Half-bridge, Push-pull and Phase-shifted Full-bridge. The signals from the transformer and the output inductor are combined together to keep the MOSFETs operating even during

deadtimes, while at the same time, are able to turn off the MOSFETs properly by using auxiliary switches. (After the acceptance of this paper for PESC06, similar research results [7] from another university appeared in APEC06.) In addition to the description of the basic idea of utilizing the output inductor, this paper also put efforts on analysis and experimental verification for wide input range application. Both the positive and negative effects of the leakage inductance are described. A remarkable advantage is that this method allows a wide range variation of the input voltage.

II. DETAILED ANALYSIS OF THE EXISTING CHALLENGES FOR WIDE RANGE APPLICATION

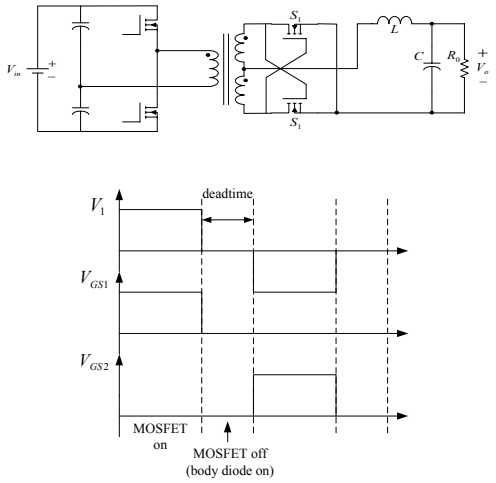


Fig.1 Basic self-driven SR for half –bridge

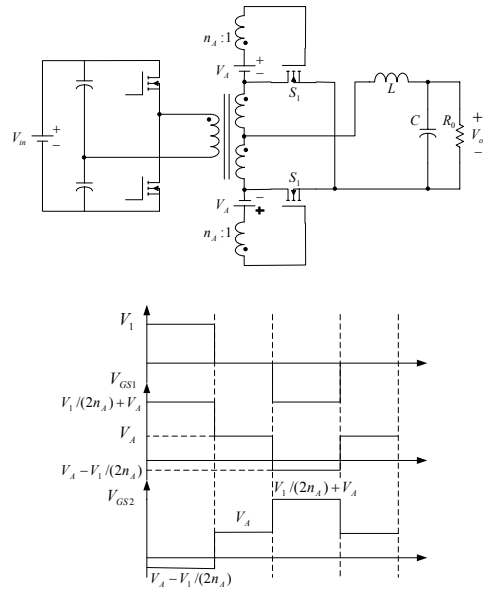


Fig. 2 An improved self-driven SR from [5]

As introduced from Section I, existing self-driven SR methods for topologies with symmetrically driven transformers still have some problems for the wide range input voltage application. Further explanation of these difficulties is now presented.

Figure 1 shows a diagram of a basic idea of self-driven SR for Half-bridge topology. In this approach, the body diodes of MOSFETs are on during the deadtimes when the driving signals are not available. When the converter operates with a wide range input, the duty ratio has a big variation, and the purpose of achieving a short deadtime is hard to realize. Thus, the conduction of the body diodes can cause significant power loss.

Figure 2 shows an improved self-driven SR which is suitable for symmetrically driven transformer [5]. An auxiliary supply V_A is utilized to compensate for the deadtime, and thus the MOSFETs operate during all the conduction period. Fig.2 also shows the waveforms of the transformer and driving signals. Suppose the turns ratio between the primary winding and auxiliary winding is $n_A:1$. Then the Gate-Source voltages of the SR are $V_{in}/(2n_A)+V_A$ and $V_A-V_{in}/(2n_A)$ when the primary switches are on, and V_A when the primary switches are off. In this case, $V_{in}/(2n_A)+V_A$ should not exceed the maximum Gate-Source voltage rating of the MOSFETs, while $V_A-V_{in}/(2n_A)$ should be zero or negative. Therefore, V_A should be smaller or equal to $V_{in}/(2n_A)$ in order to turn off the MOSFETs.

Another potential problem is the turn off of the SRs. Since the real signal from the power transformer still has a slope for turn-on and turn-off, it takes time to decrease the gate voltage to zero. Therefore, to turn off the SRs in time and avoid over-current, it is even better to design V_A to be much smaller than $V_{in}/(2n_A)$. Then, the gate voltage can quickly reach zero when needed. This also adds more pressure for wide range design.

The following design example can explain the problem when the input voltage has a wide range variation. For example, a telecommunication DC/DC converter with 36-75V input and 2.5V output (using half-bridge topology) has optimized power transformer design to be 5 turns for the primary winding and 1 turn for the secondary winding. Most suitable MOSFETs for the SR of this converter have a 2-4V gate threshold and a 20V maximum gate voltage rating. In order to effectively drive the MOSFET and guarantee the low on-resistance of the MOSFET, V_A should be 5V or higher. Since the primary winding has 5 turns, $n_A:1$ should be 2.5:1 to meet the requirement of $V_A \le V_{in}/(2n_A)$. When the input is 75V, $V_{in}/(2n_A)+V_A$ is 20V or higher. Considering the voltage spike caused by leakage and parasitic inductances, the driving voltage can easily exceed the gate-source voltage rating of the MOSFET. On the other hand, changing the transformer turns ratio or utilizing different MOSFETs with higher gate voltage rating will probably deteriorate the performance and lower power efficiency of the converter. For example, MOSFETs with 30V gate voltage rating typically have higher R_{DSON} than MOSFETs with 20V gate rating.

III. PROPOSED SELF-DRIVEN SYNCHRONOUS RECTIFIER SUITABLE FOR WIDE RANGE INPUT APPLICATION

According to the above analysis, existing self-driven synchronous rectification methods remain unsuitable for wide range application when the transformer is symmetrically driven. To deal with this problem, this paper proposes an alternative self-driven synchronous rectification scheme that is capable of driving the MOSFETs, even when the input voltage has wide range variation. By combining the signals from the secondary transformer and output filter inductor, the MOSFETs are driven during all their conduction period. Also, since the two kinds of signals are applied complementarily, the risk of exceeding the maximum gate voltage rating is greatly reduced.

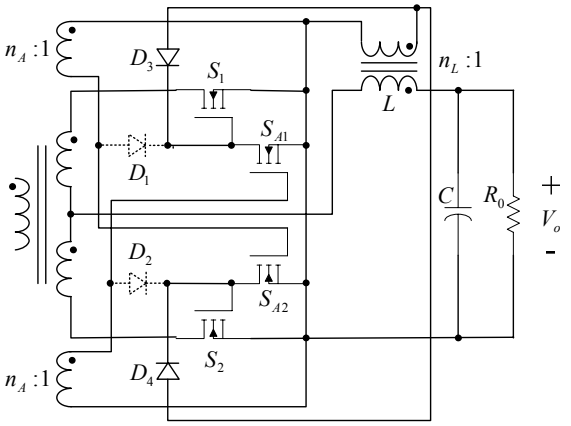
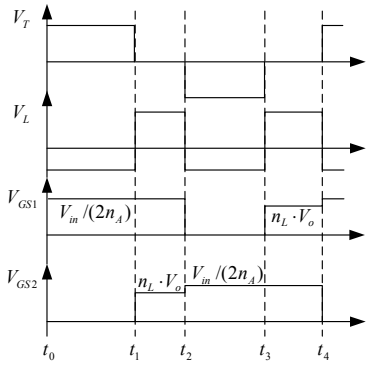
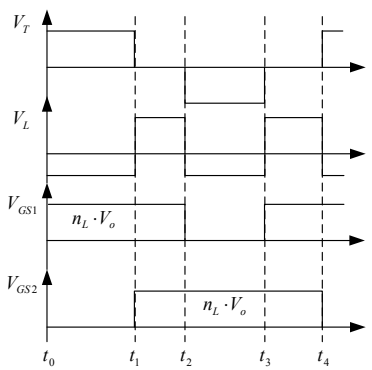


Fig.3 Proposed synchronous rectification method



(a) Timing when $V_{in}/(2n_A) \geq V_o \cdot n_L$



(b) Timing when $V_{in}/(2n_A) < V_o \cdot n_L$

Fig.4 Driving signal timing when the proposed method is applied

Fig.3 shows the proposed synchronous rectification method that obtains the driving signal directly from the secondary side. S_1 and S_2 are the MOSFETs used as synchronous rectifiers. S_{A1} and S_{A2} are the auxiliary switches used to discharge the gate of the MOSFET synchronous rectifier. D_1 and D_2 provide the channel for the auxiliary winding of the transformer to charge the gate of the MOSFETs, while D_3 and D_4 provide the channel for the auxiliary winding of the inductor. D_1 and D_2 are utilized due to practical considerations, since the inductor may be unable to provide enough current during light load or start-up time. S_{A1}, S_{A2} and D_1-D_4 are low power rating switches with small packages. (For example, S_{A1}, S_{A2} can use small MOSFETs with SOT-23 package. D_1 and D_3 can share a diode pair with SOT-23 package. The same is true for D_2 and D_4.)

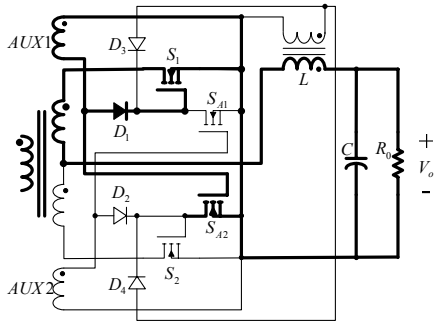
As analyzed above, adding the signal from the transformer with an auxiliary regulated voltage (shown in Fig.2) is not suitable for wide range application because the driving signal has the risk of exceeding the maximum gate voltage rating of the MOSFETs when the input voltage is high. Also, the regulated voltage cannot be high, which reduces the driving voltage during the deadtimes and thus increases the on resistance of the MOSFET. The proposed method utilizes the transformer and the inductor signals separately, while not adding them together. In other words, the signals from the transformer and the inductor are used to drive the MOSFETs at different periods of the duty cycle. This reduces the risk of exceeding the gate voltage rating while maintaining the high driving voltage during dead times. Fig.4 shows the driving signal timing of the proposed method when $V_{in}/(2n_A) \geq V_o \cdot n_L$ and $V_{in}/(2n_A) < V_o \cdot n_L$.

From Fig.3 and Fig.4, the new method operates based on two concepts: Firstly, gate charge and retention of the main MOSFETs are realized by the auxiliary diodes. The auxiliary switches can discharge the retained gate voltage of the main MOSFETs when needed. For Forward converters, this concept has been proposed in reference [6]. Secondly, the gate voltages of the main MOSFETs are rebuilt after the off period (period $t_2 - t_3$ for S_1) by the signal from the inductor during the deadtime for the transformer (period $t_3 - t_4$ for S_1).

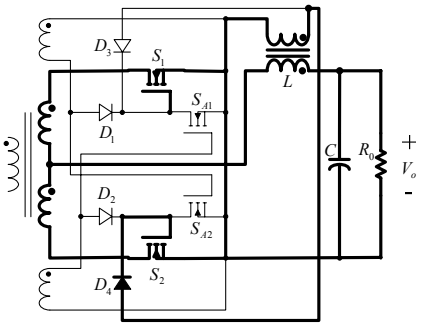
Fig.4 (a) and Fig.4 (b) show the driving signal timings of the proposed method when $V_{in}/(2n_A) \geq V_o \cdot n_L$ and $V_{in}/(2n_A) < V_o \cdot n_L$. Since principles of these two cases are similar, we just explain the condition when $V_{in}/(2n_A) \geq V_o \cdot n_L$. Fig.5 shows the condition of each operation period during the entire duty cycle. The detailed description is provided as following:

Mode 1 ($t_0 - t_1$): During this period, the gate of S_1 can receive a positive voltage from AUX1 of the transformer. D_1 is on and the auxiliary winding charges the gate of S_1. The auxiliary switch S_{A1} is off, and thus keeps S_1 on. The main current, which charges the output capacitor and

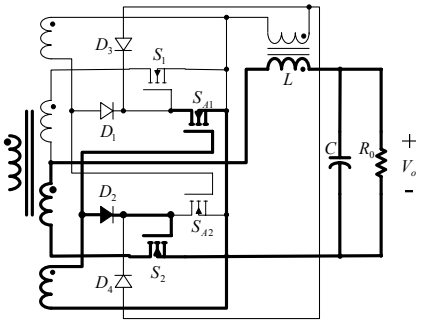
supplies the load, goes through S_1 and the output inductor. Also, the auxiliary diode D_3 and D_4 are reverse biased and the voltage of the inductor is blocked. At the same time, S_{A2} is turned on by AUX1 and discharges the gate of S_2. Therefore, S_2 is turned off.



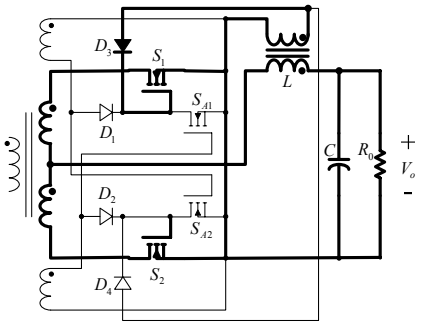
(a) The condition of the circuit during $t_0 - t_1$



(b) The condition of the circuit during $t_1 - t_2$



(c) The condition of the circuit during $t_2 - t_3$



(d) The condition of the circuit during $t_3 - t_4$

Fig.5 Detailed description of the proposed synchronous rectification scheme

Mode 2 ($t_1 - t_2$): During this period, the power transformer has no output, and the voltage on the auxiliary winding drops to zero. S_{A1} and S_{A2} get no driving signal and remain off. D_1 is reverse biased and the gate voltage of S_1 is retained. Because we are discussing the case when $V_{in}/(2n_A) \geq V_o \cdot n_L$, D_3 is reverse biased, and the gate voltage is still $V_{in}/(2n_A) - V_F$. (V_F is the forward conduction voltage of the diode.) At the same time, the auxiliary winding of the inductor charges the gate of S_2 through D_4. Therefore, S_1 and S_2 conduct in parallel to provide the channel for the free-wheeling current.

Mode 3 ($t_2 - t_3$): During this period, D_1 and D_3 are reverse biased since the voltages from the auxiliary winding of the transformer and the inductor are negative. In this case, S_1 must be turned off to avoid reverse current. AUX2 provides a positive voltage that turns on the auxiliary switch S_{A1} immediately. Thus, the retained gate voltage of S_1 is discharged, and S_1 is quickly turned off. Also, AUX2 turns S_2 on through D_2. The main current goes through S_2.

Mode 4 ($t_3 - t_4$): The expected result of this period is to turn on S_1 and S_2 at the same time. S_2 is kept on since the gate voltage is retained. D_2 and D_4 are therefore reverse biased. Since the output voltage of the transformer has already dropped to zero, the signal from the inductor becomes important to turn on S_1. In this case, S_{A1} gets no driving signal and is turned off. The auxiliary winding of the output inductor charges the gate of S_1 through D_3. Therefore, S_1 is turned on and conducts in parallel with S_2.

Based on the above analysis, the proposed synchronous rectification method is able to turn on and turn off the MOSFETs properly. The MOSFETs keep conducting even during the deadtimes and, thus, greatly reduce the power loss.

IV. EXPERIMENTAL RESULTS

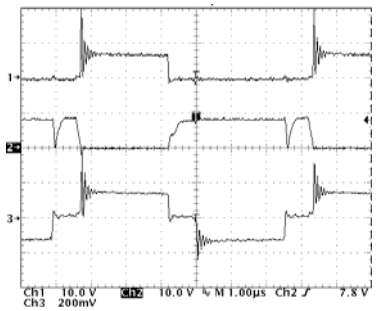
To verify the principle and wide range operation of the proposed scheme, a prototype is built by using conventional Half-bridge topology switched at 150kHz hard switched. The specification is:

- Vin: 36-75V
- Vo: 2.5V
- Io: 30A

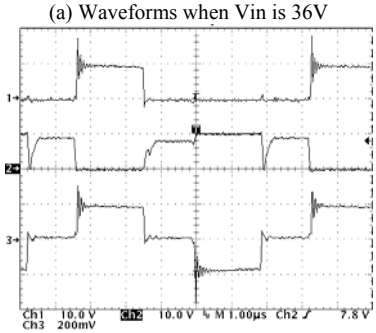
IRF7495 (100V, 22mΩ, SO-8) is used for the primary switches. Each synchronous rectifier (S_1 and S_2) uses three STS25NH3LL (SO-8) in parallel. STS25NH3LL has an on-resistance of 3.2mΩ. E18 magnetic core is used for both the power transformer and output inductor. The cross area of the magnetic core is 39.5mm^2. The power transformer has 5 turns for the primary winding and 1 turn for the secondary winding.

It should be emphasized that a certain amount of leakage inductance of the transformer is vital to avoid short period over current in some cases. Since the turn-off signals of the SRs are from the transformer, they still need a short time to rise and trigger the auxiliary switches. During that period, two SRs are on at the same time when the output of the transformer is not zero. The existence of the leakage inductance can prevent the current from reaching a very high value before one of the SRs is turned off.

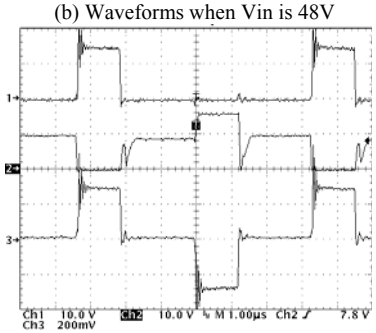
Therefore, the following analysis and experimental results are based on the condition when the transformer is not tightly coupled.



(a) Waveforms when Vin is 36V



(b) Waveforms when Vin is 48V



(c) Waveforms when Vin is 75V

Fig.6 Waveforms of Vds (Channel 1), Vgs (Channel 2) of the SR (S1) and the voltage of the secondary winding (Channel 3)

Fig.6 shows the waveforms of the SR (S_1) and the secondary winding. Channel 1 and Channel 2 show the drain-source and gate-source driving voltage of S_1. Channel 3 represents the output voltage of the transformer. It can be clearly seen that the driving signal is extended to the dead times. The waveforms are obtained when the transformer is not so tightly coupled. The scheme can still operate well in this case. From the figure, a short time gate voltage discharging, which is actually caused by the disturbance of the driving winding due to coupling problem, is shown. Fig.7 shows the details during that period. Channel 1 and Channel 2 represent the gate voltage of S_1 and S_2. Channel 3 shows the signal from the auxiliary driving winding. The voltage spike from the driving winding turns on one of the auxiliary switches (S_{A1} or S_{A2}), and thus discharge the gate voltage for a short time. The signal from the output inductor can solve this problem and quickly charge the gate of SR again. As can be seen, even during the short period, at least one of the SRs obtains a driving voltage and keeps the MOSFET on. Therefore, the power loss during that short period is very small. (10V/div in Y-axis for all these waveforms)

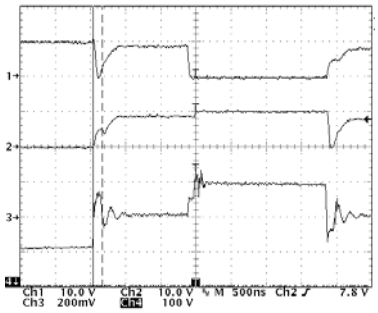


Fig.7 V_{gs1}, V_{gs2} and voltage of a driving winding when Vin is 48V

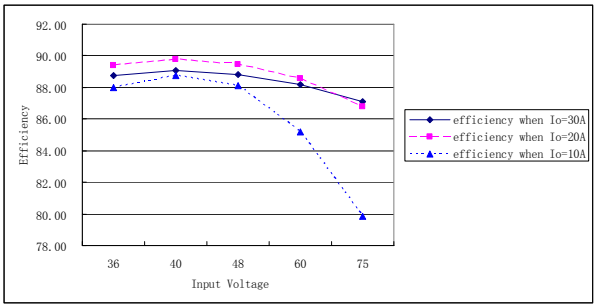


Fig.8 Efficiency of the built prototype

By applying the proposed self-driven scheme to the conventional half-bridge, an efficiency of 89% at 48V input and 2.5V-30A output is obtained. Fig.8 shows the efficiency curves under different load conditions. The experimental results verify the principle and performance of the scheme.

V. CONCLUSION

This paper presents a new self-driven synchronous rectification scheme which is suitable for the wide range input application of some very popular topologies, such as Half-bridge, Push Pull and Phase-shifted Full-bridge. The signal from the transformer and the output inductor are properly combined together to drive the MOSFETs. The principle of the proposed method is analyzed and experimental results are presented. Once again, we remark that after this paper was accepted, close to identical results appeared in [7]. The results were obtained independently and concurrently. Similar results in [7] were obtained independently and concurrently.

Reference

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