Current-Fed Dual-Bridge DC–DC Converter

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***Abstract*—A new isolated current-fed pulsewidth modulation dc–dc converter—current-fed dual-bridge dc–dc converter—with small inductance and no deadtime operation is presented and analyzed. The new topology has more than 3× smaller inductance than that of current-fed full-bridge converter, thus having faster transient response speed. Other characteristics include simple self-driven synchronous rectification, simple housekeeping power supply, and smaller output filter capacitance. Detailed analysis shows the proposed converter can have either lower voltage stress on all primary side power switches or soft switching properties when different driving schemes are applied. A 48-V/125-W prototype dc–dc converter with dual output has been tested for the verification of the principles. Both simulations and experiments verify the feasibility and advantages of the new topology.**

***Index Terms*—Current-fed, dc–dc converter, deadtime, dual-bridge, full-bridge, zero voltage switching (ZVS).**

I. Introduction

CURRENT-FED dc–dc converters have recently seen resurgence in applications [1]–[12]. In general, the term "current-fed" in an isolated dc–dc converter refers to the fact that the filter inductor of the converter is on the primary side. The voltage and current of the primary winding of the transformer are determined by the load voltage and the source impedance (the inductance of the inductor). Noticeable advantages of current-fed topologies include immunity from transformer flux-imbalance and no output inductor (which makes them a prime candidate for multi-output applications). Some typical examples of isolated current-fed dc–dc converter topologies include current-fed full-bridge [1]–[5], current-fed push–pull [6]–[9], and their derivations [10]–[12].

In this paper, a new isolated current-fed pulsewidth modulation (PWM) dc–dc converter is presented (shown in Fig. 1). The topology alternates between two stages of operation. In Stage I, it operates similar to a current-fed full-bridge converter at the operation stage that the power transmits through the transformer to the output. In Stage II, it behaves similar to a current-fed half-bridge converter. However, Stage I differs from the current-fed full-bridge because the inductor stores energy as the transformer transmits energy from the dc source to the load. When operating in the current-fed half-bridge-like stage, the inductor releases and sends the stored energy, together with the energy from the dc source, to the load. The input-to-output voltage transfer ratio of the new topology is the same as in the voltage-fed topology of [13]. As long as the inductor is in continuous conduction mode (CCM), the energy from the input dc source to the load is continuous in the whole operating period, thus achieving no deadtime[1] operation. Because of the no deadtime operation, the proposed topology has many significant advantages.

- Approximately 3.5× less inductance than that of the current-fed full-bridge dc–dc converter, which means 3.5× faster transient response speed than current-fed full-bridge converter with same design specifications;
- Simple self-driven synchronous rectification and housekeeping power supply because of no dead-time operation and approximately 50% duty ratio that creates a constant voltage across the secondary winding of the transformer;
- An input-output voltage transfer ratio that is linear with duty ratio (buck-like). This is different from other current-fed topologies, which have boost or buck-boost transfer characteristics and right half plane (RHP) zero when operating in CCM [1]–[12];
- Substantially smaller output filter capacitance compared with typical current-fed topologies and significantly reduced output current ripple in contrast to other current-fed topologies [1]–[10]. This is because the energy transfer is continuous and the load current is not retained solely by the output capacitors during the whole operating period. (The effect of the commutation of the rectification diodes is not considered here);
- With the different driving signal timing methods, the converter could have low voltage stress on all primary side power switches that is not greater than the maximum input voltage. Alternatively, a second driving method has soft switching on power switches. In this case, the voltage spikes on two of the power switches may be up to twice the maximum input voltage.

In addition, the proposed topology maintains the advantages of general current-fed topologies such as requiring only one inductor for multi-output applications and does not have the startup issue that generally occurs in current-fed topologies as in [1] and [10]. To honor the advantages of the proposed topology, the input voltage range should be limited within 2:1 for no deadtime operation. For wider input voltage range, the operation with deadtime will be engaged but the inductor will still be smaller than other current-fed topologies. Compared to a current-fed full-bridge converter, one more power switch (implemented by two MOSFETs in series to configure a bi-directional switch) is used. The two capacitors of the half-bridge configuration in the presented topology are not a real burden because they can use

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[1]by deadtime we mean the time duration in an operating period that is essentially needed to obtain a regulated output voltage. During the deadtime, the energy transmission from input dc source to output load is not continuous.

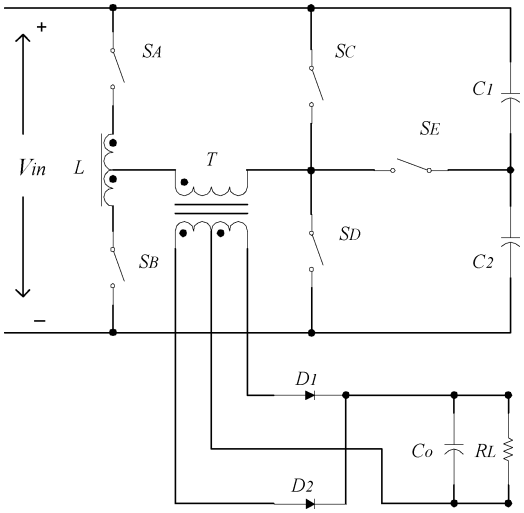


Fig. 1. Proposed isolated current-fed dc–dc converter with center-tapped inductor.

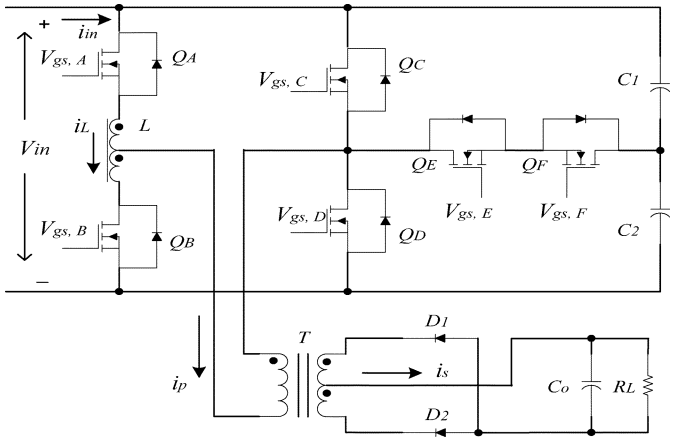


Fig. 2. Implementation of proposed isolated current-fed dc–dc converter with center-tapped inductor.

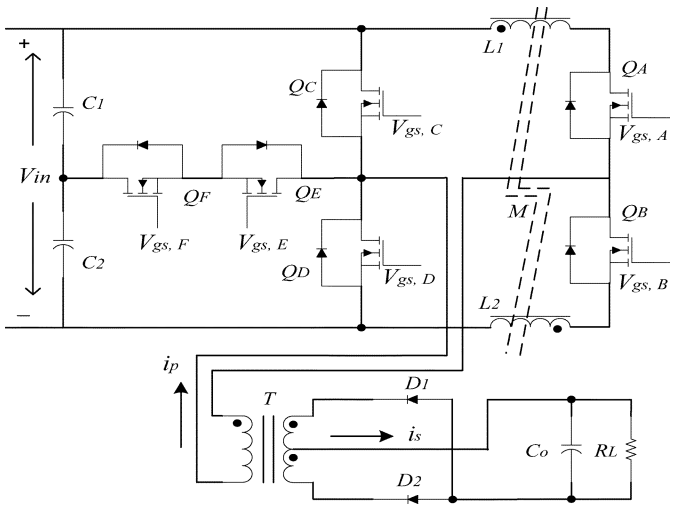


Fig. 3. Implementation of proposed isolated current-fed dc–dc converter with two coupled inductors.

the capacitors usually placed at the input end of the dc–dc converter as an input filter.

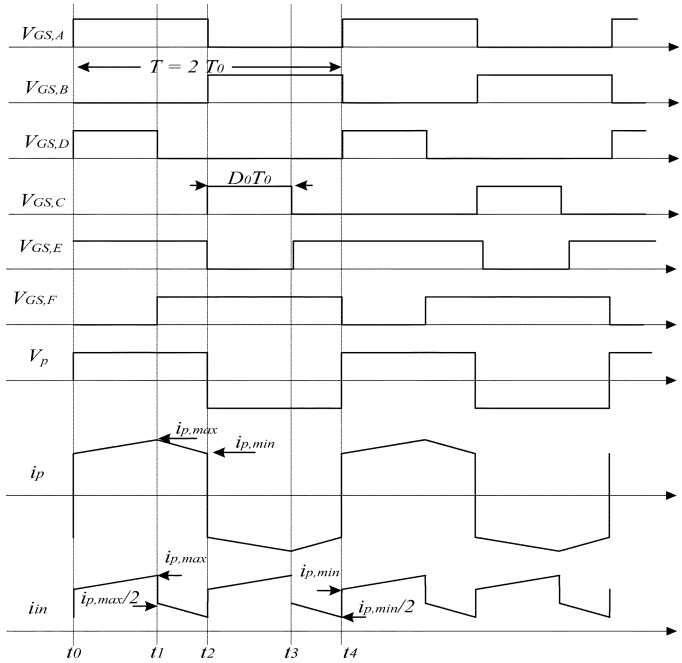


Fig. 4. Idealized waveforms of the proposed isolated current-fed dc–dc converter.

Section II introduces the principle and operation of the proposed topology. The analysis and comparison of the new topology with the current-fed full-bridge converter are given in Section III. Section IV discusses low rating voltage requirement of the power switches and soft switching characteristics under different timing of driving signal sequences. Section V gives the experimental results based on the prototype dc–dc converter with 48-V input and dual outputs of 5 V/20 A and 12.5 V/2 A. Section VI concludes the paper.

II. Principle and Operation of the Proposed Topology

Fig. 1 is the principle schematic of the proposed topology. Switches S_A, S_B, S_C, S_D, center-tapped inductor L and transformer T comprise a current-fed full-bridge; switches S_A, S_B, center-tapped inductor L and transformer T, along with two capacitors C_1 and C_2 comprise a current-fed half-bridge. C_1 and C_2 are connected to the transformer T by switch S_E. As a reference a current-fed full-bridge converter is illustrated in Fig. 6.

Fig. 2 is its implementation circuit. The inductor L is center-tapped with its dotted end shown as in the figure. The rectification diodes D_1 and D_2 can be replaced by MOSFETs as self-driven or control-driven synchronous rectifiers for low voltage high current applications to improve the efficiency. Fig. 3 is the implementation of the proposed topology in another form, in which two coupled inductors are used. Switch S_E in Fig. 1 is a bidirectional switch. It is realized in Figs. 2 and 3 by two MOSFETs Q_E and Q_F in series connection. In the following the operation of the circuits will be described for the circuit illustrated in Fig. 2.

Switches Q_A and Q_B in Fig. 2 are controlled with complementary 50% square waves so that the conduction time of the two switches slightly overlaps. The purpose of simultaneous conduction is to prevent the occurrence of the open circuit state across the inductor L. Otherwise, very high voltage spikes

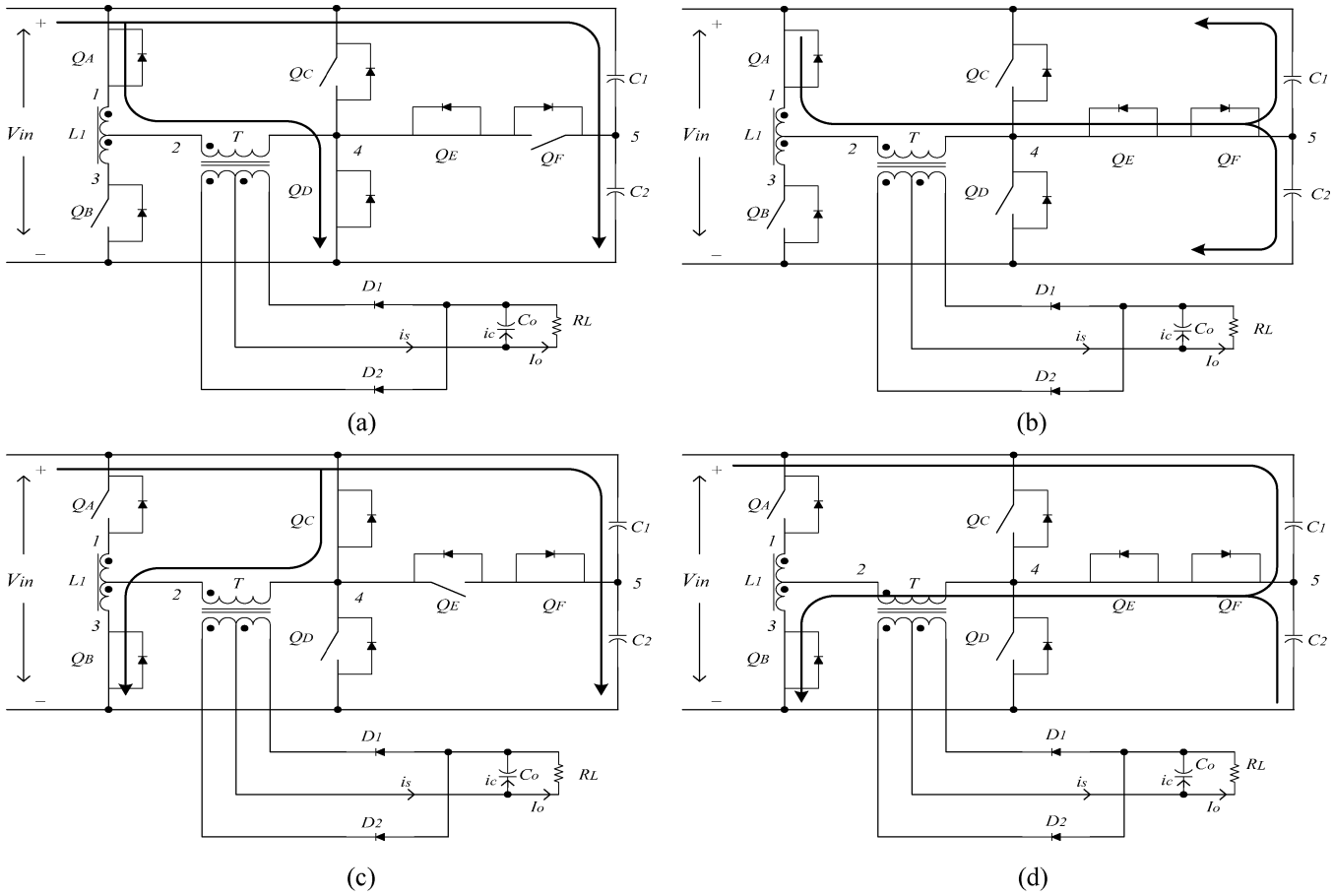


Fig. 5. Operating description of the proposed topology: (a) stage I; (b) stage II; (c) stage III; and (d) stage IV.

would occur across the switches, which may cause the switches to fail.

For simplicity the description below is based on the assumptions that the inductor L operates in continuous conduction mode; all switches are assumed ideal; the leakage inductance of the transformer is neglected. The major ideal waveforms for the circuit in steady state are shown in Fig. 4. The primary winding to secondary windings turn ratio of the transformer is n. The voltage across the primary winding is $V_p = nV_o$, where V_o is the output voltage of the converter. The input dc voltage is V_{in}. The load current is I_o. Circuit operation of each switch state is given referring to Fig. 5.

Stage I: $t_0 - t_1$ Time Interval: The state of each switch from t_0 to t_1 and the current flow are given in Fig. 5(a). Q_A, Q_D and Q_E are on; Q_B, Q_C and Q_F are off. The operation of this stage is similar to the current-fed full-bridge at the operation of transferring the energy through the transformer to the output. The difference is that during this period of time, the inductor of current-fed full-bridge converter releases energy, whereas the inductor of the dual-bridge current-fed converter stores energy.

For Stage I, the following holds:

voltage of node 1, $V_1 = V_{\text{in}}$;
voltage of node 2, $V_2 = nV_o$;
voltage of node 4, $V_4 = 0$;
voltage across nodes 1 and 2, $V_{1,2} = V_{2,3} = V_{\text{in}} - nV_o$.

The voltages across the switches:

$V_{DS,B} = V_2 - V_{2,3} = 2nV_o - V_{\text{in}}$;
$V_{DS,A} = V_{DS,D} = V_{DS,E} = 0$;
$V_{DS,C} = V_{\text{in}}$;
$V_{DS,F} = V_{\text{in}}/2$.

In this period, the input current going through the inductor L and the primary winding of the transformer linearly increases with time.

Assuming the output voltage is constant on a cycle-by-cycle basis (steady state), this leads to

$$V_{\text{in}} - nV_0 = L\frac{i_{p,\max} - i_{p,\min}}{D_0 T_0}. \tag{1}$$

One part of the energy from input transmits to the output load through the transformer; the other part is stored in the inductor L. The current i_s through the secondary winding of the transformer begins to increase from time t_0, and the discharging current i_c of C_o decreases. After $i_s = I_o$, i_s charges C_o and provides all load current I_o.

At t_1, Q_D is off and Q_F turns on. The voltage across the inductor reverses polarity to maintain the continuity of the current and the magnetic flux through the inductor. Then next stage of the operation begins.

Stage II: $t_1 - t_2$ Time Interval: Fig. 5(b) shows the state of switches and the current path at this stage. Switches Q_A, Q_E and Q_F are on, while Q_B, Q_C and Q_D are off. The operation of this stage is similar to the current-fed half-bridge topology, the inductor releases and sends the energy through the transformer to the output.

At this stage, both the inductor and the input power source provide the energy to the output load. With the release of the energy stored in the inductor, the current through the inductor and the primary winding of the transformer continuously decrease. Beginning from t_1, the input current drops to and decreases from half of $I_{p,max}$. The other half of the current through the primary winding is supplied by the discharging current of C_1. We have:

$V_1 = V_{\text{in}}$;
$V_2 = nV_o + V_{\text{in}}/2$;
$V_4 = V_{\text{in}}/2; V_{1,2} = V_{2,3} = V_{\text{in}} - (nV_o + V_{\text{in}}/2) = -(nV_o - V_{\text{in}}/2)$.

The voltages across the switches:

$V_{DS,A} = V_{DS,E} = V_{DS,F} = 0$;
$V_{DS,B} = V_2 - V_{2,3} = (nV_o + V_{\text{in}}/2) + (nV_o - V_{\text{in}}/2) = 2nV_o$;
$V_{DS,C} = V_{DS,D} = V_{\text{in}}/2$.

In this stage, the following relation holds:

$$-\left(nV_0 - \frac{1}{2}V_{\text{in}}\right) = L\frac{i_{p,\min} - i_{p,\max}}{(1-D_0)T_0}. \tag{2}$$

C_1 discharges and C_2 charges during Stage II. At t_2^+, switches Q_A and Q_E turn off, Q_B and Q_C turn on, and the operation enters the next stage.

In both full-bridge-like Stage I during which the inductor stores the energy and the half-bridge-like Stage II during which the inductor releases the energy, the energy continuously transmits from the input to the output all the time.

Stage III: $t_2 - t_3$ Time Interval: The state of each switch from t_2 to t_3 and the current flow of the circuit are given in Fig. 5(c), where Q_A, Q_D and Q_E are off; Q_B, Q_C and Q_F are on. The operation is symmetric to Stage I but the current i_p through the primary winding reverses the direction. The voltages across the switches are

$V_{DS,A} = V_{\text{in}} - V_1 = 2nV_o - V_{\text{in}}$;
$V_{DS,B} = V_{DS,C} = V_{DS,F} = 0; V_{DS,D} = V_{\text{in}}; V_{DS,E} = V_{\text{in}}/2$.

Stage IV: $t_3 - t_4$ Time Interval: At this stage (see Fig. 5(d)), beginning from t_3, switches Q_B, Q_E and Q_F are on. Q_A, Q_C and Q_D are off. i_p decreases from $i_{p,max}$ linearly to $i_{p,min}$ at $t = t_4$. The operation is symmetric to Stage II but with reversed primary winding current. Opposite to Stage II, C_1 charges and C_2 discharges. This ensures the balance of charges in C_1 and C_2 in a complete operation circle from Stage I to Stage IV.

The voltages across the switches are $V_{DS,A} = V_{\text{in}} - V_1 = 2nV_o$; $V_{DS,B} = V_{DS,E} = V_{DS,F} = 0$; $V_{DS,C} = V_{DS,D} = V_{\text{in}}/2$.

Afterwards, the operation goes back and repeats from the first stage. From the above description, it can be seen that the maximum input voltage $V_{\text{in,max}}$ is limited by $V_{DS,B}$ (at Stage I) = $V_{DS,A}$ (at Stage III)$= 2V_p - V_{\text{in}} \geq 0$. That is, $V_{\text{in,max}} \leq 2V_p = 2nV_o$. Obviously, $V_{\text{in,min}} = V_p = nV_o$. Thus, for operation with no deadtime as described above, the input voltage variation must be limited in 2:1.

However, with other control considerations, the input voltage range can be widened more than 2:1 by introducing a deadtime. For example, the converter may operate in no deadtime mode + current-fed half-bridge mode with deadtime. At low voltage the converter operates with no deadtime as illustrated above. When the input voltage is greater than 2× minimum input voltage, the converter operates as conventional current-fed half-bridge converter that consists of switches Q_A, Q_B, capacitors C_1, C_2, inductor L and transformer T. In this case, switches Q_C and Q_D are off, switches Q_E and Q_F are on in the whole period of the operation, switches Q_A and Q_B are controlled by two 180° out of phase signals with duty ratio greater than 0.5. In this paper, the discussion to the proposed converter is limited only to no deadtime CCM mode with input voltage within 2:1 range.

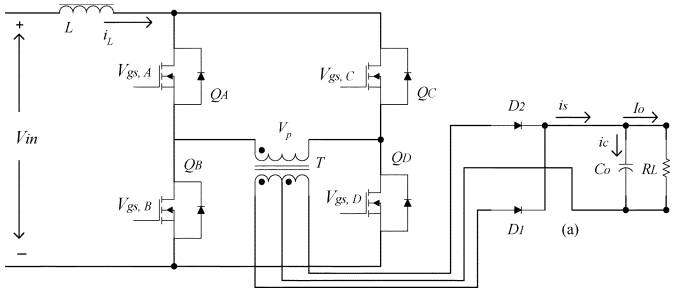


Fig. 6. Current-fed full-bridge dc–dc converter.

The voltage and current of the primary winding of the proposed topology are determined by the load voltage and the inductance of inductor L. The voltage across the secondary winding is consequently constant (depends on output load voltage). This makes a housekeeping supply with constant voltage easily obtained, and self-driven synchronous rectifier at secondary side can be used to improve the efficiency for high current applications. The driving voltage of the self-driven synchronous rectifier at secondary side can also be easily optimally designed to decrease the driving loss of the MOSFETs.

Combining (1) and (2) leads to the input-to-output voltage transfer characteristic

$$V_0 = \frac{V_{\text{in}}}{n}\frac{1+D_0}{2} \tag{3}$$

which is buck-like and is linear to D_0. It can be seen that there is no RHP zero in the voltage transfer function. Therefore, the limit caused by the RHP zero to the dynamic performance in conventional current-fed converters [14] does not exist in current-fed dual-bridge converter.

III. Analysis of the Proposed Topology and its Comparison to Current-Fed Full-Bridge Converter

The conventional current-fed full-bridge converter is shown in Fig. 6. Fig. 7 shows the idealized major waveforms of the current-fed full-bridge converter in CCM. The relations of the input inductance to current ripple of the inductor and the output filter capacitance to the output voltage ripple for both converters are analyzed in this section.

For both converters, input voltage is $V_{\text{in}}(V_{\text{in,max}} : V_{\text{in,min}} = 2:1)$; output voltage is V_o; output load is R_L; output power is P_o; output capacitance is C_o; the complete operation period is T (see Figs. 4 and 7); $T_0 = T/2$; ripple current (peak-to-peak) of the input inductor L is $\Delta i_{L,pp}$; output ripple voltage (peak-to-peak) is $\Delta V_{o,pp}$; critical inductance L_c is defined as the minimum inductance to keep the inductor current continuous at the 10% rating output power; D_0T_0 is the time that the current through the inductor increases. For the new topology (parameters denoted by overhead ∼), the turns ratio of primary winding

TABLE I
COMPARISON OF PROPOSED TOPOLOGY AND CURRENT-FED FULL-BRIDGE DC–DC CONVERTER

Proposed Current-Fed DC-DC Converter (CCM)	Current-Fed Full-Bridge DC-DC Converter (CCM)
$\tilde{V}_o = \frac{V_{in}}{n}\frac{1+D_0}{2}$	$V_{o,F} = \frac{V_{in}}{2n}\frac{1}{1-D_0}$
$\Delta\tilde{i}_{L,pp,\max} = \Delta\tilde{i}_{L,pp}\big\|_{D_0=\sqrt{2}-1} = 0.172\frac{nV_oT_0}{L}$	$\Delta i_{L,pp,F,\max} = \Delta i_{L,pp,F}\big\|_{D_0=1/2} = 0.5\frac{nV_oT_0}{L}$
$\Delta\tilde{V}_{o,pp} = \frac{n^2V_oT_0^2}{8LC_o}\frac{D_0(1-D_0)}{1+D_0}$	$\Delta V_{o,pp,F} = \frac{V_o}{R_LC_o}D_0T_0$
$\tilde{L}_{c,\max} = \tilde{L}_c\big\|_{D_0=\sqrt{2}-1} = 0.0858\frac{n^2V_o^2T_0}{P_o}$	$L_{c,F,\max} = L_{c,F}\big\|_{D_0=1/3} = 0.296\frac{n^2V_o^2T_0}{P_o}$

~ denotes proposed topology; subscript F denotes full-bridge; V_{in} and V_o denote input and output voltage, respectively; $\Delta I_{L,pp}$ denotes peak-to-peak current ripple through inductor; $\Delta V_{o,pp}$ is peak-to-peak output voltage ripple; L_c is critical inductance to keep inductor current continuous at output power of P_o.

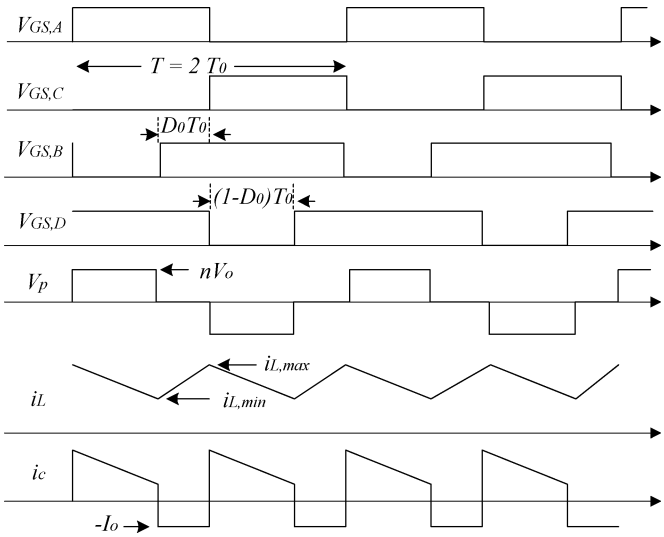


Fig. 7. Idealized waveforms of current-fed full-bridge dc–dc converter.

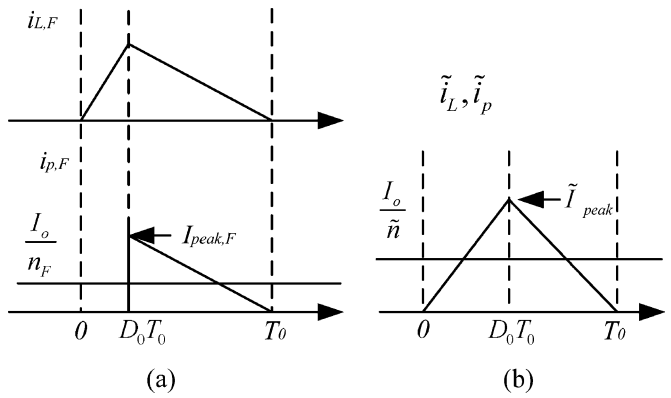


Fig. 8. Current waveforms of inductors and primary windings at critical CCM/DCM: (a) Current-fed full bridge where $i_{L,F}$ is current through inductor, i_p is current through primary winding, $I_{\mathrm{peak,F}}$ is maximum inductor current and (b) proposed converter where i_L and i_p are equal. In both cases, the load current is I_0.

to secondary winding is $\tilde{n} = n = N_p/N_s$; $\tilde{D}_0$ changes between 0 and 1. $\tilde{V}_o$ is its output voltage. For current-fed full-bridge converter (parameters denoted by subscript F), the turns ratio of primary winding to secondary winding is $n_F = N_p/N_s$. For $V_{\mathrm{in}} = V_{\mathrm{in,min}}$, $D_{0,F} = 0$; for $V_{\mathrm{in}} = V_{\mathrm{in,min}}$, $D_{0,F} = 0.5$. We have $n_F = 2n$ with $D_{0,F}$ changes between 0 and 0.5. $V_{o,F}$ is its output voltage. All components are ideal. For steady state operation, the equations in Table I hold.

From the equations in Table I, it can be seen that $V_{o,F}$ has a RHP zero. $\tilde{V}_o$ is linear to $\tilde{D}_0$. Further, the critical inductance required to maintain the inductor current in continuous conduction mode is different in the two topologies. Fig. 8 shows inductor currents and primary currents for both the current-fed full-bridge and the proposed converter in borderline CCM/DCM operation. In the conventional current-fed full-bridge converter, the primary winding current is zero for $0 < t \leq D_{0,F}T_0$, as illustrated in Fig. 8(a). On $D_{0,F}T_0 < t \leq T_0$, the primary winding current equals the inductor current. On the other hand, as Fig. 8(b) shows, the proposed converter always has the primary winding current equal to its inductor winding current. Thus, to keep an average output current of I_0 to the load, the current-fed full-bridge requires peak inductor current $I_{\mathrm{peak,F}} = 2I_o/[n_F(1 - D_{0,F})]$. On the other hand, the proposed converter requires peak inductor current $\tilde{I}_{\mathrm{peak}} = 2I_o/\tilde{n}$. Since $n_F = 2\tilde{n}$ and $D_{0,F}$ changes between 0 and 0.5, $I_{\mathrm{peak,F}} \leq \tilde{I}_{\mathrm{peak}}$. And the inductor of the current-fed full-bridge converter needs to store more energy than that of the proposed converter for the same output power. This results in larger inductance requirement for the current-fed full-bridge converter.

Fig. 9 shows the normalized critical inductance versus D_0. The maximum $\tilde{L}_c$ for the proposed topology occurs at $\tilde{D}_0 = 0.414$. For the current-fed full-bridge converter, the maximum $L_{c,F}$ occurs at $D_{0,F} = 0.333$. $L_{c,F,\max}/\tilde{L}_{c,\max} = 3.5$, which means when keeping the converters operating at CCM under the same minimum output current (or output power, usually, this power is 10% rating output power), the required inductance for current-fed full-bridge converter is 3.5× greater than the proposed converter. Correspondingly, its magnetic core size of the inductor is also much smaller than that of the current-fed full-bridge converter.

Fig. 10 presents normalized curves that show the relation of the peak-to-peak ripple current through the inductor to D_0. The actual range of D_0 for current-fed full-bridge converter is 0 ∼

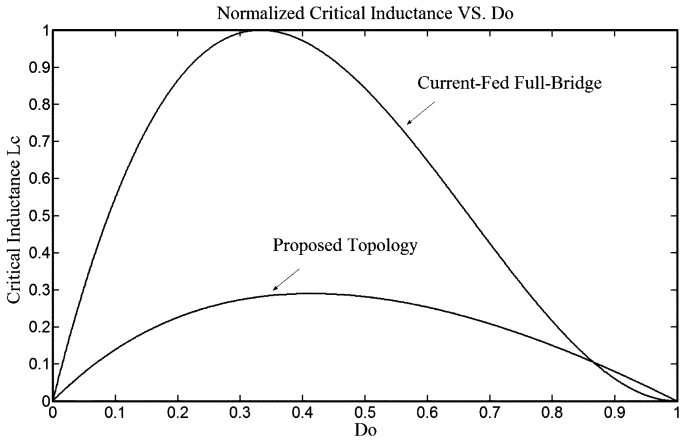


Fig. 9. Normalized critical inductance versus D_0.

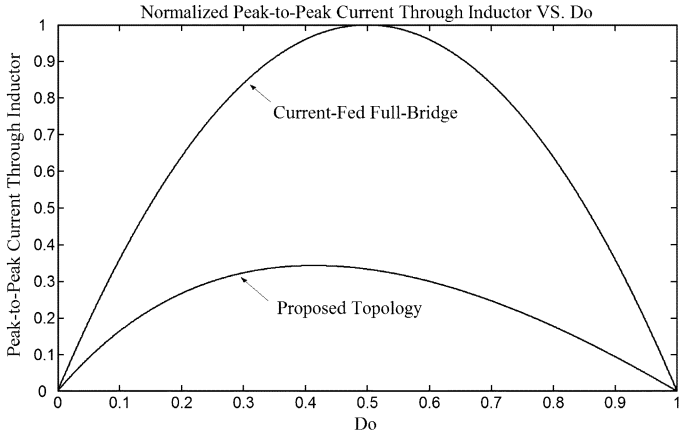


Fig. 10. Normalized peak-to-peak current through inductor versus D_0.

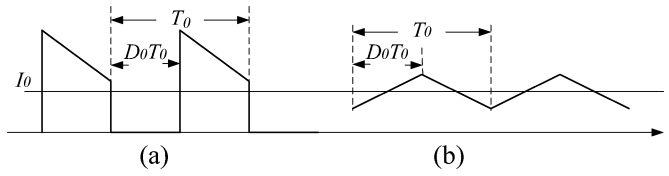


Fig. 11. Current waveforms at rectifiers output: (a) current-fed full-bridge and (b) proposed topology.

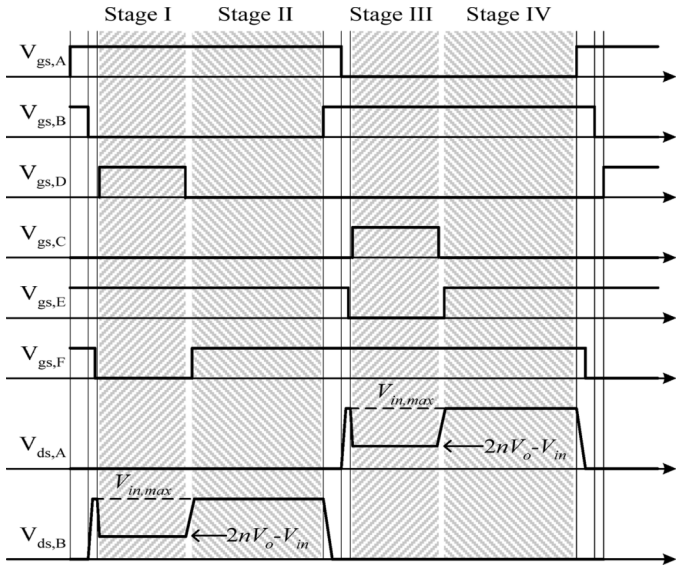


Fig. 12. Driving signals timing for lower voltage stress on power switches during transitions.

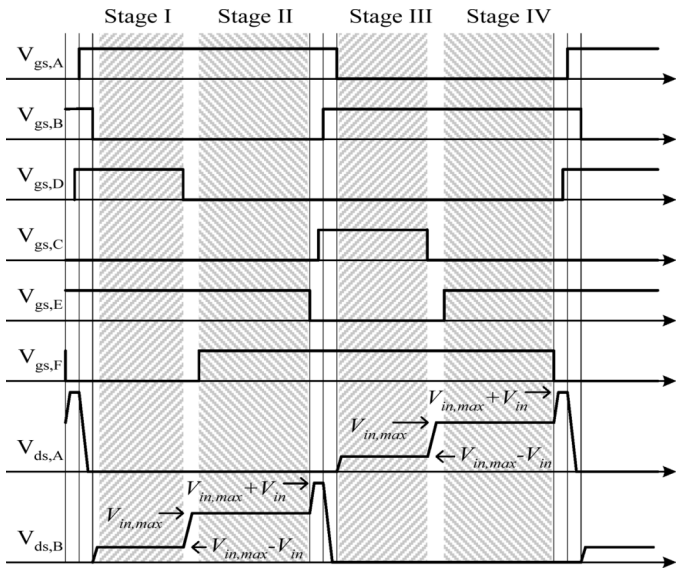


Fig. 13. Driving signals timing for ZVS switching.

0.5 in the case of 2:1 input voltage range while D_0 for the proposed topology is $0 \sim 1$. Obvious, if the two converters use the same value inductance, then the ripple current through the traditional current-fed full-bridge converter is approximately $3\times$ larger than that of the proposed topology.

Because of the existence of the deadtime D_0T_0 in conventional current-fed full-bridge converter, the load current is only maintained by the output capacitor during deadtime. Fig. 11 shows the current waveforms of rectifier outputs for both the current-fed full-bridge and the proposed converter. It can be seen that the peak current of current-fed full-bridge converter is greater. Further, during the time interval D_0T_0, only output capacitor C_0 provides energy to the load in the current-fed full-bridge converter. Comparatively, smaller capacitance is needed for the proposed converter if the same output voltage ripple is specified (see formula in Table I).

IV. Low Voltage on Power Switches and ZVS Switching Characteristics From Different Timing Considerations of Control Signals

From the description in Section II, the greatest voltage stresses of the power switches occurs on Q_A and Q_B at Stages II and IV, and equals the maximum input voltage. The voltage stresses of the power switches during switching transitions differ under different timing of driving signals on the gates of MOSFETs. As shown in Figs. 12 and 13, during the transition from Stage II to Stage III (from Stage IV to Stage I), the rising edge of $V_{GS,C}(V_{GS,D})$ may trail or lead the transition from $V_{GS,A}$ on to $V_{GS,B}$ on (from $V_{GS,B}$ on to $V_{GS,A}$ on) as in Fig. 12 (Fig. 13). Correspondingly, power switches may have voltage stresses as low as the maximum input voltage, or have zero voltage switching (ZVS) characteristics with higher voltage spikes on switches Q_A and Q_B. Designers can choose

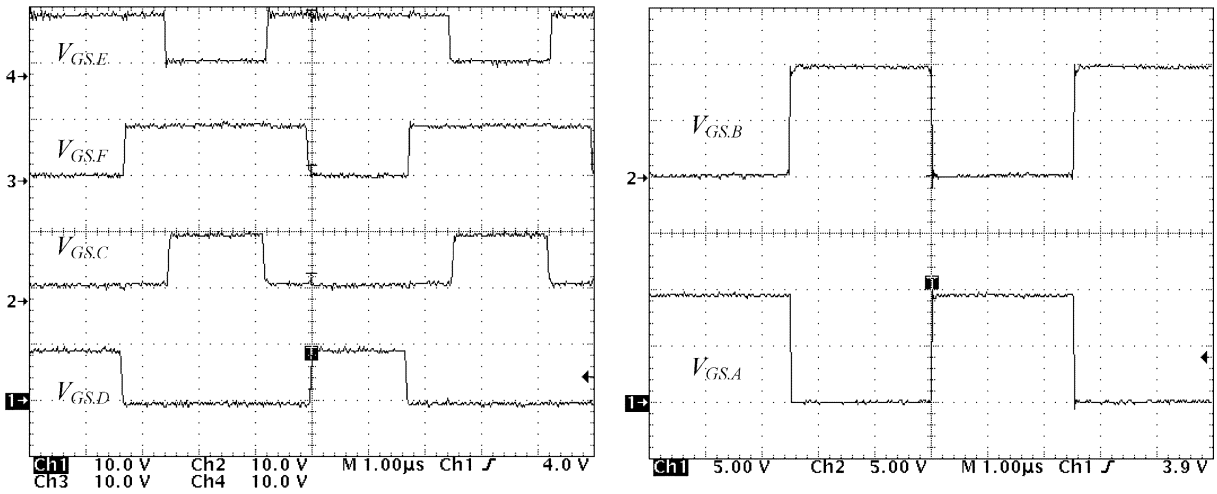


Fig. 14. Control signals of the proposed converter. (a) 1. $V_{GS,D}$ 2. $V_{GS,C}$, 3. $V_{GS,F}$ 4. $V_{GS,E}$; and (b) 1. $V_{GS,A}$ 2. $V_{GS,B}$, time base: 1 μs/div.

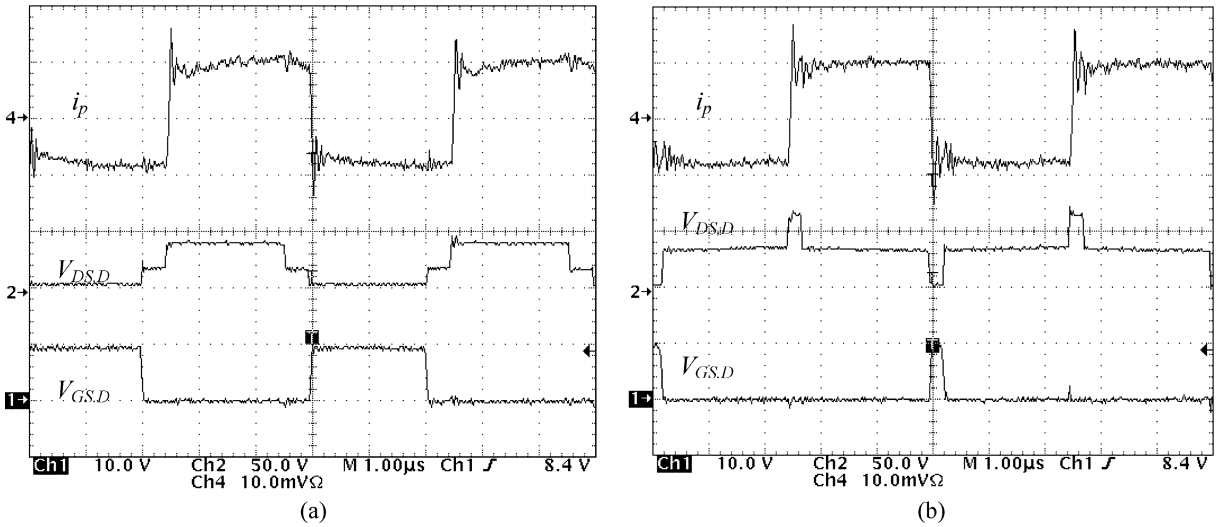


Fig. 15. 1. $V_{GS,D}$, 2. $V_{DS,D}$, 4. i_p(5 A/div) time base: 1 μs/div: (a) $V_{\rm in} = 36$ V and (b) $V_{\rm in} = 62$ V.

which timing method to drive the switches, depending on their preferences or needs.

A. Low Voltage Stresses on Power Switches

The driving signals have the timing as shown in Fig. 12.

Transition From Stage I to Stage II: Beginning from the turning off of Q_D, V_4 increases by the charging of i_p to C_{oss} of Q_D and is clamped to $V_{\rm in}/2$ through the body diode of Q_F. Then Q_F is driven to turn on. Energy is release from L. V_2 rises from nV_o to $nV_o + V_{\rm in}/2$, $V_{ds,B}$ from $2nV_o - V_{\rm in}$ to $V_{\rm in,max}$. ZVS of Q_F can be realized by proper time delay from Q_D off to Q_F on.

Transition From Stage II to Stage III: $V_{GS,B}$ leads $V_{GS,C}$. At the end of stage II, Q_B is driven on. During the slight overlapping of $V_{GS,A}$ and $V_{GS,B}$, $V_{DS,B}$ drops from $2nV_o$ (the maximum input voltage allowed) to 0. With the turning off of Q_A, the voltage at the center-tapping point is clamped to $V_2 = V_p + V_4 = -nV_o + V_{\rm in}/2$, thus $V_{DS,A} = V_{\rm in} - 2V_2 = V_{\rm in} + 2nV_o - V_{\rm in} = 2nV_o = V_{\rm in,max}$. Then Q_E is turned off, followed by Q_C driven on, $V_2 = V_{\rm in} - nV_o$, $V_{DS,A} = V_{\rm in} - 2V_2 = 2nV_o - V_{\rm in} = V_{\rm in,max} - V_{\rm in}$. The operation enters Stage III.

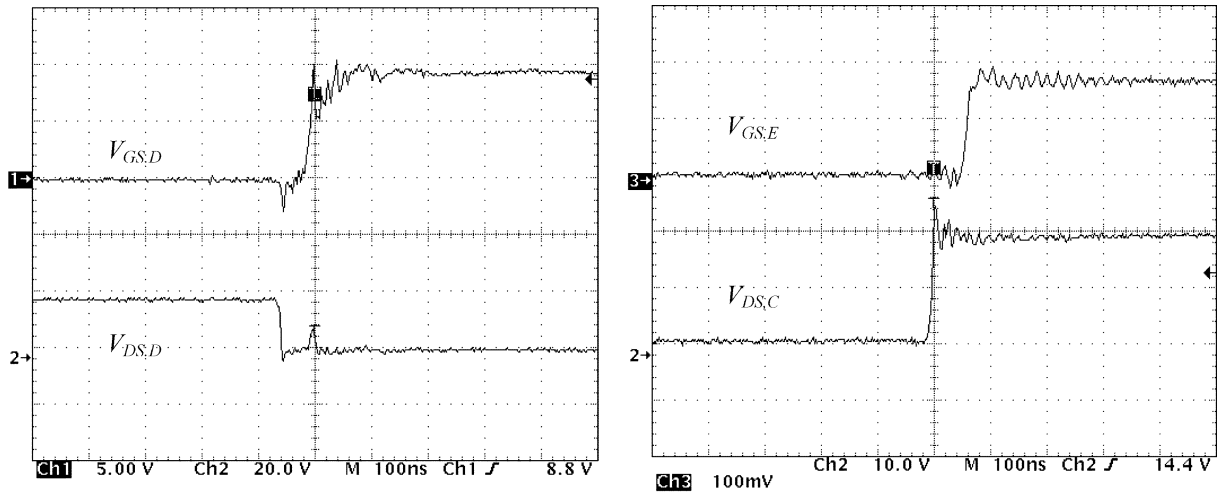
The transition from Stage III to Stage IV is similar to from Stage I to Stage II. And the analysis of transition from Stage IV to Stage I is similar to from Stage II to Stage III.

The voltage spikes on Q_A and Q_B are the maximum input voltage $V_{\rm in,max} = 2nV_o$ with the timing sequences of driving signals given in Fig. 12. Q_E and Q_F may be in ZVS switching but Q_A, Q_B, Q_C and Q_D are all in hard switching.

B. ZVS Switching on Power Switches

For the timing sequences of driving signals as shown in Fig. 13, the transitions from Stage I to II and from Stage III to IV are the same as illustrated in the low voltage stress driving scheme above.

ZVS switching of Q_E and Q_F are realized by the proper time delay from the trailing edges of $V_{GS,C}$ and $V_{GS,D}$ to the leading edges of $V_{GS,E}$ and $V_{GS,F}$, that is Q_E and Q_F are driven on after the voltages on capacitors C_{oss} of Q_C and Q_D are charged by the inductor current to $V_{\rm in}/2$.



(a) (b)

Fig. 16. ZVS of Q_D and Q_E. (a) 1. $V_{GS,D}$ (5 V/div) 2. $V_{DS,D}$ (20 V/div) and (b) 2. $V_{DS,C}$ (10 V/div) 3. $V_{GS,E}$ (5 V/div).

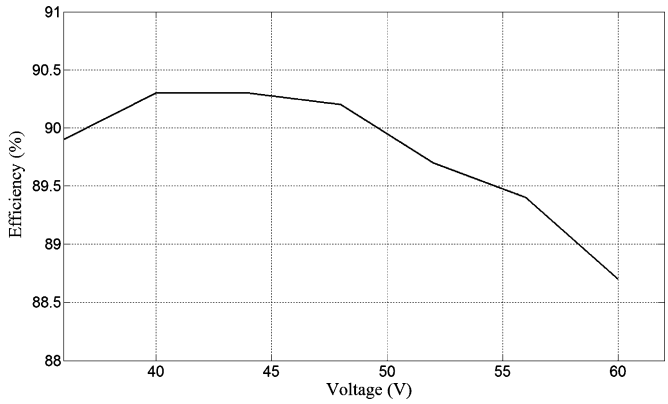


Fig. 17. Efficiency at full load (5 V/20 A, 12.5 V/2 A).

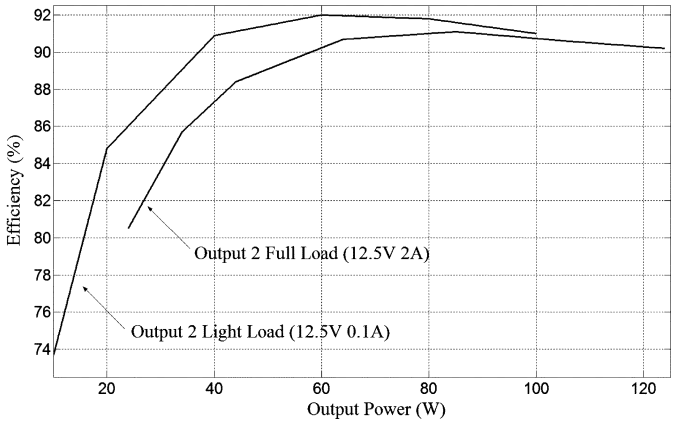


Fig. 18. Efficiency at $V_{\rm in} = 48$ V.

Transition From Stage II to Stage III: At the end of Stage II, Q_E is driven off. Inductor current charges capacitors C_{oss} of Q_D and Q_E, and discharges capacitor C_{oss} of Q_C. The voltage V_4 will be rising until the body diode of Q_C is on. Then $V_{GS,C}$ drives Q_C on with ZVS. In the meanwhile, V_2 changes from $nV_o + V_{\rm in}/2$ to $nV_o + V_{\rm in}$. $V_{DS,B} = V_{\rm in} + 2(V_2 - V_{\rm in}) = 2nV_o + V_{\rm in} = V_{\rm in,max} + V_{\rm in}$. The maximum voltage spike on Q_B may be two times of $V_{\rm in,max}$ at the highest input voltage $V_{\rm in,max}$. Thereafter, $V_{GS,B}$ drives Q_B on, and during the overlapping of $V_{GS,A}$ and $V_{GS,B}$, both $V_{DS,A}$ and $V_{DS,B}$ are zero. Then Q_A is turned off. $V_{DS,A}$ rises to $V_{\rm in,max} - V_{\rm in}$ and the operation enters Stage III.

Transition From Stage IV to Stage I: This transition process is the same as from Stage II to Stage III analyzed above. The ZVS of Q_D is realized with the timing sequences of driving signals as shown in Fig. 13. The maximum voltage spike on transition is $V_{\rm in,max} + V_{\rm in}$ and may be twice as high as the maximum input voltage $V_{\rm in,max}$.

In brief, with the timing sequences of control signals in Fig. 12, the voltage stresses on power switches Q_A and Q_B are the maximum input voltage $V_{\rm in,max} = 2nV_o$, on Q_C and Q_D are the input voltage $V_{\rm in}$, and on Q_E and Q_F are $V_{\rm in}/2$. Only Q_E and Q_F may have ZVS. For the timing sequences as shown in Fig. 13, the voltage spikes on Q_A and Q_B may be twice as high as $V_{\rm in,max}$. The voltage stresses on other power switches are the same as driven by timing sequences in Fig. 12. Q_C, Q_D, Q_E and Q_F may have ZVS but Q_A and Q_B are hard-switched.

V. Experimental Results

The prototype of the proposed current-fed converter with ZVS was built with the specifications: input voltage $V_{\rm in} =$ 48 VDC (36–62 VDC), two outputs of $V_{o1} = 5$ V/20 A and $V_{o2} = 12.5$ V/2 A with total output power of 125 W, and $f = 200$ kHz ($T_0 = 2.5$ μs). Philips planar E22/6/16—3F3 core was used to build the transformer with turns ratios of 6:1 (5-V output) and 6:2.5 (12.5-V output). The inductor was built with Philips planar E18/4/10—250 ($18 \times 10 \times 6$ mm^3, effective volume is 960 mm^3) and had totally 14 turns of center-tapped windings. Comparatively, E22/6/16 size core ($22 \times 16 \times 8.5$ mm^3, effective volume is 2550 mm^3) has to be used for the inductor of the current-fed full-bridge converter. Self-driven synchronous rectifiers of MOSFETs were used for the 5-V output and Schottky diodes for the 12.5-V output.

The coupled inductor was wound to ensure the best coupling between the two windings and minimize the influence of the

leakage inductance. Same consideration was made for the transformer windings. The voltage spikes on switches Q_A and Q_B caused by the stray inductance of the transformer and the coupled inductor in this experiment were 110 V, which is acceptable for Vishay MOSFET Si4488DY with 150-V rated drain-to-source voltage. The voltage spikes may be limited by applying an RC snubber across the inductor between Q_A source and Q_B drain if necessary.

The driving signals have the timing sequence as in Fig. 13 for ZVS of power switches Q_C, Q_D, Q_E and Q_F. Some of the experimental results are shown in Figs. 14–18. Fig. 14 shows the control signal waveforms. Fig. 15 shows the waveforms of (from top to bottom) the primary winding current of the transformer, the drain-source voltage $V_{DS,D}$ and gate-source voltage $V_{GS,D}$ of switch Q_D under 36-V and 62-V input voltages, respectively. The dc offset of the primary winding current in the figure is from the dc current offset of the current probe. The ZVS waveforms of Q_D and Q_E are given in Fig. 16. Full load efficiency curve is shown in Fig. 17. Efficiency curves with 48-V input voltage are given in Fig. 18 for 12.5-V output at 2 A and at 0.1 A, respectively. All efficiency curves are over all efficiencies that include control circuit. It can be seen that with the increase of output power at 12.5-V output the efficiency drops. This is due to the power loss on Schottky diodes of the 12.5-V output is greater than the power loss on the synchronous rectifier of the 5-V output.

VI. Conclusion

A new topology, isolated current-fed dc–dc converter, characterized by small inductor and no deadtime operation, is presented and analyzed. An experimental prototype with 48-V (36–62 V) input and dual outputs of 5 V/20 A and 12.5 V/2 A verifies the validity and merits of the new topology. It has small inductor (corresponding to faster transient response speed), and no RHP zero in its transfer characteristic. Its output ripple current is smaller in contrast to other current-fed topologies [1]–[10], and it has no start-up problem mentioned in [1] and [10]. The main limitations of the new topology are that six power switches are used, and that input voltage range should remain within 2:1 in order to maintain the no deadtime property.

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