# Input-Series Two-Stage DC-DC Converter with Inductor Coupling

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**Abstract: This paper presents an input-series and inductor-coupled two-stage scheme to DC-DC converter. Discussions of the circuit in Discontinuous Conduction Mode (DCM) are provided both when inversely coupled interleaving and when directly coupled without phase shift. According to detailed analysis, inverse coupling is more beneficial for current ripple reduction when the windings are not so tightly coupled. The reason to avoid tight coupling is that current spikes and resonance due to voltage mismatch can be suppressed, since the two coupled windings have a large leakage inductance. A prototype with 500-700V input and 5V/30A output is built. Experimental results verify the principle and performance of the proposed approach.**

## I. INTRODUCTION

For low output voltage and high output current applications, the power loss of the synchronous rectifiers (SRs) on the secondary side can significantly influence the entire power conversion efficiency of a DC-DC converter. However, the efficiency of the secondary SRs is usually poor in single stage converters when the input voltage has a wide range variation. Two-stage [1-6] structure DC-DC converters seem to be a suitable solution for this issue. An obvious advantage of the two-stage [1-6] concept is that fixed duty operation of the second stage helps to improve the performance of the SRs. The voltage and current stress of the SRs are reduced when the input voltage range is wide. This leads to the utilization of MOSFETs with lower on-resistance. Typically, a traditional two-stage low voltage converter utilizes a buck circuit in the first stage to regulate the output. The second stage uses an isolated topology as a "DC transformer" [6] to drop the output voltage of the buck. The second stage operates with a fixed duty ratio (such as 50% for half-bridge). For example, output-inductorless half-bridge with 50% duty can be utilized in the second stage to minimize the output inductor and fasten the response speed [1,2]. The obvious disadvantage of two-stage converters is their higher part count.

To handle especially high input voltage, a new self-balanced input-series two-stage concept [7] has recently been proposed. The approach maintains the benefits of traditional two-stage converters, yet has some additional interesting features. Series connection is applied for the first stage to reduce voltage stress. By choosing suitable topology, the second stage is capable of regulating the charge balance of the first stage as well as improving the performance of the SRs. Similar as many typical two-stage converters, the new approach utilizes output-inductorless half-bridge for the second stage. The two stages are synchronized and operate at the same frequency. Voltage ripple across the intermediate capacitors can be reduced in order to suppress the current ripple of the output-inductorless second stage. According to the analysis, discontinuous mode operation of the first stage is capable of achieving lower voltage ripple.

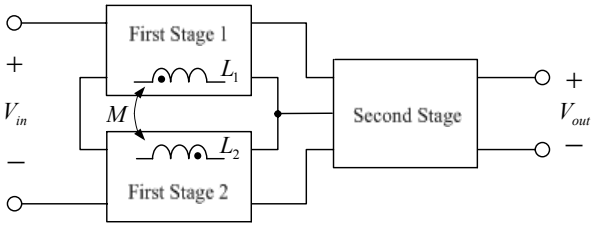


Fig.1 Proposed input-series inductor coupled two-stage scheme

A disadvantage of the new self-balanced input Series concept [7] is that relatively more components are used for input-series two-stage when compared with single stage topologies. To deal with this problem, this paper presents a new input-series and inductor-coupled two-stage scheme, which is shown in Fig.1, to reduce the size and amount of the magnetic components. Unlike typical multi-phase buck circuits with coupled inductor, input-series two-stage topology prefers discontinuous conduction mode (DCM) [7]. Therefore, we present discussions of the circuit in DCM both when inversely coupled interleaving and when directly coupled without phase shift. Inverse coupling is more beneficial for current ripple reduction when the windings are not so tightly coupled. When the coupling is not so tight, current spikes and resonance caused by the voltage mismatch of the two windings can be suppressed. Detailed analysis including the specific consideration for DCM is provided in Section III. *In fact, for a certain current ripple demand, the inductors can be integrated into one magnetic core, and size is significantly reduced by means of suitable inductor coupling design for this specific application.*

## II. OPERATION PRINCIPLE

Fig.2 shows the proposed input-series two-stage converter with inductor coupling, and Fig.3 represents the related

waveforms. $V_{gs1}$, $V_{gs2}$, $V_{gs3}$ and $V_{gs4}$ are the driving signals for the switches on the primary side. As can be seen in the figure, the first stage includes dual interleaved buck converters with coupled inductor. The upper buck consists of $C_1$, $C_3$, $S_1$, $D_1$ and $L_1$. The lower buck consists of $C_2$, $C_4$, $S_2$, $D_2$ and $L_2$. As shown in Fig.2 and Fig.3, $I_{L1}$ and $I_{L2}$ are inductor currents. $I_T$ is the current flowing through the primary winding of the transformer on the second stage. Each buck circuit shares half of the voltage stress. In this paper, an E magnetic core is used. Each inductor ($L_1$ or $L_2$) utilizes one outer leg of the E core for windings. Assume both inductors have an inductance value of $L$. (In practical circuits, there might be a minor difference between the two inductors.) $M$ is the coupling inductance between the two inductors. In Fig.2, the inductors are inversely coupled, and the two buck circuits are interleaved, which can be seen in Fig.3. The second stage uses an output-inductorless half-bridge, which consists of $C_3$, $C_4$, $S_3$, $S_4$, $T_1$, $S_5$, $S_6$ and $L_k$ with fixed operation (50% duty cycle). $L_k$ can be an external small inductor or just the leakage inductance of the transformer.

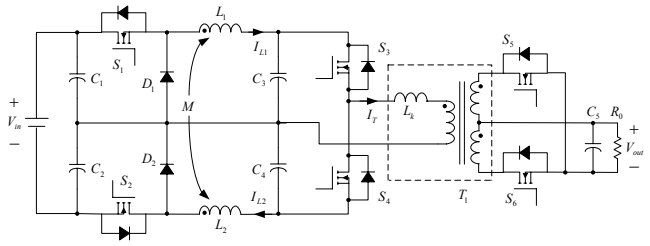


Fig.2 Proposed input-series two-stage converter with inductor coupling

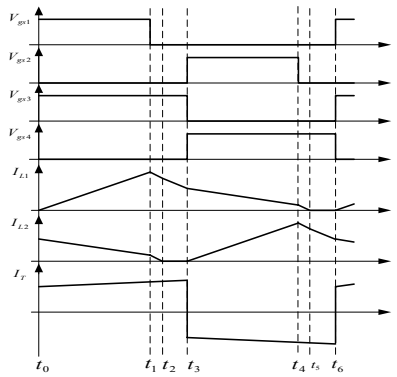


Fig.3 Waveforms of the proposed topology

For the purpose of reducing the voltage ripple across the intermediate capacitors, the first stage operates at discontinuous mode [7]. For the convenience of description, the short transition time of the second stage is not included. Obviously, ZVS for $S_3$ and $S_4$ can be fulfilled during the transition time just as traditional circuits [1-5].

The first stage has two interleaved buck circuits. During $t_0$-$t_1$, $S_1$ is turned on. The upper buck circuit transfers energy from $C_1$ to $C_3$ through $L_1$. The charging current $i_{L1}$, which is shown in Fig.3, increases linearly. At the same time, the current of the lower buck circuit, which is $i_{L2}$, flows through the freewheeling diode $D_2$ and charges $C_4$. The current decreases linearly. During $t_1$-$t_2$, $S_1$ is turned off. Therefore, current $i_{L1}$ goes through the freewheeling diode $D_1$ and starts to decrease linearly. $i_{L2}$ decreases until zero. During $t_2$-$t_3$, the condition of the upper buck is the same as interval $t_1$-$t_2$, but $i_{L2}$ has already been zero. During $t_3$-$t_4$, $S_2$ is turned on. The lower buck circuit transfers energy from $C_1$ to $C_3$ through $L_1$. The charging current $i_{L2}$ increases linearly. In the mean time, the current of the upper buck circuit, which is $i_{L1}$, flows through the freewheeling diode $D_1$ and charges $C_3$. The current decreases linearly. During $t_4$-$t_5$, $S_2$ is turned off. Current $i_{L2}$ goes through the freewheeling diode $D_2$ and starts to decrease linearly. $i_{L1}$ decreases until zero. During $t_5$-$t_6$, the condition of the upper buck is the same as interval $t_3$-$t_4$, but $i_{L1}$ has already been zero.

The second stage operates with a 50% duty cycle. The second stage transfers energy from $C_3$ to the load through the transformer during $t_0 - t_3$. The transformer current $i_T$ flows through $S_3$. The intermediate capacitor $C_3$ transfers energy to the load through the transformer. Also, $C_4$ transfers energy to the load through the transformer and $S_4$ during $t_3 - t_6$.

In this case, the changing rates of the current through inductors are reduced during $t_0 - t_1$ and $t_3 - t_4$ due to coupling of the inductors. Similarly, the changing rates increase during $t_1 - t_2$ and $t_4 - t_5$. Since the buck circuits operate at discontinuous mode, there is no effect during $t_2 - t_3$ and $t_5 - t_6$. $t_0 - t_6$ is defined as one duty cycle $T$. The length of $t_0 - t_1$ and $t_3 - t_4$ are defined as $DT$, which represents the duty ratio.

## III. Analysis of Two Different Coupling Methods in Discontinuous Mode Condition

Inductor coupling has been a popular technology for paralleled interleaving buck circuits in VRMs [8]. This research extends the idea to specific conditions in the proposed input-series two-stage converter, which has two DCM buck circuits with BALanced Output-series Operation. Using the derived equations below, optimized design can be achieved for converters according to their specific requirement. Specifically, a compromise between ripple reduction and current spike suppression should be obtained.

*A. Directly Coupled Operation without Phase Shift*

For two directly coupled inductors, the following typical relations can be obtained [8,9],

$$v_1 = L_1 \cdot \frac{di_1}{dt} + M \cdot \frac{di_2}{dt} \quad (1)$$

$$v_2 = M \cdot \frac{di_1}{dt} + L_2 \cdot \frac{di_2}{dt} \quad (2)$$

In the above case, let $\alpha = \frac{M}{L_1} = \frac{M}{L_2}$. $v_1$ and $v_2$ are the voltages applied on the two corresponding windings. $M$ is the coupling inductance. When the two inductors are directly coupled without phase shift, $v_1$ is equal to $v_2$. According to (1) and (2), the equations related with the calculation of current ripple during rising and falling intervals are derived.

$$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = \frac{V_i - V_0}{1+\alpha} \quad (3)$$

$$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = \frac{-V_0}{1+\alpha} \quad (4)$$

$V_i$ and $V_o$ are the input voltage and output voltage of each buck circuit. $V_i$ is half of the input voltage $V_{in}$ in the proposed topology. The effect of direct coupling relies heavily on the coupling inductance. According to equation (3) and (4), a higher value of $\alpha$ results in a lower current ripple when there is no phase shift. However, for practical circuits, especially for this high voltage application, switches cannot operate exactly simultaneously. Minor mismatch can lead to high current spikes and resonance when the two inductors have good coupling and small leakage inductance ($\alpha$ has a high value close to 1.). Therefore, the coupling between the two inductor windings has to be weakened in order to reduce the current spikes and resonance. The effect of voltage mismatch is suppressed by a bigger leakage inductance. However, the change rate of the current increases with the decrease of $\alpha$ according to equation (3) and (4).

*B. Inversely Coupled Interleaved Operation*

For two inversely coupled inductors, the following typical relations can be obtained [8,9],

$$v_1 = L_1 \cdot \frac{di_1}{dt} - M \cdot \frac{di_2}{dt} \quad (5)$$

$$v_2 = L_2 \cdot \frac{di_2}{dt} - M \cdot \frac{di_1}{dt} \quad (6)$$

Inverse coupling is more flexible to achieve a compromise between ripple reduction and current spike suppression. The reason to avoid tight coupling is that current spikes and resonance due to voltage mismatch can be suppressed since the leakage inductance has a big value. When the two bucks have inversely coupled inductors with interleaved operation in DCM, the following equations are derived. To completely take the advantage of inductance coupling, steady state duty cycle should be chosen so that each inductor current starts to decrease before the other inductor current drops to zero as shown in Fig.3. During Interval $t_0 - t_1$, $V_i - V_o$ and $-V_o$ are applied to the two inductors. Similarly, the change rate of the inductor currents during all intervals can be derived according to (5) and (6).

$t_0 - t_1$: $L_1 \frac{di_{L1}}{dt} = \frac{V_i - (1+\alpha)V_0}{1-\alpha^2}$,

$$L_2 \frac{di_{L2}}{dt} = \frac{\alpha V_i - (1+\alpha)V_0}{1-\alpha^2} \quad (7)$$

$t_1 - t_2$: $$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = \frac{-V_0}{1-\alpha} \quad (8)$$

$t_2 - t_3$: $L_1 \frac{di_{L1}}{dt} = -V_o$,

$$L_2 \frac{di_{L2}}{dt} = 0 \quad (9)$$

$t_3 - t_4$: $L_1 \frac{di_{L1}}{dt} = \frac{\alpha V_i - (1+\alpha)V_0}{1-\alpha^2}$,

$$L_2 \frac{di_{L2}}{dt} = \frac{V_i - (1+\alpha)V_0}{1-\alpha^2} \quad (10)$$

$t_4 - t_5$: $$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = \frac{-V_0}{1-\alpha} \quad (11)$$

$t_5 - t_6$: $L_1 \frac{di_{L1}}{dt} = 0$,

$$L_2 \frac{di_{L2}}{dt} = -V_o \quad (12)$$

As shown in Fig.3, the current ripple is determined by

$$\Delta i_{L1} = \Delta i_{L2} = \frac{V_i - (1+\alpha)V_0}{(1-\alpha^2) \cdot L} \cdot DT \quad (13)$$

Suppose using same inductance value $L = L_1 = L_2$ when no coupling is utilized. Then the current ripple is determined by $\Delta i_{L1} = \Delta i_{L2} = \frac{(V_i - V_o)DT}{2L}$. Therefore, when coupling is utilized, equation (13) yields that $\frac{V_i - (1+\alpha)V_0}{1-\alpha^2} \le V_i - V_o$ should be satisfied in order to achieve a reduced current ripple. In other words, smaller inductance value can be used to satisfy identical current ripple requirement when $\alpha \le \frac{V_o}{V_i - V_o}$. (Remember, $V_o$ is the output of the buck circuit and is not the same as $V_{out}$ of the second stage.) In addition to the value of $\alpha$, the ratio of $V_i$ and $V_o$ also affects the current ripple reduction of inverse coupling.

## IV. Experimental Results

To verify the principle of the proposed topology, a prototype is built. The specification is: 500-700V input, 5V/30A output and 200kHz switching frequency. STD5NK50ZT4 (500V, 4.4A, DPAK) is used for the first stage switches ($S_1$ and $S_2$). IRF3000PBF (300V, 1.6A, SO-8) is used for the second stage

switches ($S_3$ and $S_4$). Each synchronous rectifier ($S_5$ and $S_6$) uses two STS25NH3LL (30V, 25A, SO-8) in parallel. A single E18 Magnetic core is used for the first stage inductors and E22 is utilized for the second stage power transformer. Each first stage inductor uses one outer leg of the E18 core for winding. All the legs have gaps with approximately same distances. Therefore, $\alpha$ is approximately equal to $1/3$. The power transformer of the second stage has 20 turns for the primary winding, 1 turn for the secondary winding.

Fig.4 and Fig.5 show the waveforms of the first stage when the input voltage is 600V. In Fig.4, Channel 1 shows the drain-source voltages of $S_1$. Channel 2 represents the drain-source voltage of $S_2$. Channel 3 shows the current flowing through the inductor $L_1$. Fig.5 shows the drain-source voltages of $S_1$ and $S_2$ and the current flowing through the inductor $L_2$. As described in [7] when there is no inductor coupling, the first stage has discontinuous inductor current at full load. This significantly reduces the size of the inductor as well as reducing the switching power loss for $S_1$ and $S_2$ [7]. The change rate of the inductor current of one buck differs as expected when the other buck operates in a different mode. This phenomenon occurs due to the mutual effect between the coupled windings. By comparing the waveforms from the upper and lower buck circuits, it can be clearly seen that the two parts are self-balanced. Each part shares half of the input voltage. Fig.6 shows the drain-source voltages of $S_1$ and $S_3$ and the current through the primary winding of the transformer. Fig.7 shows the drain-source voltages of $S_1$ and $S_4$ and the current through the transformer. It can be clearly seen that the drain source voltages of $S_3$ and $S_4$ drops to a value close to zero before the currents start to increase. Therefore, Zero-Voltage Turn-On is almost fulfilled for the second stage switches ($S_3$ and $S_4$).

By applying the proposed topology in the built prototype, an efficiency of 89.2% at 600V input and 5V/30A output is obtained. The experimental results verify the principle and performance of the topology.

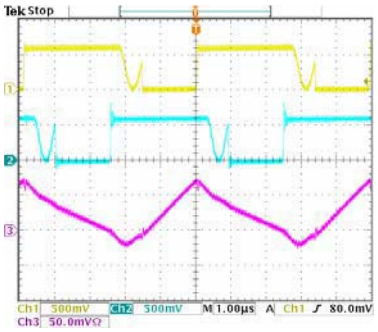


Fig.4 (Vin=600V) $V_{ds\_S1}$ (Channel 1, 250V/div), $V_{ds\_S2}$ (Channel 2, 250V/div) and $I_{L1}$ (Channel 3, 1A/div)

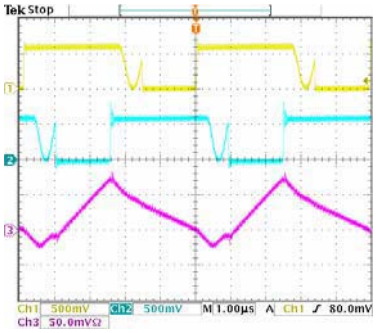


Fig.5 (Vin=600V) $V_{ds\_S1}$ (Channel 1, 250V/div), $V_{ds\_S2}$ (Channel 2, 250V/div) and $I_{L2}$ (Channel 3, 1A/div)

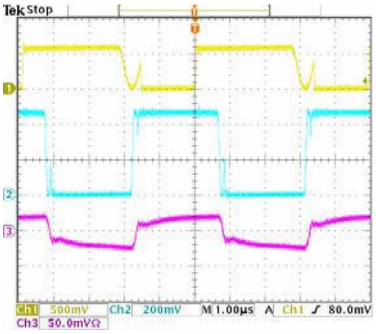


Fig.6 (Vin=600V) $V_{ds\_S1}$ (Channel 1, 250V/div), $V_{ds\_S3}$ (Channel 2, 100V/div) and $I_T$ (Channel 3, 2A/div)

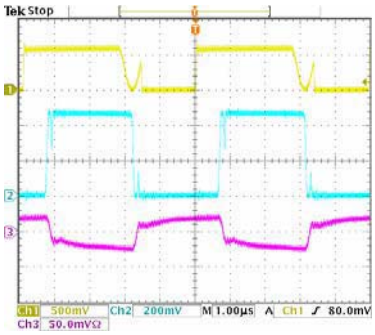


Fig.7 (Vin=600V) $V_{ds\_S1}$ (Channel 1, 250V/div), $V_{ds\_S4}$ (Channel 2, 100V/div) and $I_T$ (Channel 3, 2A/div)

## V. Conclusion

Self-balanced input-series two-stage concept [7] has been proposed to reduce the voltage stress as well as keeping the benefits of two-stage structure. This paper presents a new input-series and inductor-coupled two-stage scheme to further reduce the size and amount of the magnetic components. Discussions of the circuit in DCM are provided for both inverse coupling and direct coupling. According to detailed analysis, inverse coupling is more beneficial for current ripple reduction when the windings are not so tightly coupled. When the coupling is not so tight, current spikes and resonance caused by the voltage mismatch of the two windings can be

suppressed. Experimental results verify the principle and performance of the proposed approach.

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