Three-Level Switching Cell for Low Voltage/High-Current DC–DC Converters

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***Abstract*—New three-level switching cell converter topologies are proposed for transformer isolated low voltage/high current output dc–dc conversion. When compared with corresponding conventional converters without the three-level switching cell, the proposed converters operate with smaller current ripple and reduced voltage stresses. Alternatively, the current ripple size can be kept the same and the filter inductor value can be reduced for higher slew rate. First, the operation principles of these converters are described. Then converter design, control implementation and applications are presented. The capacitor charge balance problem is also addressed. Circuit simulations and experiments verify the basic operation of the new converters and their efficiency improvement.**

***Index Terms*—Synchronous rectification (SR), voltage regulator modules (VRM).**

I. Introduction

TELECOMMUNICATION dc–dc brick converters with low output voltage feed from the nominal 48-V input bus, which often varies from 36 to 75 V. With such a wide voltage conversion ratio, the converter efficiency is usually poor at the highest input voltage due to large ripple current, since design can only be optimized around a specific input voltage. A bigger inductor could be selected to reduce the current ripple, but, at expense of circuit response and board space. So, topologies with inherent low ripple current would be desirable to efficiency improvement without sacrificing the response speed and board space.

On the other hand, voltage regulator modules (VRM) for microprocessor demand faster transient response as load current slew rate keeps increasing. With proposals to increase the input bus voltage of VRM to 48 V, instead of using the existing 12 V and 5 V input bus [1], it is challenging to achieve fast transient response without losing conversion efficiency.

With a properly designed feedback loop, the transient response is mainly determined by the response of the output filter [2]. The output voltage transient can be quickened by decreasing the filter inductor and/or by increasing the voltage applied to the inductor. The filter inductor can be reduced by increasing switching frequency. But, simply increasing switching frequency would degrade efficiency for low-voltage/high-current converter with synchronous rectification (SR) [3]. A few alternative approaches [3], [4] have been investigated to reduce the filter components and to improve the transient response.

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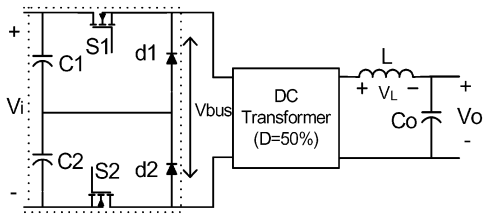


Fig. 1. General three-level voltage-fed converter structure.

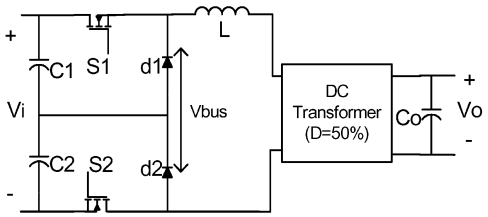


Fig. 2. General three-level current-fed converter structure.

[3] reduces the inductance by operating two or more individual converters in parallel with interleaved gating signals, and [4] uses a step inductor to minimize the inductor in transient regulation.

In recent years, more attention has been drawn to three-level power electronic converters. These converters were first derived from multilevel inverter topologies [5], [6], which were originally proposed to reduce device voltage stress for high-voltage/high-power applications, with a feature of low ripple current for inverter applications. The approach was then extended to three-level dc–dc converters, focusing on half-bridge type topologies [7]–[10] with soft switching. However, since their transformer voltage can only be in two voltage levels, $V_i/2$ or 0, the ripple current is not reduced.

To take advantage of three voltage levels, some nonisolated dc–dc topologies have recently been developed [11]–[15]. They have low current ripple for wide conversion ratio range. Among them, the three-level boost converter in [11] addresses ripple current reduction in PFC application. A family of six nonisolated dc–dc converters and another version of these converters are derived in [12] and [13], respectively, where circuits in [13] are the extension of the early version in [14]. The topologies in [13] and [14] have common grounds for the inputs and outputs. Also, further development of three-level boost converters with coupled interleaving operation has been reported in [15], to further reduce the ripple current and alleviate the diode reverse recovery.

A few isolated topologies were also reported to have the capability of three-voltage-level operation [16]–[22]. The topologies proposed in [16] and [17] utilize two transformers to create three

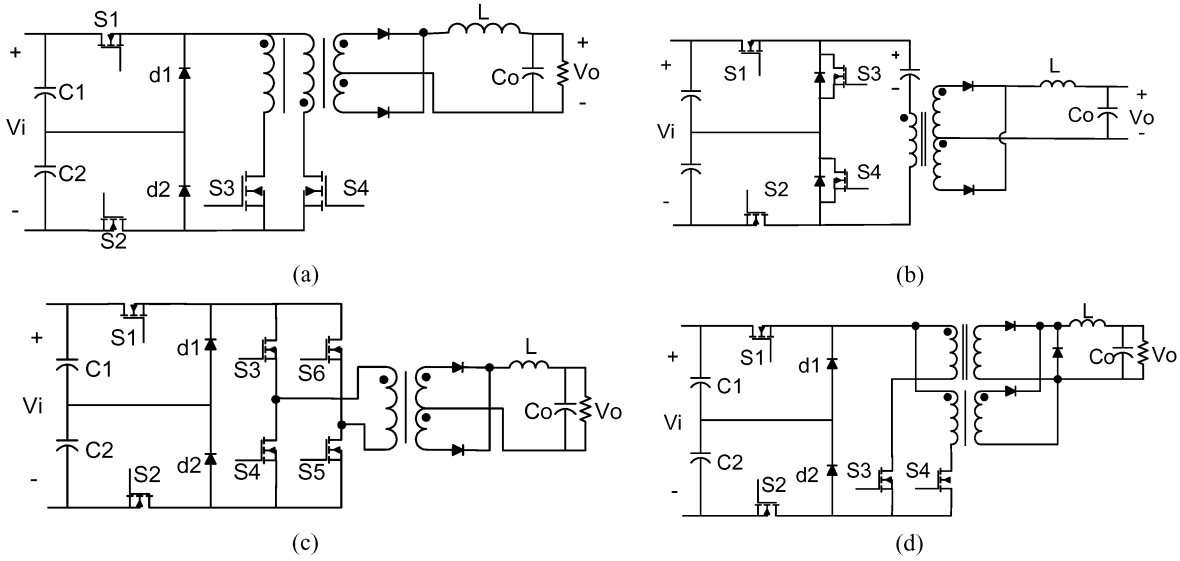


Fig. 3. Three-level topologies for high voltage input, low voltage output dc–dc conversion. (a) Three-level switching cell push–pull converter. (b) Three-level switching cell asymmetrical half-bridge converter. (c) Three-level switching cell full-bridge converter. (d) Three-level switching cell dual-forward converter.

voltage levels and, therefore, require additional board space. The topology in [18] is more related to the present research: It proposes an additional bridge leg to standard full-bridge converters, and is able to create three voltage levels. However, the approach leads to additional complexity of the circuits, e.g., an additional bi-directional switch. Finally, an interleaved three-level boost converter utilizing the "dc transformer" is also proposed in [20], and a hybrid version of conventional [7]–[10] three-level topologies is presented in [21].

The purpose of this paper is to introduce a new class of isolated three-level buck-derived dc–dc converters[1] The novelty of the converters is that the proposed three-level switching cell can be connected to any type of "dc transformer," and thus are applicable to numerous topologies, such as push–pull, bridge types, dual forward, most current-fed topologies, two-stage converters, etc. A major benefit of the proposed isolated three-level dc–dc converter topologies is that they are able to create three different voltage levels, which as we explain reduces the filter inductor value. The proposed topologies do not require additional transformers and the three-level switching cell is relatively simple to implement.

The general circuit structures are shown in Figs. 1 and 2, where Fig. 2 shows the current-fed version. Different from the conventional three-level half-bridge topologies [7]–[10], the proposed three-level topologies can operate with the additional mode, to handle the wide input voltage range $(V_{imax} > 2V_{imin})$ without increasing the ripple current. These features make them candidates for fast transient, high efficiency, low-voltage/high-current dc–dc converters with wide input range. In comparison with conventional isolated three-level converters [7]–[10], the proposed topologies have the following.

- Small inductor ripple current, leading to reduced size and cost of filter inductor and fast circuit response. For example, in a 36–75 V input, 3.3 V output 100 W converter, inductance can be reduced three times and inductor core volume can be reduced from an E18 core to E14 core, saving 660 mm^3 of board space.
- The ability to operate from wide input voltage range.
- A transformer operating at 50% duty ratio (which we call a "dc transformer"), making self-driven synchronous rectification simple when current-fed or two-stage versions of the converters are used.
- Numerous isolated versions, such as push–pull, full-bridge, dual-forward, etc.

[1]The converters were first introduced in the preliminary version of this paper presented at 2003 IEEE APEC [19].

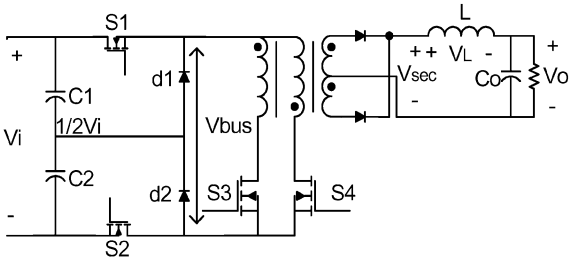


Fig. 4. Three-level push–pull converter.

Further, the converters maintain the known benefits of the conventional isolated three-level converters, such as the following.

- Input ripple current reduced by one-half, which reduces the required size of input filter.
- Voltage stresses of switching cell devices reduced by one-half.

The following sections will investigate some of the new three-level topologies. Section II explains the operation principles of the three-level switching cell with an example converter. Section III discusses the design and other implementation issues. Section IV gives the experimental results.

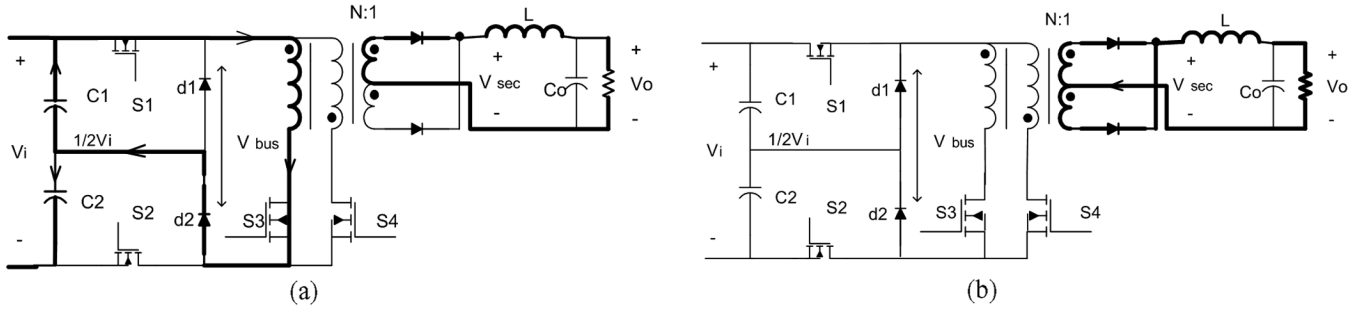


Fig. 5. Mode 1 operation stages: (a) inductor charging stage and (b) inductor discharging stage.

II. New Three-Level High Voltage/Low Voltage Ouput Converters

The proposed three-level switching cell is shown in the dotted line in Fig. 1. It consists of C1, C2, S1, S2, d1, and d2. The general structure of three-level converter consists of the three-level switching cell, a "dc transformer" which operates with 50% duty cycle and a secondary side LC stage.

Definition: An isolated dc–dc converter is said to have a "dc transformer" when 1) its transformer switches operate with fixed duty cycle, typically around 50%, 2) the transformer is followed by rectifiers, and 3) output voltage regulation is achieved by a separate stage.

The "dc transformer" can be a push–pull, full-bridge, dual-forward structure and etc., as Fig. 3 shows. Since the function all the "dc transformers" is the same (to step down their input dc voltage with isolation), and the operation of three-level switching cell is independent of the "dc transformers" topology it connects, the operation principles of all the proposed three-level converters can be presented as a general one. A three-level push–pull converter in Fig. 4 is taken as an example to explain the operation as below.

The converter operates in two modes. The basic principle of the three-level switching cell is to allow $\mathrm{V_{bus}}$ to switch either between Vi/2 and 0 (Mode 1) or between Vi and Vi/2 (Mode 2). Conventionally, without the switching cell, $\mathrm{V_{bus}}$ always equals V_i and 0. Creating this new $\mathrm{V_{bus}}$, as we explain below, reduces the volt–second product on the output filter, and as a result, smaller output filter inductor is needed.

Mode 1: 0 < D ≤ 0.5.: ($Vi \geq 2NV_{\circ}$ in steady state, N is transformer turns ratio.)

S1 and S2 are turned on alternatively with equal time and a duty ratio less than 50%, as shown in Fig. 5. S3 and S4 are turned on complimentarily with 50% duty cycle. S1 and S3 are turned on at the same time instant; S2 and S4 are turned on at the same time instant.

$0 \leq t \leq DT$: At $t = 0$, S1 and S3 are turned on while S2 and S4 are off. As Fig. 5(a) shows, the primary winding current flows from the positive terminal of Vi through S2, S3 and d2. Since the voltage between C1 and C2 is equal to Vi/2, half the input voltage is applied to transformer primary winding, i.e., $\mathrm{V_{bus}}$ =Vi/2. The secondary winding voltage charges inductor L. L current increases and this is the inductor charging stage. The transformer primary current is supplied by the discharging current of C1 and the charging current of C2. Since S2 is open, the input current is equal to charging current of capacitor C2, as Fig. 5(a) illustrates.

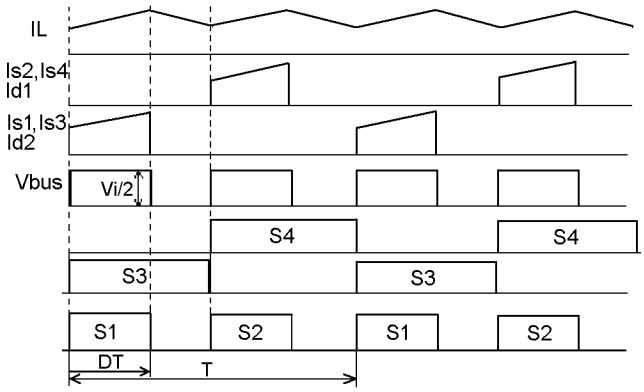


Fig. 6. Mode 1 operation waveforms of three-level push–pull converter.

$DT \leq t \leq T/2$: When S1 is turned off, the inductor L current freewheels via two secondary side rectifiers. The output inductor current decreases, as shown as the inductor discharging stage of Fig. 5(b). Since both S3 and S4 are off, no current flows in the primary windings and $\mathrm{V_{bus}} = 0$.

The next cycle of operation is symmetric to that described above. S2 and S4 are turned on while S1 and S3 are kept off. Half the input voltage is applied to transformer primary winding and $\mathrm{V_{bus}}$ = Vi/2. The inductor L current increases. The transformer primary current is supplied by charging current of C1 and discharging current of C2. The input current is equal to charging current of capacitor C1. After that, S2 is turned off again, L current freewheels and decreases.

Thus, in Mode 1, $\mathrm{V_{bus}}$ is able to switch between Vi/2 to 0 V.

Mode 2: 0.5 < D ≤ 1: (Vi≤ $2NV_{\circ}$ in steady state).

$0 \leq t \leq (D\text{-}1/2)T$: Referring to Fig. 7(a), both switch S1 and S2 are turned on while S3 and S4 operate in the same way as in Mode 1. Assuming that S3 is on and S4 is off, full input voltage is applied to the primary winding of the push–pull transformer. $\mathrm{V}_{bus} = \mathrm{V}_i$. The secondary winding voltage charges inductor L. The input current equals the primary winding current, and this is the inductor charging stage.

$(D\text{-}1/2)T \leq t \leq T/2$: As shown in Fig. 7(b), switch S1 is turned off while S2 is kept on. S3 remains on and S4 remains off. Current is diverted through the diode d1. Subsequently, $\mathrm{V_{bus}}$ changes from V_i to $\mathrm{V}_i/2$, and the primary winding of push–pull transformer is applied with $\mathrm{V}_i/2$. The reflected voltage on the

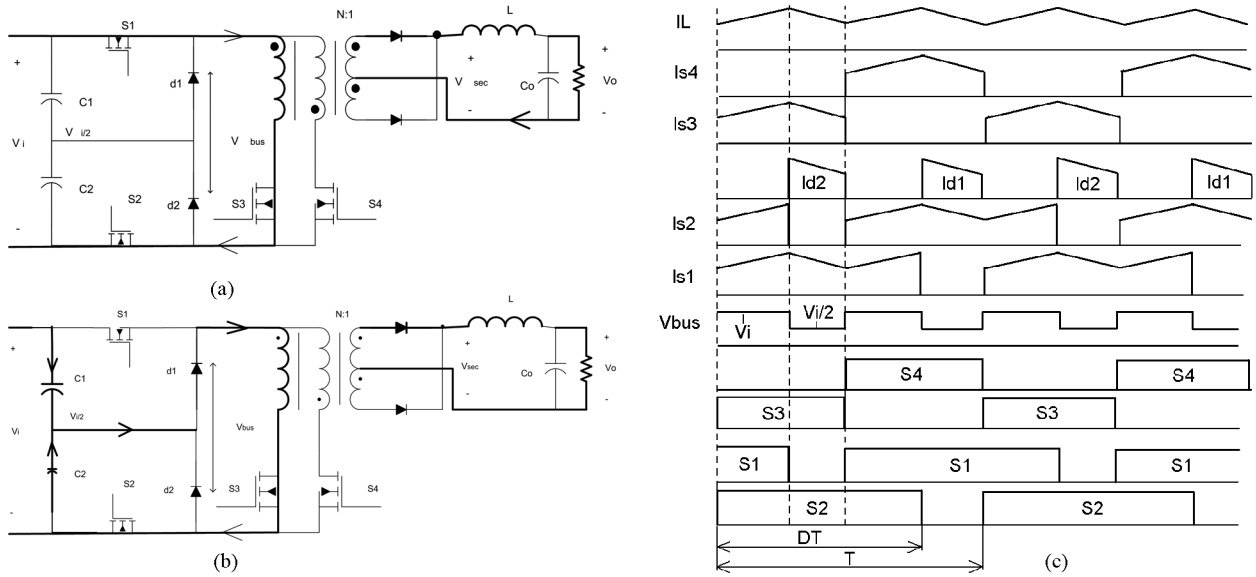


Fig. 7. Mode 2 operation waveforms of three-level push–pull converter: (a) inductor charging stage, (b) inductor discharging stage, and (c) key waveforms.

secondary winding is less than output voltage. The inductor L current decreases, and this is the inductor discharging stage. The primary winding current is supplied by the discharging current of capacitor C2, and by the charging current of capacitor C1. Since S1 is open, the input current is equal to the charging current of capacitor C1, as Fig. 7(b) illustrates.

The next cycle of operation is symmetric to that described above. At first, S1 and S4 are turned on, S3 is turned off, and S2 remains on. So, $\mathrm{V_{bus}}$ goes back to Vi, after d1 stops conducting. The input current flows through another primary winding applied with V_i, and the inductor L current increases. In the next state, S2 is turned off while S3 and S4 remain unchanged. Current is diverted through diode d2 and C2 from the input. $\mathrm{V_{bus}}$ changes from V_i to $\mathrm{V}_i/2$ again. L current decreases once again. The primary winding current is supplied by the charging current of C2, and by the discharging current of C1. The input current is equal to the charging current of C1.

Thus, in Mode 2, $\mathrm{V_{bus}}$ is able to switch between Vi and Vi/2.

From the above symmetric operation, it can be seen that the output voltage is regulated by the duty ratio of S1 and S2, as defined in Figs. 6 and 7. By alternatively turning on S1 and S2 with equal time, the input capacitors C1 and C2 are charged and discharged by the same average current over time, because both the charging and discharging current is half load current reflected in the primary side. So their charges are balanced. Their voltages remain constant and equal to half the input voltage. Moreover, since the peak-peak amplitude of the input current is only half the primary current, the input current ripple is reduced by half compared to that in conventional converters without the three-level switching cell. Thus, a smaller input filter is needed. Besides, all the switching devices in the switching cell are subject to only half the input voltage, since they block $\mathrm{V}_i/2$. This allows low R_{dson} switching devices to be used to reduce the conduction losses. Also, switching losses and reverse recovery losses can be reduced too. Furthermore, unlike the half-bridge type three-level converters [7]–[10], the size of the required output filter is reduced. That is because the voltage across the inductor is equal to $\mathrm{V_{sec}} - \mathrm{V_o}$ in forward converters ($\mathrm{V_{sec}}$ is the voltage after the secondary rectification), and the peak-to-peak value of $\mathrm{V_{sec}}$ has been reduced to $\mathrm{V}_i/2N$, as opposed to being V_i/N in conventional converters. This leads to a reduced voltage-second product in the filter inductor. So the size of the required output filter is reduced, as the next section will show.

The operation slides from one mode to the other mode according to dynamic input and load changes. As D increases above 0.5, S1 and S2 naturally begin to overlap, and the converter enters Mode 2 from Model 1. Mode 1 and Mode 2 have same small signal models: $\hat{\mathrm{V}}_o/\hat{d} = (\frac{V_i}{2N})[s^2LC + s(L/R) + 1]$ (without parasitic parameters), which can be easily proved.

III. Design and Applications of Three-Level Converters

A. Three-Level Converters with Center-Tapped Output

Inductor Design: With the definitions of D in Figs. 6 and 7, the output voltage in Mode 1 and Mode 2 can be expressed in the same formula $V_o = (V_i D/N)$ for the normal output, where N is the transformer turns ratio. Assuming i_{Lp-p} is the required inductor ripple current, the relationship between inductor value and ripple current can be derived as

$$\text{Mode 1}: L = \frac{(1-2D)V_o T_s}{2i_{Lp-p}} \tag{1}$$

$$\text{Mode 2}: L = \frac{(1-D)(2D-1)}{D}\frac{V_o T_s}{2i_{Lp-p}}. \tag{2}$$

For purpose of comparison, the formula for conventional two-level converter without the three level switching cell (standard push–pull) is also given as (3) (Note: two-level converter operates with $T_S/2$ for equivalent comparison)

$$\text{Two-level converter}: L = \frac{(1-D)V_o T_s}{2i_{Lp-p}}. \tag{3}$$

TABLE I
INDUCTOR DESIGN FOR CENTER-TAPPED OUTPUT

	With center-tapped output	
Three-level switching cell converters	Mode 1	$L=\frac{(1-2D_{\min})V_oT}{2i_{Lp-p}}=\left(\frac{1}{2}-\frac{NV_o}{V_{i\max}}\right)\frac{V_oT}{i_{Lp-p}}$
	Mode 2	$L=\frac{\left(\sqrt{2}-1\right)^2}{2}\frac{V_oT}{i_{Lp-p}}$
Conventional two-level converters		$L=\frac{(1-D_{\min})V_oT}{2i_{Lp-p}}=\frac{1}{2}\left(1-\frac{NV_o}{V_{i\max}}\right)\frac{V_oT}{i_{Lp-p}}$

Since the inductor design should take the maximum value for a given $i_{\mathrm{Lp-p}}$ and input voltage range, the design formulas can be found in Table I.

By simple analysis, it can be seen that both inductor determined by Mode 1 and Mode 2 three-level operation are smaller than the typical inductor in conventional converter. Since there are two inductor design formulas, corresponding to two operation modes, the inductor value should be determined by the maximum value of (1) and (2) under given input and output conditions. In the meantime, the inductor value should be minimized by an appropriate design. Since the maximum value of (2) is a fixed number, the maximum value given by (1) should not be larger than this fixed number as long as the duty cycle of (1) is always higher than a minimum duty cycle. The maximum value of (2) is found by taking derivative of (2) and setting it equal to zero. By setting this maximum value equal to the left-hand-side of (1), the minimum duty cycle in (1) can be solved. The corresponding minimum turns ratio can be further found as (4), below, by taking $V_o=(V_iD/N)$ into calculation. When the turns ratio is larger than or equal to the value determined by (4), the inductor value is minimized and determined by the maximum value of (2), which is evaluated at $D=1/\sqrt{2}$, the duty cycle solved from $\partial L/\partial D=0$ of (2). The inductor value is finally solved as (5). However, the turns ratio, N, should not be too big. It should be less than $\mathrm{V_{imin}/V_o}$ to maintain proper operation at $\mathrm{V_{imin}}$, and keep D not to close to 1 in Mode 2, and at same time keep D not to close to 0 at $\mathrm{V_{imax}}$. On other hand, a high turns ratio is not good for optimizing efficiency. Thus, the optimum N is selected to be the minimum N set by (4)

$$N_{\min}\approx(\sqrt{2}-1)V_{i\max}/V_o \tag{4}$$

$$L=L_{\min}=\frac{(\sqrt{2}-1)^2V_oT_s}{2i_{LP-P}}. \tag{5}$$

Compared to the inductor formulas for conventional two-level converter and the bridge-type three-level converter [7]–[10], the inductor in the three-level switching cell converter is about $5.83(1-V_{i\min}/V_{i\max})$ times smaller when transformer turns ratio takes the optimized number. For typical telecommunication power supplies with 36–75 V input, 100 W, 3.3 V output, the inductor value can be reduced by three times, from 900 nH to 300 nH, which corresponds to a reduction from an E18 (960 $\mathrm{mm^3}$) core to E14 (300 $\mathrm{mm^3}$) core. This saves 660 $\mathrm{mm^3}$ of board space.

Input voltage dividing capacitors (C1, C2): The two capacitors with same capacitance (C1, C2) are supposed to hold up half input voltage on each. Their values are determined by their ripple voltage allowed, $\Delta\mathrm{V_{Cripple}}$, since the voltage across the switching devices is equal to $(1/2)\mathrm{Vi}+\Delta\mathrm{V_{Cripple}}$. $\Delta\mathrm{V_{Cripple}}$ can be decided by the exact voltage rating of the selected switching devices. The values of the two capacitors should be larger than those calculated from (6). In the meantime, each input capacitor should have enough ripple current rating to handle input RMS current

$$\begin{aligned}C1=C2&=I_o\Delta T_{\max}/(2N\Delta\mathrm{V_{Cripple}})\\&=I_o\mathrm{T}/(4N\Delta\mathrm{V_{Cripple}}).\end{aligned} \tag{6}$$

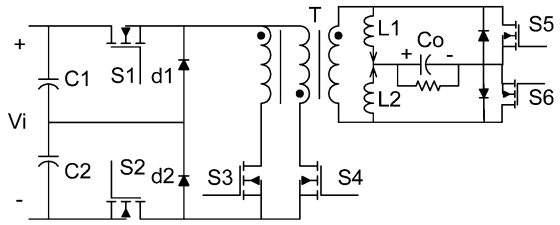


Fig. 8. Three-level push–pull VRM converter with current doubler.

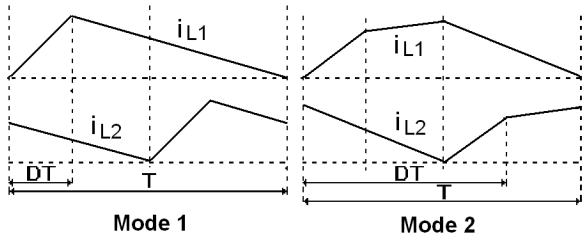


Fig. 9. Inductor current of current doubler of three-level converters.

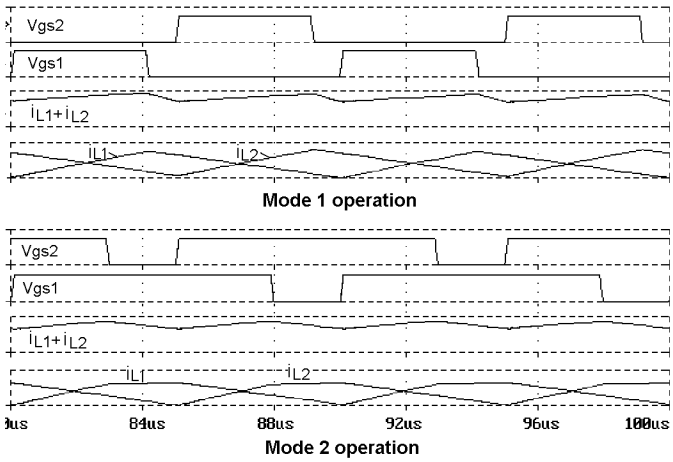


Fig. 10. Simulated waveforms of three-level converter with current doubler.

B. Three-Level Converters With Current Doubler Output

The proposed three-level switching cell converters can be also applied with a current doubler output. Fig. 8 shows a three-level push–pull converter with current doubler output. The inductor current waveforms of the current doubler are drawn in Fig. 9. Its simulated waveforms are shown in Fig. 10. Since current

TABLE II
INDUCTOR DESIGN FOR CURRENT DOUBLER OUTPUT

	With current doubler output	
Three-level switching cell converters	Mode 1	$L=(1-2D_{\min})\frac{V_oT}{i_{p-p}}=\left(1-\frac{4V_oN}{V_{i\max}}\right)\frac{V_oT}{i_{p-p}}$
	Mode 2	$L=\frac{(2D-1)(1-D)}{D}\frac{V_oT}{i_{p-p}}\Big\|_{D=\sqrt{2}/2}=\left(\sqrt{2}-1\right)^2\frac{V_oT}{i_{p-p}}$
Conventional converters		$L=(1-D_{\min})\frac{V_oT}{i_{p-p}}=\left(1-\frac{2V_oN}{V_{i\max}}\right)\frac{V_oT}{i_{p-p}}$

doubler reduces the voltage conversion ratio by half, which is $V_\circ = (V_i D/2N)$ for both modes, transformer turns ratio should be less than $\mathrm{V_{imin}}/2\mathrm{V_\circ}$. The operation of three-level push–pull converter with current doubler depends on the chosen turns ratio of transformer. The breakpoint of Mode 1 and Mode 2 can be determined by:

$$\text{Mode 1} : 4\mathrm{NV_\circ} \le \mathrm{V_i} \le \mathrm{V_{imax}}$$
$$\text{Mode } 2\mathrm{V_{imin}} \le \mathrm{V}_i \le 4\mathrm{NV_\circ}.$$

The ripple currents in terms of inductor values are calculated as below, where $i_{\mathrm{p-p1}}$ is the ripple current of individual inductor and $i_{\mathrm{p-p}}$ is total ripple current

$$\text{Mode 1} : i_{p-p1} = \frac{(1-D)V_\circ T}{L} = \left(1-\frac{2V_\circ N}{V_i}\right)\frac{V_\circ T}{L} \quad (7)$$

$$i_{\mathrm{p-p}} = (i_{\mathrm{L1}}+i_{\mathrm{L2}})(DT)-(i_{\mathrm{L1}}+i_{\mathrm{L2}})(0) = (1-2D)\frac{V_\circ T}{L} = \left(1-\frac{4V_\circ N}{V_i}\right)\frac{V_\circ T}{L} \quad (8)$$

$$\text{Mode 2} : i_{p-p1} = \frac{V_\circ T}{2L} \quad (9)$$

$$i_{\mathrm{p-p}} = (i_{\mathrm{L1}}+i_{\mathrm{L2}})((D-1/2)\mathrm{T})-(i_{\mathrm{L1}}+i_{\mathrm{L2}})(0) = \frac{(2D-1)(1-D)}{D}\frac{V_\circ T}{L}. \quad (10)$$

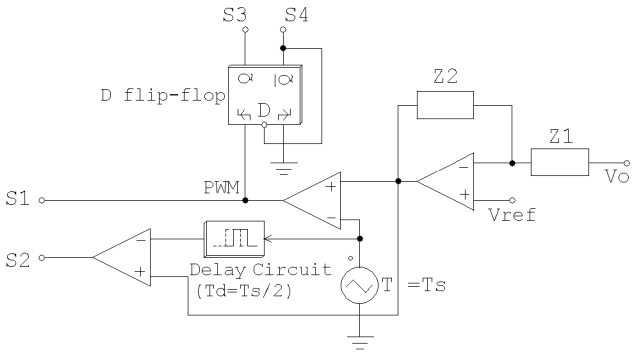
For purpose of comparison, the ripple current in a conventional converter with current doubler converter is also calculated as

$$i_{p-p1} = \frac{(2-D)V_\circ T}{2L} = \left(1-\frac{V_\circ N}{V_i}\right)\frac{V_\circ T}{L} \quad (11)$$

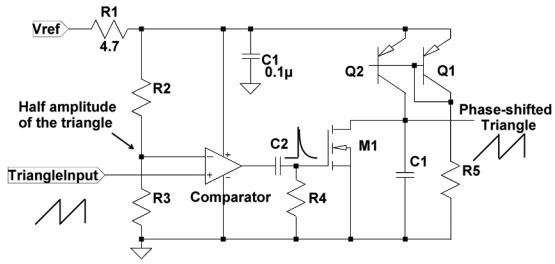
$$i_{\mathrm{p-p}} = (\mathrm{i_{L1}}+i_{\mathrm{L2}})(\mathrm{DT})-(i_{\mathrm{L1}}+i_{\mathrm{L2}})(0) = (1-D)\frac{V_\circ T}{L} = \left(1-\frac{2V_\circ N}{V_i}\right)\frac{V_\circ T}{L}. \quad (12)$$

The inductor will be determined by the total ripple current. Since the inductor design should take the maximum value for a given $i_{\mathrm{p-p}}$ and input voltage range, the design formulas can be found in Table II.

It can be seen from (7)–(12) that both the individual inductor ripple current and total ripple current in three-level converters are reduced compared to those in conventional converters. From Table II, it can be seen that both the inductances determined by Mode 1 and Mode 2 three-level operation is smaller than the typical inductor designed for conventional converters. The choice of inductor design formula between



(a)



(b)

Fig. 11. (a) Simple gating signal generation for three-level converter. (b) Delay/phase-shift circuit of the triangular circuit.

Mode 1 and Mode 2 should be the one giving higher inductance value. By appropriately designing the transformer turns ratio, the inductor value can be minimized to the one determined by Mode 2 formula. A simple analysis shows that the inductor in three-level converter with current doubler can be at least $(1-V_{i\min}/V_{i\max})/(\sqrt{2}-1)^2$ times smaller than the one in the conventional current doubler converter for the same total ripple current, when turns ratio is optimized in $(\sqrt{2}-1)V_{i\max}/2V_o \le N \le V_{i\min}/2V_o$, where $\mathrm{V_{imin}}/2V_o$ is the maximum usable turns ratio and $(\sqrt{2}-1)V_{i\max}/2V_o$ is the optimum turns ratio.

Input Voltage Dividing Capacitors (C1, C2): Similar to the capacitor design for center-tapped output, the capacitors can be calculated as

$$C1 = C2 = I_o\Delta T_{\max}/(4N\Delta V_{\mathrm{cripple}}) = I_oT/(8N\Delta\mathrm{V_{cripple}}). \quad (13)$$

C. Applications of Three-Level Converters

Center-Tapped Output Circuit: From subsection A, it can be seen that the optimum turns ratio for the minimum inductance design in (4) will be limited by $\mathrm{V_{imin}}/V_\circ$ when the highest input voltage increases further. When $(\sqrt{2}-1)V_{i\max}/V_o \ge V_{i\min}/V_\circ$, corresponding an input voltage range of 2.41:1, the optimum turns ratio (4) can not be used, and optimal inductance design determined by Mode 2 formula in Table I does not hold. Instead, $N = \mathrm{V_{imin}}/V_\circ$, the inductance reduction is calculated by dividing the formula for the conventional two-

level converter in Table I with the Mode 1 formula in Table I, giving $(1 - V_{i\min}/V_{i\max})/(1 - 2V_{i\min}/V_{i\max})$ times inductance value reduction for the input voltage range is bigger than 2.41:1.

The above analysis shows that the three-level switching cell converters with a fixed output voltage can accommodate a wide range of input voltage with a much smaller inductor. Likewise, the three-level switching cell converters with a relatively constant input voltage should be able to generate a widely adjustable output. How big the input voltage range or output voltage range can be depends on how many times the inductor value is to be reduced. For three times inductance reduction, a 2.5:1 input voltage range can be obtained by solving the equation $(1 - V_{i\min}/V_{i\max})/(1 - 2V_{i\min}/V_{i\max}) = 3$. The minimum output voltage that can be adjusted down is $V_\circ/2.5$. So the output voltage can be adjusted within [$V_\circ$, 0.4 $V_\circ$].

Current Doubler Output Circuit: Through similar analysis, it is found that the three-level switching cell converters with current doublers can also accommodate the same wide input voltage range with a constant output, or yield the same wide-range adjustable output with a nearly constant input, while using roughly one-of-third inductor value in conventional converters with the same input or output voltage range. The optimum design is valid only when input or output voltage range is less than 2.41:1, which is solved from $(\sqrt{2} - 1)V_{i\max}/2V_o = V_{\text{imin}}/2V_\circ$. After this range, Mode 1 formula should be used ($N = V_{\text{imin}}/2V_\circ$), and the inductance will be reduced by $(V_{\text{imax}}/V_{\text{imin}} - 1)/(V_{\text{imax}}/V_{\text{imin}} - 2)$ times. This reduction can be easily calculated by dividing the formula for the conventional two-level converter in Table II by Mode 1 formula in Table II.

For three times inductance reduction, the input voltage range can be up to 2.5:1 (by solving $(V_{\text{imax}}/V_{\text{imin}} - 1)/(V_{\text{imax}}/V_{\text{imin}} - 2) = 3$). The minimum adjustable output voltage with constant input is $V_\circ/2.5$. So the output voltage can be adjusted within [$V_\circ$, 0.4 $V_\circ$].

D. Control Implementation

The operation slides from one mode to the other mode according to dynamic input and load changes. Mode 1 and Mode 2 have same small signal models: $\hat{V}_o/\hat{d} = (V_i/2)/[s^2LC + s(L/R) + 1]$ (Parasitic parameters are not included.) Control becomes easy. Its control and gating signals can be easily generated, as Fig. 11(a) shows. The driving signals of S3 and S4 can be generated by a rising edge triggered D flip-flop fed with the PWM signal. The S2 driving signal can be generated by comparing the output of error amplifier and a half-cycle delayed triangular waveform. The delay circuit can be implemented as Fig. 11(b). The propagation delay caused by comparator and M1 can be compensated by adjusting R3 a little.

S1 and S2 driving signals should be designed symmetrical with 180° degree phase-shift, so that the charge is balanced in the input capacitors, and the capacitor voltage is equally $(1/2)$Vi. However, due to the unequal delay, propagation time, asymmetrical driving circuit and etc., two driving signals at gates of MOSFETs may turn out to have unequal duty cycle.

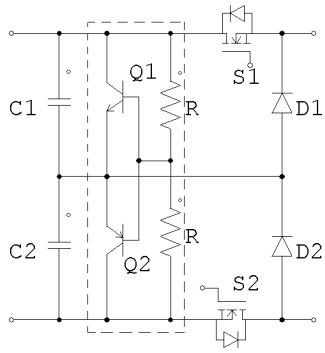


Fig. 12. Correction circuit for balanced capacitor voltage.

This causes the voltages of the two input capacitors to become unequal, hence resulting in unbalanced voltage stresses on the switching cell devices. This research developed a simple correction circuit to solve this problem. The circuit is shown in Fig. 12. It functions in the way that when the C2 has more than half input voltage, the EB junction of the Q2 is forward biased, because the base voltage is set at the half input voltage by the resistor voltage divider. Then Q2 operates in amplification region, drawing current from C2, forcing C2 voltage to drop and C1 voltage to increase. On the other hand, when C2 voltage is less than (1/2)Vi, the BE junction of Q1 is forward biased, since the base voltage is set at (1/2)Vi. Q1 operates to discharge C1 and charge C2, forcing the voltage across C1 and C2 equal to each other. During this time, Q2 does not work. Such a circuit has been proved to be effective in experimental operation.

Without the correction circuit, if the duty cycles of S1 and S2 is a little bit unsymmetrical, there will be an equivalent net charge or discharge current in C1 and C2. This would cause the average voltage of one capacitor to go lower than (1/2)Vi, while the other goes higher than (1/2)Vi. This imbalance stops until each capacitor has equal average charging and discharging current. The small net charging or discharging current can be estimated by (14), where Δd is the difference between the duty cycles of S1 and S2. In order to correct this, Q1 or Q2 in the correction circuit should be able to sink or source an opposite current of the same amount. So, the power loss of Q1 and Q2 should be assessed by $(1/2)V_i * \mathbf{I}_{\text{imb}}$. If there is only a small amount of asymmetry, this correction circuit is simple to implement

$$I_{\text{imb}} = \frac{\Delta d}{N}\left(i_\circ - \frac{(1-D)V_\circ}{2L}\right) + \frac{1}{2}\left[1 - \left(1 - \frac{\Delta d}{D}\right)^2\right] D(1-D)\frac{V_\circ}{LN}T. \quad (14)$$

Of course, the voltage imbalance can also be corrected by the feedback control with an error amplifier which monitors the input capacitor voltages. This can be done by adjusting R5 voltage with an error amplifier output. It will achieve better voltage balance in both steady state and dynamic state without incurring power losses. However, it requires an appropriate control loop design and relevant knowledge of the power circuit model.

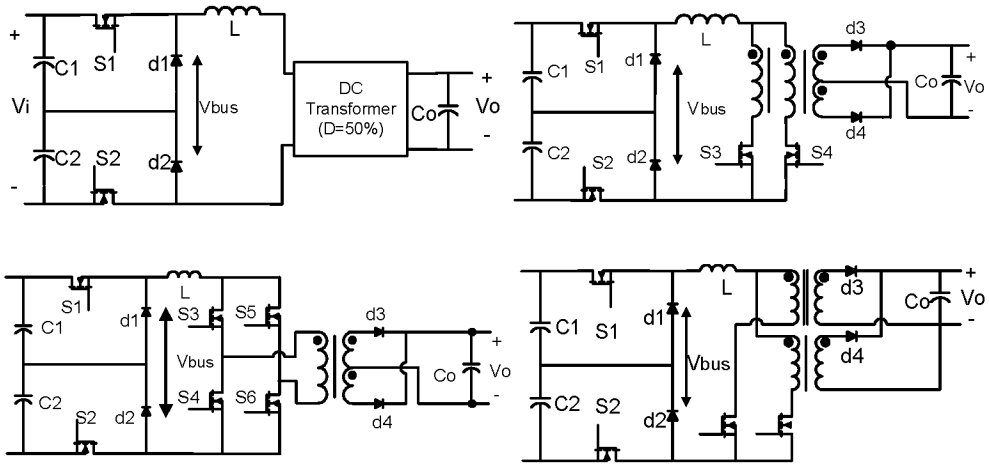


Fig. 13. Three-level current-fed dc–dc converters. (a) General three-level current-fed converter structure. (b)Three-level current-fed push–pull buck converter. (c) Three-level current-fed full-bridge converter. (d) Three-level current-fed dual-forward converter.

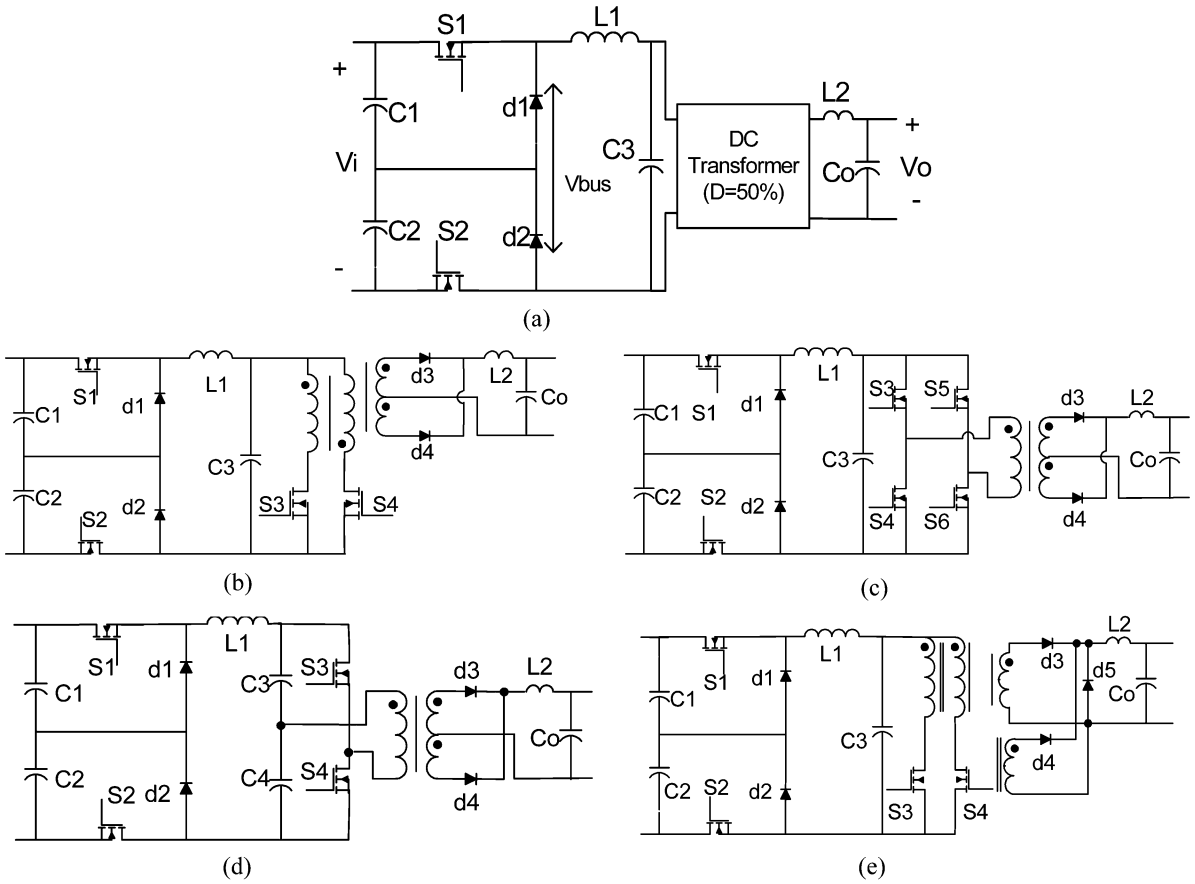


Fig. 14. Three-level two-stage dc–dc converters. (a) General three-level two-stage converter structure. (b) Three-level two-stage push–pull converter. (c) Three-level two-stage full-bridge converter. (d) Three-level two-stage half-bridge converter. (e) Three-level two-stage dual-forward converter.

IV. Various Isolated Three-Level DC–DC Topologies

A. Current-Fed Topologies

The three-level switching cell converters proposed in Fig. 3 can also be extended into current-fed topologies, as shown in Fig. 13. The operation of these topologies is similar to that of voltage-fed topologies as described in Section II. The switches in three-level switching cell operate in the exactly same way as those in voltage-fed push–pull topology in Section II, creating the same three-level bus voltage. The transformer switches are also operated with fixed 50% duty ratio, and synchronized to the turn-on of the switching cell switches, as described in Section II. The three-level bus voltage is filtered by the primary-side inductor and output capacitor. The benefits of current-fed topologies are a) synchronous rectification is optimized since transformer voltage is stepped down and pre-regulated; b) easy high

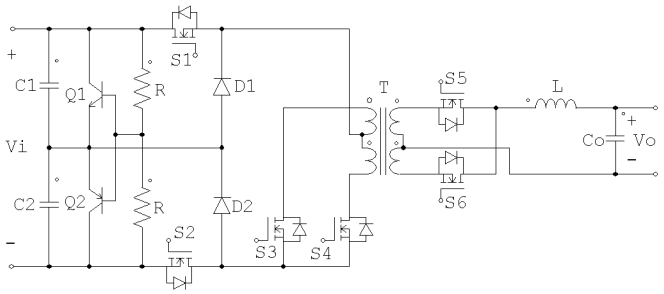


Fig. 15. Experimental circuit of three-level push–pull converter.

efficiency self-driven SR taken from secondary winding; c) less conduction losses with filter inductor on the high voltage side; d) no cross-conduction problem with the transformer switch, and e) no stepping dc magnetization problem in push–pull transformer. To alleviate the voltage spike between the inductor and transformer winding, a RC snubber may be added.

B. Two-Stage Topologies

The three-level switching cell can also be applied in two-stage topologies, which were reported to have high efficiencies in low output voltage application [22]–[24]. It can be seen from Fig. 14(a) that it consists of a three-level switching cell attached to a first LC filter, a dc transformer and a second LC filter. The same operation principles described before still applies. The only topological difference is that there is an LC filter on the primary side. The transformer stage and secondary side LC acts as a second relatively independent dc–dc converter, but with a fixed 50% duty ratio. The regulation is performed by operating the three-level switching cell as before. The primary side LC filter averages $V_{\rm bus}$, which is then sent to the dc transformer. Some three-level two-stage topologies are shown in Fig. 14(a)–(e).

V. Experimental Implementation

An experimental three-level push–pull 36–75 V input, 3.3 V output dc–dc converter [Fig. 3(a)] has been constructed, as shown in Fig. 15. The switching frequency is 165 kHz. The components are listed as following: S1 and S2: Si4480x2, S3 and S4: PhZ5NQ10T, D1 and D2: B1645; Q1: 2N4401, Q2: 2N2907, R: 22K, C1, C2: 10 μF/50 V, Transformer: E22 with turns 12:2, S5, S6: Si4466x3, L: 300 nH, $C_{\rm o}$: 440 μF. S5 and S6 are driven by the same timing signals of S3 and S4.The key operation waveforms are shown in Figs. 16–19, from which it can be seen that the converter accommodates input voltage that varies from 36–75V with two operation modes. Fig. 17 shows the current ripple is close to zero when V_i equals $2NV_{\rm o}$. Comparing to the conventional two-level operation with the switching cell in Fig. 15 removed, it can be seen that the inductor ripple current for the new three-level converter is three-times smaller that that in the conventional converter without the switching cell (compare Fig. 18 with the results with switching cell removed in Fig. 19). The spikes in Fig. 16–18 are caused by the switching transition of the three-level switching cell. In Mode 1, S1 and S2 are subject to a voltage less than $(1/2)$Vi before turn-on of S1 or S2, since there is no current in the primary-side circuit. After turning on

Fig. 16. Mode 1 (Vi= 70 V), R1: Vgs1, 20 V/Div, M1: Vgs2, 20 V/Div, R3: Vbus, 20 V/Div, R4: IL, 8 A/Div.

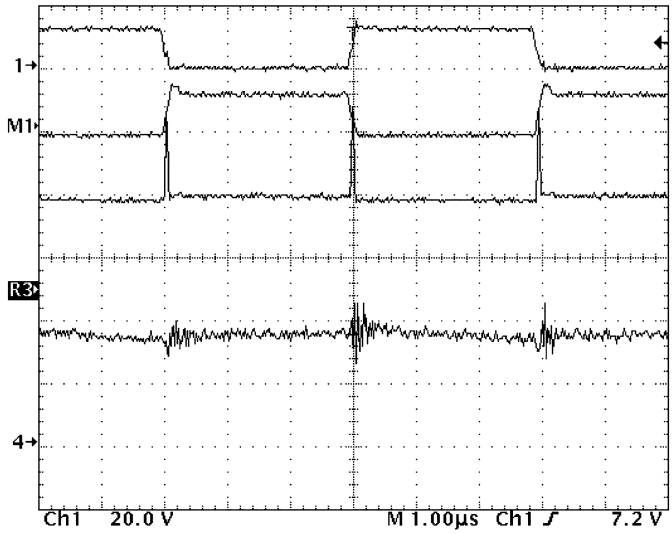


Fig. 17. Boundary of Mode 1 and Mode 2 (Vi=56 V) Ch1: Vgs1, 20 V/Div, M1: Vgs2, 20 V/Div, R3: Vbus, 20 V/Div, Ch4: IL, 8 A/Div.

S1 or S2, initially the voltage applied to $V_{\rm bus}$ is higher than (1/2)Vi and then settles down at $(1/2)$Vi as the switching cell diode conducts. In the boundary of Mode 1 and Mode 2, due to the short common conduction of S1 and S2, the $V_{\rm bus}$ goes higher than (1/2)Vi momentarily. In Mode 2, when S1 or S2 is turned on, the conducting switching cell diode experiences hard turn-off, causing parasitic oscillations. The power circuit efficiencies were measured, as shown in Fig. 20, with the same inductor and switching frequency. Fig. 20 shows the efficiencies at various input voltage, where efficiencies become lower when the input voltage increases. But in general, high efficiencies are achieved. In the prototype, controlled-driven synchronous rectification is employed on the secondary side.

If the same ripple current is kept, the inductor can be reduced three times accordingly. It can be expected that the circuit response could be quickened if the control loop is appropriately designed. That is, since the slew rate of the inductor is three times faster, the circuit can respond three times quicker to load

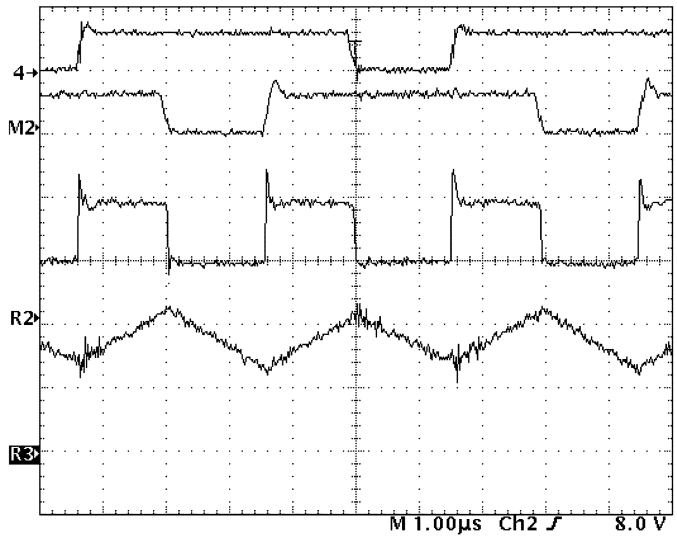


Fig. 18. Mode 2 (Vi=36 V), Ch4: Vgs1, 20 V/Div, M2: Vgs2, 20 V/Div, R2: Vbus, 20 V/Div, R3: IL, 8 A/Div.

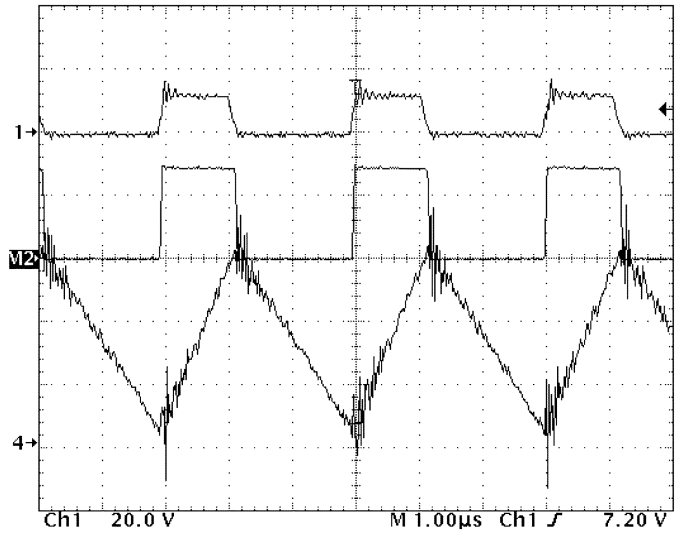


Fig. 19. Two-level operation with Vi = 36 V, Ch1: Vgs, 20 V/Div, M2: Vbus, 50 V/Div, Ch4: IL, 8 A/Div (Same conditions as Fig. 18, only now with the three-level switching cell removed.).

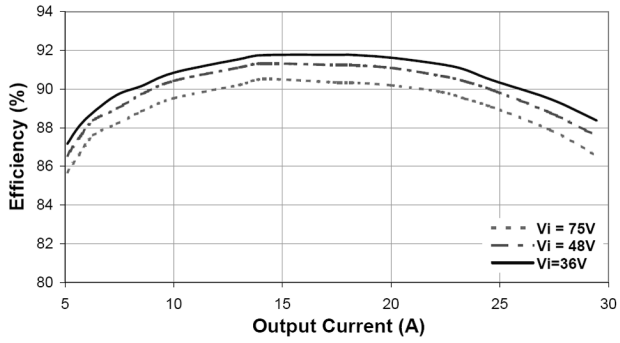


Fig. 20. Efficiencies of experimental three-level dc–dc converter.

changes—see [25] for more discussion on the relation of slew rate to dynamic response.

VI. Conclusion

This paper presents new three-level converter topologies that feature small inductor ripple current. The switches in the switching cell were shown to have low voltage and switching stresses for wide high input voltage range applications. High efficiency can, therefore, be obtained. Circuit response can also be improved as a result of reduction of filter inductor if ripple current is kept same. The proposed three-level cell can also be applied to numerous topologies. It is also noticed that the proposed topologies are not limited for low voltage low power application, they are also suitable for high voltage/high power conversion. However, the approach also has some disadvantages: extra switching devices and associated driving circuits are needed.

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