Dual Interleaved Active-Clamp Forward With Automatic Charge Balance Regulation for High Input Voltage Application

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***Abstract*—This paper proposes a new dual interleaved active-clamp forward topology suitable for high input voltage and high-density application. Two interleaved forward circuits are connected in series on the primary side and in parallel on the secondary side. Therefore, only two high-voltage MOSFETs are needed for the primary switches. Also, the two interleaved parts utilize auxiliary windings to share one capacitor to fulfill active-clamp. Charge balance of the two channels is, thus, regulated by the shared clamping capacitor without demand for extra control schemes. Through the resonance between the magnetizing inductors and the equivalent capacitors of the switches during the transition time, switching loss of the primary switches can be reduced. Interleaved operation reduces the size of the output filter inductor. Based on detailed analysis, a prototype with 220–400-V input and 5-V/30-A output is built. Experimental results verify the performance of the new topology.**

***Index Terms*—Active-clamp, forward circuit, interleaved.**

I. Introduction

FOR THE DESIGN of high input voltage isolated dc–dc converters, the high-voltage stress of the primary switches is always an important issue that impedes converters to obtain high efficiency and low cost. MOSFETs with high-voltage ratings typically have high on-resistances, which can cause high conduction losses. Switching losses of these high-voltage switches are, also, noticeable. Phase-shifted full-bridge [1], [2] is a popular and reliable topology to achieve zero voltage switching (ZVS). The voltage rating of the primary switches is equal to the input voltage. Three-level [3]–[5] topologies can also realize ZVS and even reduce the voltage rating to half of the input voltage.

Half-bridge and two-switches forward converters are typical alternative candidates for low power and high-density design, since fewer components are utilized. However, the switching losses of these two topologies are usually high, since soft switching cannot be realized without extra auxiliary circuits. This factor usually prevents the circuits from operating at higher switching frequencies to further reduce the size of the converter. Asymmetrical half-bridge [6] seems to be an efficient method to fulfill ZVS for the primary switches. However, asymmetrical voltage and current stresses on the components can cause extra problems when the input voltage or output range is wide. For example, synchronous rectifiers with higher voltage rating are needed at the penalty of degrading the efficiency. Another disadvantage is the higher duty ratio variation, which makes the topology unsuitable for wide range application. Also, for the above three topologies, the voltage stress of the primary switches always exceed the input voltage. When the input voltage has a wide range of variation, the higher maximum input voltage requires the higher voltage rating of the switches.

Active-clamp forward [7]–[17] is known as a simple solution to achieve ZVS by utilizing the energy stored in the magnetizing inductor. The voltage stress on the primary switch is $V_{\rm in}/(1-D)$, which makes it possible to reduce the voltage rating when the input voltage has a wide range variation. For example, if the duty ratio is less than 50% at maximum input voltage, the voltage stress is also lower than twice of the input voltage. Therefore, connecting two active-clamp forward circuits seems a simple solution to obtain both ZVS and reduced voltage rating. A double active-clamp forward [15]–[17] has been proposed to fulfill this purpose. The primary part of these circuits consists of two active-clamp forward circuits and one transformer. Each forward circuit utilizes a separate primary winding of the transformer to transfer energy to the secondary part. But in addition to the two main primary switches, two high-voltage auxiliary primary switches and two high-voltage capacitors have to be used to realize the active-clamp.

This paper proposes a new dual interleaved active-clamp forward topology suitable for high input voltage and high-density application. Two interleaved forward circuits are connected in series on the primary side and in parallel on the secondary side. The two transformers share one low-voltage capacitor for clamping through auxiliary windings and switches. By doing this, the following advantages are obtained.

- *The number of high-voltage components is reduced when compared with double active-clamp forward* [15]–[17], *phase-shifted full-bridge and three-level*. Only two high-voltage switches are used. The auxiliary switches and the clamping capacitor are low-voltage rated components due to the utilization of the auxiliary windings. Although the power conversion efficiency depends on practical design and may not be improved, the cost of the circuit can be reduced.
- *Charge balance of the two channels is regulated by the shared clamping capacitor*. The proposed circuit has no

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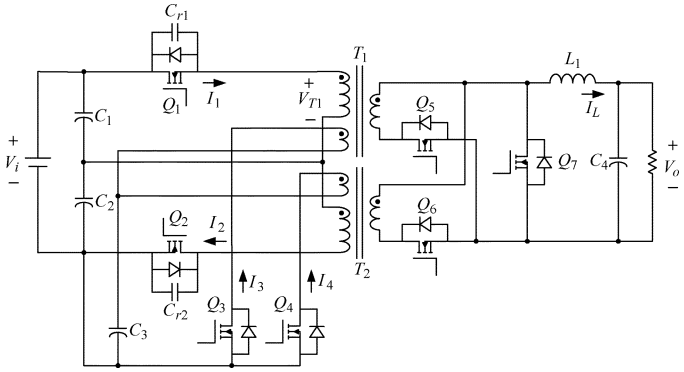


Fig. 1. The proposed dual active-clamp forward topology.

demand for an extra control scheme to adjust for input voltage balance and output current sharing.

- *ZVS of the primary switches can be realized by utilizing the magnetizing inductances of the transformers*. Through the resonance between the magnetizing inductors and the equivalent capacitors of the switches during the transition time, the drain-source voltage of the switches can drop to zero or a low value before the switches are turned ON.
- *Two interleaved channels reduce the size of the output inductor on the secondary side*. When the frequency of the output inductor is doubled due to the interleaved operation, the inductance value is reduced to half of the value that is needed for single channel.
- *Self-driven scheme for synchronous rectifiers can be easily fulfilled*. Unlike some typical topologies with symmetrically driven transformers, such as half-bridge, the driving signals can be easily obtained by combining the signals from the two transformers.

II. Operation Principle

Fig. 1 shows the proposed dual interleaved active-clamp forward topology, and Fig. 2 represents the related waveforms. Q_1 and Q_2 are the main primary switches. Q_3 and Q_4 are the auxiliary switches, which are connected with the reset windings to obtain active clamp. Also, ZVS of the main switches can be fulfilled with their assistance. V_{c1}, V_{c2} and V_{c3} are the voltages across C_1, C_2 and C_3. Capacitors C_{r1} and C_{r2} are the equivalent resonant capacitors of Q_1 and Q_2. C_1, Q_1, T_1, Q_3, and C_3 are the primary side components of one active-clamp forward, while the other forward consists of C_2, Q_2, T_2, Q_4, and C_3. The two forward circuits share the clamping capacitor C_3 so that the charge balances of C_1 and C_2 are kept. Since the control signals of the two channels have the same duty cycle, unbalanced voltage on C_1 and C_2 can generate different magnetizing current to charge the capacitors. Therefore, the two input voltages are adjusted to a balanced value at steady state. Also, the two channels share the freewheeling switch Q_7 and output inductor L_1 on the secondary side. Therefore, there is no current sharing problem. The size of the output inductor is reduced due to interleaved operation. One potential concern is the effect of the leakage inductor between the primary winding and the active clamp winding. The energy stored in the leakage inductor can impose excessive voltage spikes on the switches. This leads to higher voltage stress on the switches and should be taken into account for design. Thus, transformers with tight coupling are required. Also, effective snubber is helpful to reduce the voltage stress. The following description explains the detailed operation principle of the proposed topology.

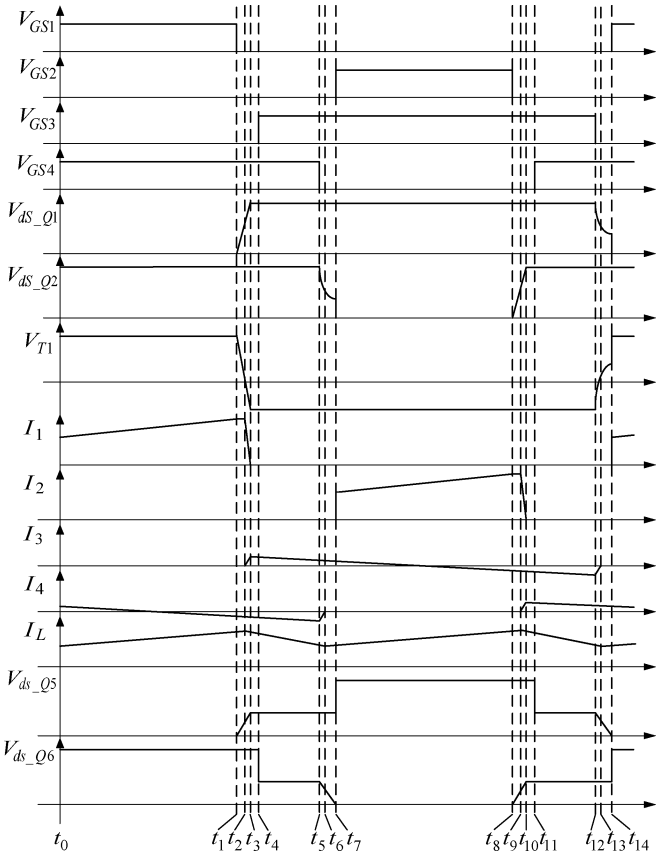


Fig. 2. Waveforms of the proposed topology.

In general, circuit operation can be qualitatively described over several modes/intervals. The upper forward circuit transfers energy to secondary side during time interval t_0–t_1. The under forward circuit transfer energy during interval t_7–t_8. Interval t_4–t_5 and interval t_{11}–t_{12} are utilized for the freewheeling process of the output current. All the remaining intervals are transition intervals and are substantially smaller in length than energy transfer or freewheeling time intervals. Interval t_0–t_{14} is defined as the switching period T. The lengths of t_0–t_1 and t_7–t_8 are defined as DT, which represents the duty ratio, and thus, the duty ratio D will always be less than one-half. The lengths of t_1–t_4 and t_8–t_{11} are set to a suitable value t_d, which is longer than the required transition time t_1–t_3 and t_8–t_{10}.

The length of t_0–t_1 and t_7–t_8 are defined as DT, which represents the duty ratio.

Mode1 (t_0–t_1): The condition of this interval is shown in Fig. 3(a). In this mode, Q_1 is turned on, the voltage across the primary winding of T_1 is equal to $V_{c1} = V_{\text{in}}/2$. The power is transferred to the load through transformer T_1. The output inductor current i_L flows through Q_5 and L_1, and is equal to $(n_p/n_s)I_1$, where I_1 is the current through the primary winding of T_1 shown in Fig. 2. i_L increases linearly according

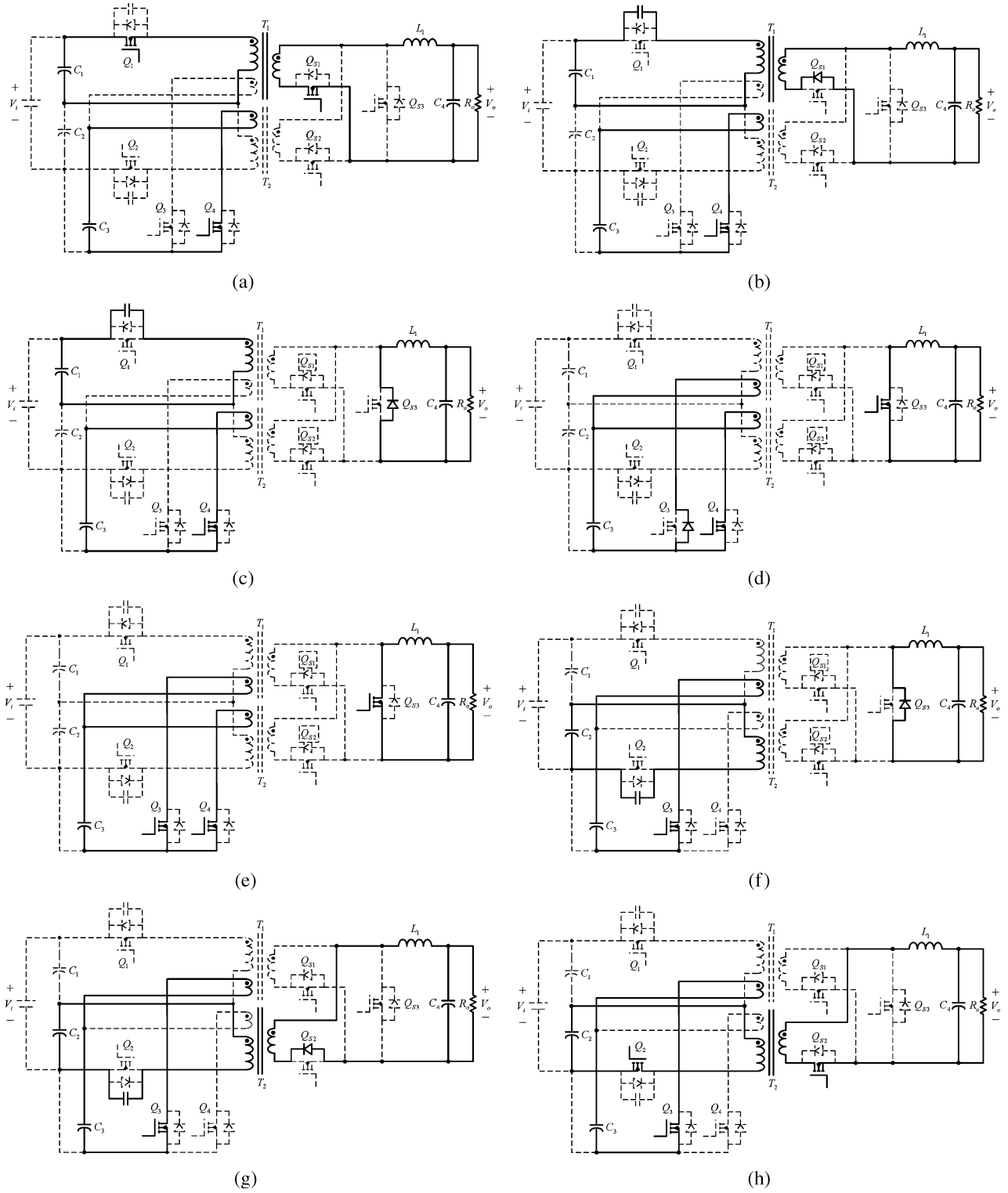


Fig. 3. Detailed description of the operation principle of the proposed topology. (a) The condition of the circuit during t_0–t_1; (b) the condition of the circuit during t_1–t_2; (c) the condition of the circuit during t_2–t_3; (d) the condition of the circuit during t_3–t_4; (e) the condition of the circuit during t_4–t_5; (f) the condition of the circuit during t_5–t_6; (g) the condition of the circuit during t_6–t_7; and (h) the condition of the circuit during t_7–t_8.

to $L_1(di_L/dt) = (n_s/n_p) \cdot (V_{\text{in}}/2) - V_o$. The voltage across Q_6 is $V_{ds\_Q6} = (n_s/n_p) \cdot (V_{\text{in}}/2) \cdot (1/(1-D))$. The freewheeling switch Q_7 is turned OFF, and its intrinsic diode is reverse-biased. At the same time, Q_4 is turned ON, and C_3 provides clamping voltage for the reset winding of T_2. The magnetizing current of transformer T_2 (equal to I_4 during this interval) decreases linearly from a positive value to negative value. This interval finishes when Q_1 is turned OFF at time t_1.

Mode2 $(t_1 - t_2)$: Fig. 3(b) shows the condition of this transition mode. At time t_1, Q_1 is turned OFF, and the circuit remains in this mode until t_2, when the transformer voltage of T_1 decreases to zero. The primary current of T_1 charges the reso-

nant capacitor C_{r1} from zero to V_{c1}. The charging current (I_1) is almost a constant value. Also, Q_4 is still ON. According to voltage-second balance of the transformer, the voltage across the reset winding of T_2 is $V_{c3} = (Dn_r/2(1-D)n_p) \cdot V_{\text{in}}$. Rectifier switch Q_5 is turned OFF. The voltage across Q_5 starts to increase (until it reaches $(n_s/n_p) \cdot (V_{\text{in}}/2) \cdot (D/(1-D))$ at t_3). In this mode, $V_{ds\_Q6} = (n_s/n_p) \cdot (V_{\text{in}}/2) \cdot (D/(1-D))$. Since the voltage across the secondary winding of T_1 is still positive, the output current flows through the intrinsic diode of Q_5 and L_1. The current value still increases.

Mode3 $(t_2 - t_3)$: This mode starts at time t_2, when the transformer voltage of T_1 reaches zero, and ends at t_3, when V_{T1} reaches $-V_{c3} \cdot n_p/n_r$. During this interval, the voltage across C_{r1} keeps increasing through the resonance with the magnetizing inductance of T_1. At the same time, I_1 decreases to zero. The clamp voltage on T_2 remains the same level as in Mode2. The intrinsic diode of Q_5 is reverse-biased. The output current starts the freewheeling process and flows through the intrinsic diode of Q_7 and L_1. The current value begins to decrease according to $L_1(di_L/dt) = -V_o$. This interval finishes when the voltage across C_{r1} increases to $V_{c1} + V_{c3} \cdot n_p/n_r$. ($n_p$ and n_r are the turn number of the primary and reset windings.)

Mode4 $(t_3 - t_4)$: Once the voltage across C_{r1} reaches $V_{c1} + V_{c3} \cdot n_p/n_r$ at t_3, the magnetizing current of T_1 circulates through the intrinsic diode of Q_3 and decreases linearly. The reset winding of T_1 is clamped by V_{c3}. The magnetizing currents of the two transformers are equal to I_3 and I_4 shown in Fig. 1. Also, the reset winding of T_2 is still clamped. In this mode, the freewheeling switch Q_7 is turned ON and the energy stored in the output inductor L_1 discharges to supply the output power.

Mode5 $(t_4 - t_5)$: At time t_4, Q_3 is turned ON before the intrinsic diode of Q_3 is reverse-biased. The details are shown in Fig. 3(e). Thus, Q_3 realizes ZVS. During this interval, both forward circuits share the clamp voltage from C_3 for their transformer. The magnetizing current of transformer T_1 decreases linearly from a positive value to negative value. The output current continues freewheeling through Q_7 and L_1.

Mode6 $(t_5 - t_6)$: As shown in Fig. 3(f), Q_4 is turned OFF at t_5. In this mode, the voltage across C_{r2} decreases from $V_{c2} + V_{c3} \cdot n_p/n_r$ to V_{c2} through the resonance between C_{r2} and the magnetizing inductance of T_2. V_{ds2} reaches V_{c2} at time t_6. Q_7 is turned OFF. The output current continues flows through the intrinsic diode of Q_7 and L_1.

Mode7 $(t_6 - t_7)$: The interval begins at time t_6, when the voltage across C_{r2} decreases to V_{c2}. At this time, the transformer voltage of T_2 drops to zero. The intrinsic diode of Q_7 is reverse-biased. During this interval, the intrinsic diode of Q_6 conducts the output current. V_{ds2} continues to decrease as in Mode 6 until t_7. The minimum voltage across C_{r2} is mainly determined by input voltage, switching frequency, duty ratio, C_{r2} and the magnetizing inductance of the transformer The leakage inductance between the primary winding and the secondary winding should also be taken into account although its effect is comparatively smaller than the magnetizing inductance) [8], [9].

Mode8 $(t_7 - t_8)$: Q_2 starts to be turned ON at t_7, when V_{ds_Q2} drops to a value lower than $V_{c2} + V_{c3} \cdot n_p/n_r$ or even to zero. Thus, switching loss of Q_2 is greatly reduced. The voltage across the primary winding of T_2 is equal to V_{c2}. The power is transferred to the load through transformer T_2. The magnetizing current of T_2 starts to increase. The output current flows through Q_6 and L_1, and is equal to $(n_p/n_s)I_2$, where I_2 is shown in Fig. 2. At the same time, the reset winding of T_1 is still clamped by V_{c3}.

Since the two interleaved channels operate symmetrically, the interval t_8–t_{14} has similar condition as the interval t_1–t_7, although the conditions of the two forward circuits switch.

Assume the duty ratio of each forward circuit is D ($D < 50\%$), and the turn ratio of each transformer is n_p/n_s. Based on the voltage balance of the output inductor, the input transfer ratio is therefore obtained

$$V_o = DV_{\text{in}} \cdot \frac{n_s}{n_p} \tag{1}$$

where V_o and V_{in} are the output and input voltage of the converter. The transition intervals are neglected since they are comparatively short enough. This circuit is suitable for wide range application when the turn ratio of the transformer is carefully chosen. Due to the voltage balance of the transformer

$$\frac{V_{\text{in}}}{2} = V_{c1} = V_{c2} = \frac{(1-D) \cdot n_p}{D \cdot n_r} \cdot V_{c3}. \tag{2}$$

The voltage rating of the primary main switches (Q_1 and Q_2) is thus obtained

$$V_{ds\_pm} = \frac{V_{\text{in}}}{2} \cdot \frac{1}{1-D}. \tag{3}$$

Also, the voltage rating of the auxiliary switches (Q_3 and Q_4) is

$$V_{ds\_\text{aux}} = \frac{V_{\text{in}}}{2} \cdot \frac{1}{1-D} \cdot \frac{n_r}{n_p}. \tag{4}$$

III. Charge Balance Analysis

When two converters are directly connected in series, a small mismatch in parameters always exists between them. This leads to uneven individual output currents of the converters. As a result, charge balance of capacitors is caused by the unbalanced output currents. Therefore, input-series–output-series connection demands extra control schemes to maintain input voltage balance and output current sharing [18]–[20]. This complicates the design of the system. On the other hand, common-duty-ratio scheme can result in a stable operation for input-series-output-parallel (ISOP) connection [20]. Specifically, the converter with higher input voltage can momentarily produce a higher inductor current. This leads to a higher input current in this converter, which discharges the input capacitor and reduces the input voltage of the corresponding converter. Hence, ISOP converters have a self-correcting mechanism ensures stable operation: Input voltage balance and load current sharing are maintained.

A similar benefit of this proposed topology is that charge balance can be automatically regulated without adding extra control schemes or auxiliary circuits. A benefit compared with ISOP converters is that the output inductor is shared. There is

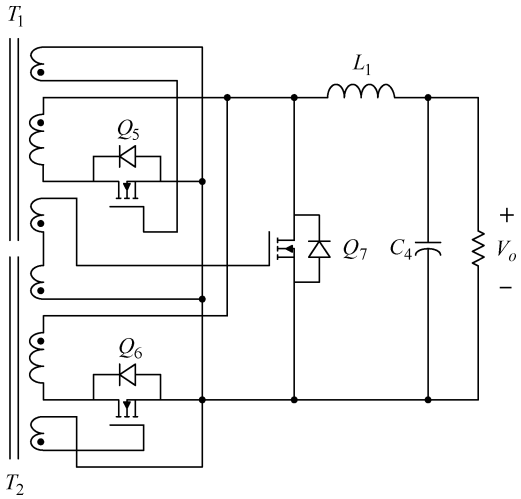


Fig. 4. Self-driven scheme for the proposed topology.

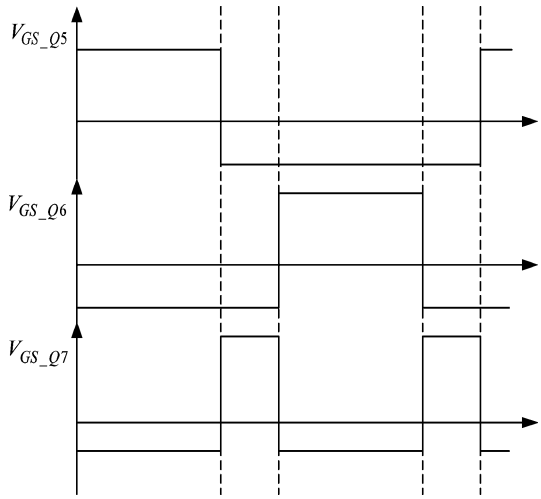


Fig. 5. Timing of the driving signals from the auxiliary winding.

no output current sharing problem, since the two channels share the output inductor on the secondary side and have approximately equal duty ratios. Although the corresponding load currents on the primary side have minor mismatch, the magnetizing currents can be automatically regulated to compensate the mismatch. As a result, equal input currents are achieved for the two channels, and the voltage balance of C_1 and C_2 are kept. As has been introduced, sharing the clamping capacitor, C_3, has the advantage of regulating the magnetizing current and balancing the input voltage of the two interleaved channels. Assume I_{M1} and I_{M2} are the magnetizing current of the two transformers, and $\overline{I_{M1}}$ and $\overline{I_{M2}}$ are the average value of I_{M1} and I_{M2}. In the ideal symmetrical case, $\overline{I_{M1}} = \overline{I_{M2}} = 0$ and $V_{c1} = V_{c2} = (((1-D)\cdot n_p)/(D\cdot n_r))\cdot V_{c3}$. Now, suppose that V_{c1} starts to increase due to a small amount uneven current. This leads to V_{c2} decreasing and $V_{c1} > (((1-D)\cdot n_p)/(D\cdot n_r))\cdot V_{c3} > V_{c2}$. This causes $\overline{I_{M1}}$ to decrease, but makes $\overline{I_{M2}}$ to increase. As a result, C_1 is discharged by the average magnetizing current after sufficient time, which prevents V_{c1} from increasing. Nevertheless, C_2 is charged eventually, and V_{c2} is regulated. Similarly, when $V_{c1} < (((1-D)\cdot n_p)/(D\cdot n_r))\cdot V_{c3} < V_{c2}$, C_2 is discharged by the averaged magnetizing current, but C_1 is charged. Therefore, the charge balance of C_1 and C_2 are automatically adjusted. (Whenever one of the capacitors has lower voltage, the transformer will generate higher magnetizing current to regulate it.)

IV. Self-Driven Scheme for the Proposed Dual Active-Clamp Forward

For the application of low output voltage, high output current, synchronous rectification is a popular technology to achieve high efficiency. Since the proposed topology has two interleaved channels, the freewheeling switch should be turned ON during the deadtime when both of the transformers stop transferring power to the secondary side. Therefore, the situation is similar as some typical topologies with symmetrically driven transformers, such as half-bridge, full-bridge and push–pull. For these topologies, only a few self-driven schemes for synchronous rectifiers have been presented [21]–[23]. The signal from the output inductor has to be included for wide range application [23].

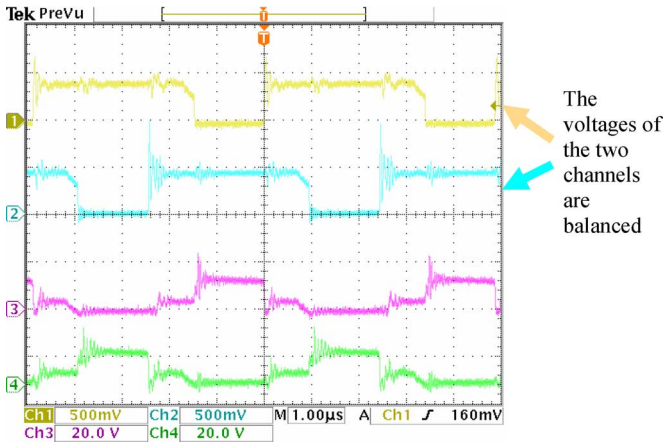


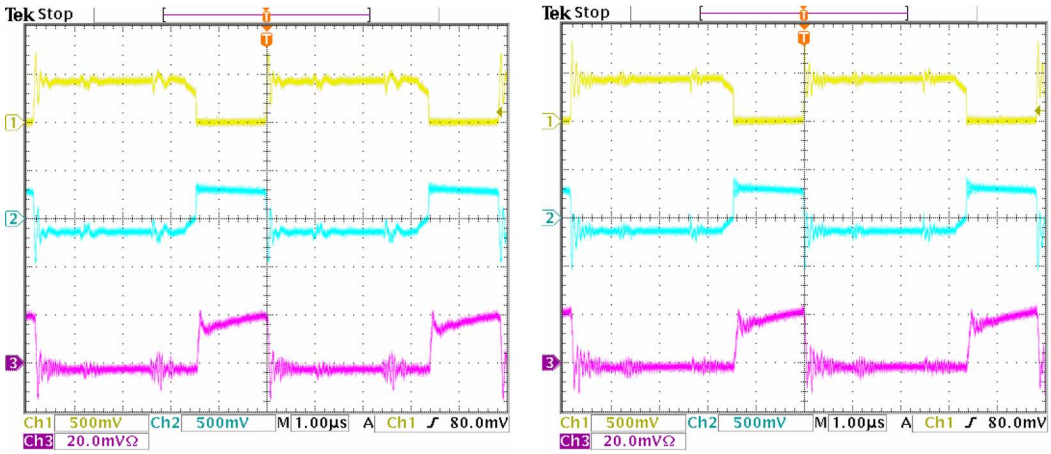
Fig. 6. Waveforms of V_{ds_Q1} (Channel 1, 250 V/div in Y axis), V_{ds_Q2} (Channel 2, 250 V/div in Y axis), V_{ds_Q5} (Channel 3, 20 V/div in Y axis) and V_{ds_Q6} (Channel 4, 20 V/div in Y axis).

Unlike these typical topologies, the proposed dual-channel circuit can easily realize self-driving for the synchronous rectifiers. Fig. 4 shows the diagram of the driving scheme. The auxiliary windings from the two transformers are connected in series to drive the freewheeling switch. Fig. 5 shows the timing of the driving signals. Since the duty ratio of each forward circuit is less than 50%, the voltages across the auxiliary windings are asymmetrical on both directions due to voltage-second balance. Therefore, when one of the transformers is transferring power from the primary side, a negative voltage is applied on the gate of the freewheeling switch. On the other hand, when both the reset windings are clamped by C_3, each auxiliary winding for the freewheeling switch has a positive voltage. The switch is thus turned ON.

V. Experimental Results

To verify the principle of the proposed topology, a prototype is built. The specification is as follows:

- V_{in}: 220–400 V;
- V_o: 5 V;
- I_o: 30 A;
- switching frequency: 200 kHz.



(a) (b)

Fig. 7. V_{ds} of each main primary switch (Channel 1, 250 V/div in Y axis), the transformer primary voltage (Channel 2, 250 V/div in Y axis) and the transformer primary current (Channel 3, 2 A/div in Y axis) of the dual active-clamp forward. (a) Waveforms of forward 1 when V_{in} is 300 V and (b) waveforms of forward 2 when V_{in} is 300 V.

E18 Magnetic core is used for all the power transformers and output inductor. The cross area of the magnetic core is 39.5 mm^2. The power transformers have 32 turns for the primary winding, two turns for the secondary winding and three turns for the auxiliary winding. Using (3) and (4), the benefits of the topology can be directly seen. Ideally, the voltage ratings required for the input voltage range are only less than 260 V for Q_1, Q_2 and 24 V for Q_3, Q_4. In practical application, the influence of the voltage spikes should be considered. STD5NK50ZT4 (500 V, 4.4 A, DPAK) is used for the main primary switches (Q_1 and Q_2). STS7NF60L (60 V, 7.5 A, SO-8) is used for the auxiliary switches (Q_3 and Q_4). Each synchronous rectifier (Q_5 and Q_6) and the freewheeling switch (Q_7) use three STS25NH3LL (SO-8) in parallel. STS25NH3LL has an on-resistance of 3.2 mΩ. These components have small sizes and are suitable for high-density application.

Fig. 6 shows the drain-source voltages of the main primary switches (Q_1 and Q_2) and the secondary synchronous rectifiers (Q_5 and Q_6). The two forward circuits are interleaved. The waveforms of the secondary side are in phase with the primary side. The measured signals are in accordance with the expected waveforms shown in Fig. 2. By comparing the waveforms from the upper and under forward circuits, it can be clearly seen that the two parts are self-balanced by sharing the clamping capacitor. Each part shares half of the input voltage.

Fig. 7 shows the primary side waveforms of each forward. Channel 1 shows the drain-source voltages of the main primary switches (Q_1 and Q_2). Channel 2 represents the voltage across the primary winding of the transformer (T_1 or T_2). Channel 3 shows the transformer primary current (I_1 or I_2, which is shown in Fig. 1). Although only 300-V input is shown, similar waveforms over the entire input voltage range 220–400-V have been obtained, that is, the proposed circuit operates well during the whole input voltage range. As seen in Fig. 7, the voltage across the primary winding of the transformer is equal to half of the input voltage when the main primary switch is turned ON and V_{ds} drops to zero. The transformers have a constant output voltage during the deadtime when the main switches are turned OFF. Thus, active-clamp is fulfilled by applying $V_{c3} = (Dn_r/(2(1-D)n_p)) \cdot V_{\text{in}}$ to the reset winding. The voltage across C_3 is maintained. Also, the drain source voltages of Q_1 or Q_2 decrease by resonance during the transition time before the currents start to increase. Therefore, switching power losses of the main primary switches are reduced. Since the rising slope of the current waveform reflects both the magnetizing current and the ripple of the secondary inductor current, it can be concluded that the inductor current ripple is controlled to a acceptable value.

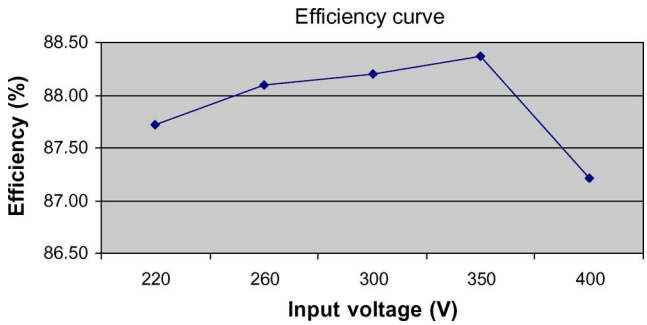


Fig. 8. Efficiency of the built prototype.

By applying the proposed topology in the built prototype, an efficiency of 88.2% at 300-V input and 5-V/30-A output is obtained. Fig. 8 shows the efficiency curve during the whole input voltage variation range. The experimental results verify the principle and performance of the topology.

VI. Conclusion

This paper proposes a new Dual Interleaved active-clamp forward topology suitable for high input voltage and high-density application. Two interleaved forward circuits are connected in series on the primary side and in parallel on the secondary side. The two transformers share one low-voltage capacitor for clamping through auxiliary windings and switches. Charge balance of the two forward circuits can be self-regulated by sharing the clamping capacitor. This method provides a new solution to

reduce the voltage stress and number of components. A prototype with 220–400-V input and 5-V/30-A output verifies the principle of the new topology.

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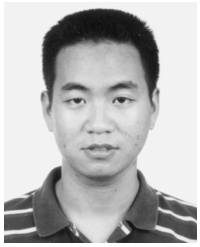

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