Self-Driven Synchronous Rectification Scheme Without Undesired Gate-Voltage Discharge for DC-DC Converters With Symmetrically Driven Transformers

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***Abstract*—This paper proposes a new self-driven synchronous rectification scheme for dc–dc converters with symmetrically driven transformers and wide input voltage range. The driving signals are obtained from the output inductor. Two auxiliary switches are utilized to turn off the main switches properly. Two extra auxiliary switches, which are controlled by a delayed signal from the inductor, are added to avoid the undesired gate discharge. This approach can achieve high efficiency and is suitable for practical applications. Experimental results based on a 36–75 V input, 2.5 V/30 A output prototype are shown to verify the proposed scheme.**

***Index Terms*—Self-driven, synchronous rectification.**

I. Introduction

SYNCHRONOUS rectification is an important technique to achieve high power-conversion efficiency for low-output-voltage and high-output-current dc–dc converters [1]–[7]. Utilizing small-package MOSFETs (which have on-resistances of the order of milli-ohms) instead of diodes can greatly reduce the conduction loss that is caused by the forward voltage drop. It is important to choose suitable driving methods for synchronous rectifiers (SRs) in order to reduce the conduction loss during the entire switching cycle.

For isolated topologies, there are two kinds of driving strategies: self-driven methods that obtain the driving signal directly from the secondary side of the transformer, and controller-driven algorithms that drive MOSFETs by using signals from the controller. An obvious advantage of the self-driven method is that there is no need for driving transformers, especially when the isolation requirement between the input and output is very high. Also, it is easier to generate a driving signal, since it is taken directly from the secondary side of the power transformer. For those topologies with no deadtime operation, such as active-clamped forward, flyback and asymmetrical half-bridge, there is no problem for the implementation of self-driven synchronous rectifiers. However, some very popular and reliable topologies, such as half-bridge, push-pull and phase-shifted full-bridge, have deadtimes[1] in their transformer waveforms. Since the transformers have no output voltage during deadtimes, it is not easy to extend the conduction period of MOSFETs to the deadtimes when using a self-driven method.

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[1]Deadtime is defined as the time interval in which there is no direct energy connection/flow from input to output. For these isolated buck-derived topologies, the deadtime is the interval when the primary switches are off, and no energy is applied to the primary transformer.

To address some of these issues, recent research [3]–[7] proposes several self-driven approaches. In [3], [4], an additional winding of the transformer is connected to the gates of both SRs, and one diode is paralleled between the gate and the source of each SR. These methods depend heavily on the coupling of the transformers. Adding a regulated voltage on the secondary side of the symmetrically driven transformer to help drive the MOSFETs [5] is an alternative solution to extend the conduction period of the MOSFETs to the deadtimes. An approach that combines the signals from the output filter inductor and the transformer in order to keep the MOSFETs operating even during deadtimes, while at the same time turning off the MOSFETs properly, is proposed in [6], [7]. (This scheme first appears in APEC2006 [6]. Then independent research in PESC2006 discusses wide-input-voltage-range applications [7].) Since the driving signals from [3]–[5] have positive voltage steps, the risk of exceeding the maximum gate voltage rating of the MOSFETs increases when the input voltage has a wide range variation. The advantage of utilizing the signal from the output inductor is that a comparatively wider range variation of the input voltage is allowed, as the input voltage range is directly seen on the gate voltage of the auxiliary switches without extra voltage steps [7].

Fig. 1 shows the original circuit that utilizes the output inductor to drive the SRs, as proposed in [6], [7]. A technical challenge of this new approach is that there is unexpected gate voltage discharge, which can influence the gate-voltage retention and add extra power loss in the SRs. This phenomenon is caused by the leakage inductor of the transformer. The voltage spike from the transformer can turn on the auxiliary discharging switches and thus cause undesired voltage drop. Because the SRs should be turned off immediately when the transformer voltage becomes negative, the voltage spike cannot be removed by directly using a filter.

To solve the above mentioned challenges, this paper presents a new, improved self-driven synchronous rectification scheme to reduce the extra power loss. Two extra auxiliary switches are added to block the undesired disturbance and retain the gate-voltage during the entire operation period. The body diodes of the added auxiliary switches provide the path to turn off the original auxiliary switches. The advantages of the proposed method are that undesired gate-voltage discharge of SRs is removed, and power efficiency can be improved.

II. Analysis of Undesired Gate Voltage Discharge

As has been introduced in Section I, the recently proposed schemes utilizing the output inductor to drive SRs have a problem of short-period gate-voltage discharge. The timing of the waveforms is shown in Fig. 2. V_{AUX} is the voltage from the driving winding of the transformer, and V_L is the voltage from the auxiliary winding of the output inductor. V_{GS1} and V_{GS2} are the gate voltages of the SRs (S_1 and S_2). From the figure,

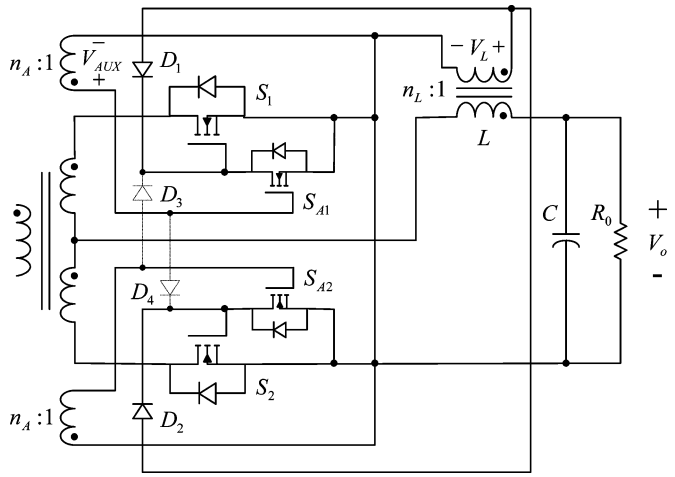

Fig. 1. Recently proposed schemes utilizing the output inductor for SRs [6], [7].

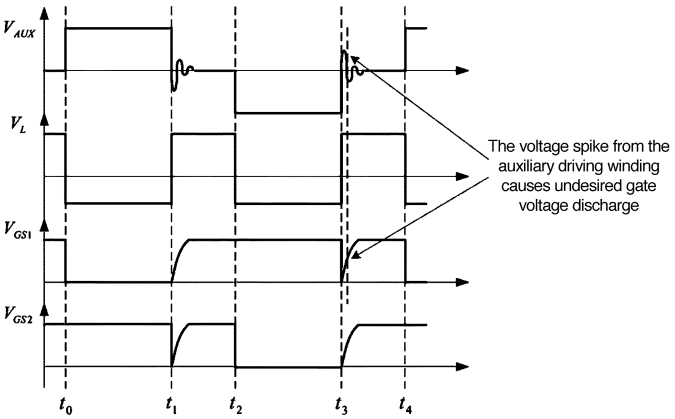

Fig. 2. Timing of the waveforms.

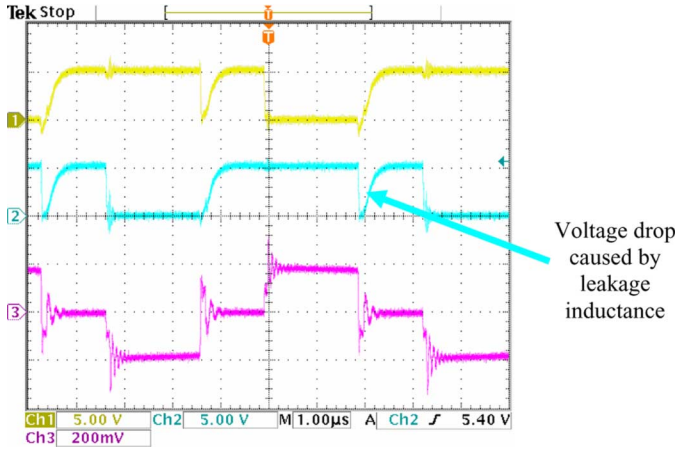

Fig. 3. $V_{\rm gs1}, V_{\rm gs2}$ and $V_{\rm AUX}$ when using the output inductor.

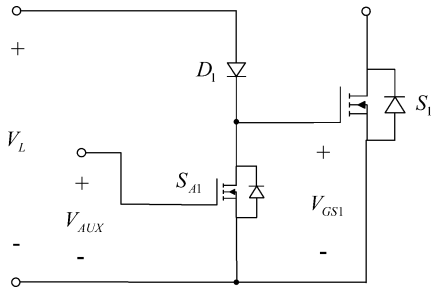

Fig. 4. Simplified diagram for the recently proposed self-driven scheme [6], [7].

a short-time gate-voltage discharge, which is actually caused by the disturbance of the driving winding due to coupling problem, is shown. Fig. 3 shows an experimental waveform of the gate discharge problem (Vin is 48 V, 10 V/div in Y axis.). Channel 1 and Channel 2 represent the gate voltage of S_1 and S_2, respectively. Channel 3 shows the signal from the auxiliary driving winding. The voltage spike from the driving winding turns on one of the auxiliary switches (S_{A1} and S_{A2}), and thus discharges the gate voltage for a short time.

On the other hand, directly dealing with the leakage inductance is not a proper solution because of two factors: Firstly, the gate parasitic capacitors of the auxiliary switches are relatively small and thus sensitive. Even a little leakage inductance can cause disturbance on the gates. Secondly, keeping a certain amount of transformer leakage inductance is vital in order to avoid a short period of over-current in some cases [7]. Since the turn-off signals of the SRs are from the transformer, they still need a short time to rise and trigger the auxiliary switches. During that period, two SRs are on at the same time when the transformer output is not zero. The existence of the leakage inductance can prevent the current from reaching a very high value before one of the SRs is turned off. Therefore, the following analysis and experimental results are based on the condition when the transformer is not tightly coupled.

III. Improved Self-Driven Synchronous Rectification Scheme to Avoid Undesired Gate-Voltage Discharge

According to the above analysis, the existing self-driven synchronous rectification method using an output inductor still has practical problems due to undesired gate-voltage discharge. The voltage spike due to leakage inductance of the transformer can turn on the auxiliary switches. Thus, extra power loss is caused by body-diode conduction. To deal with this problem, this paper proposes a new, improved self-driven synchronous rectification scheme that is capable of avoiding the unexpected discharge. Only small, low-power switches and other components are added. The approach can improve the efficiency of the SRs and is more suitable for practical application. The following analysis discusses the detailed consideration for the improvement.

Fig. 4 shows the simplified diagram for the recently proposed scheme [6], [7]. The gate voltages of the main MOSFETs are rebuilt by the signal from the inductor during the deadtime (period $t_2 - t_3$ for S_1 in Fig. 2). Gate charge and retention of the main MOSFETs are realized by the auxiliary diodes. The auxiliary switches can discharge the retained gate voltage of the main MOSFETs when needed. However, undesired gate discharge caused by the leakage inductance prevents this method from achieving high efficiency. Fig. 5 shows a simplified diagram that explains the basic idea of the proposed self-driven scheme. An extra auxiliary switch is added for each main switch. In this case, S_{A1} is the original auxiliary switch and S_{A3} is the new one. The body diode of S_{A3} provides the path to turn off S_{A1}. Meanwhile,

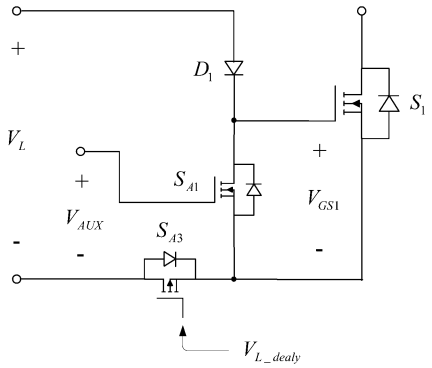

Fig. 5. Simplified diagram for the improved, self-driven scheme. The expected gate discharge of the main switch is guaranteed by turning on S_{A1} and S_{A3} in time. On the other hand, S_{A3} is turned off when needed to block the voltage spike from $V_{\rm AUX}$.

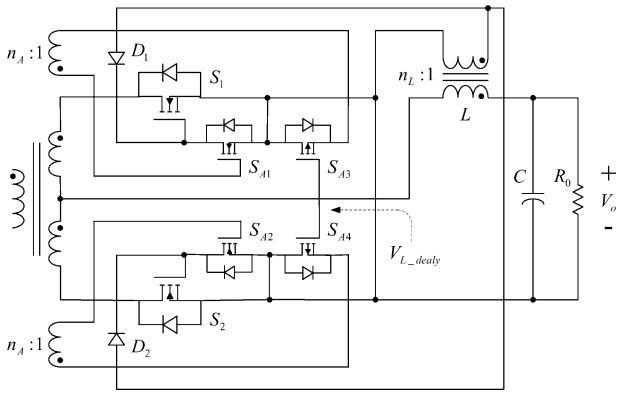

Fig. 6. Improved scheme utilizing the output inductor for SRs.

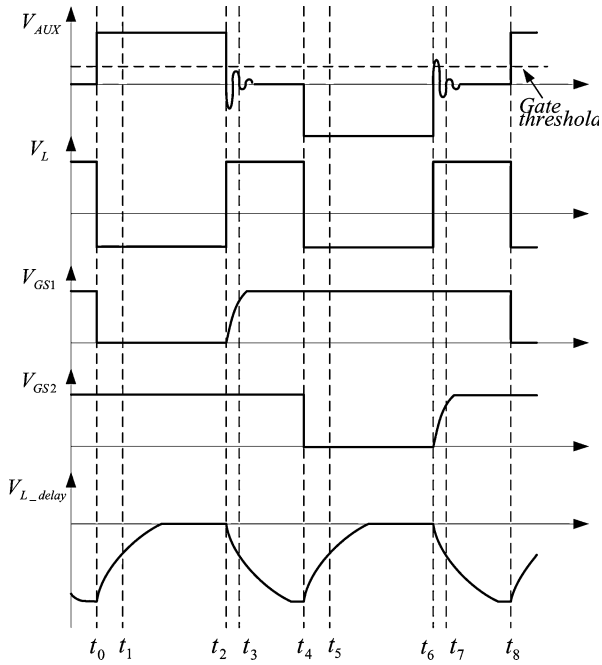

Fig. 7. Timing of the waveforms from the improved scheme.

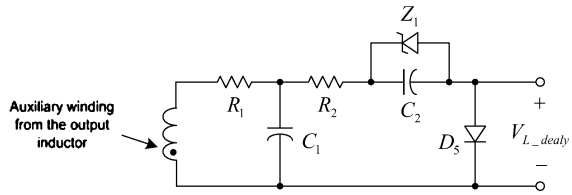

Fig. 8. Suggested circuit to generate the signal $V_{L\_\rm delay}$.

a delayed signal $(V_{L\_\rm delay})$ from an auxiliary winding of the inductor is applied to control S_{A3}.

Fig. 6. shows the proposed synchronous rectification method that is suitable for practical application. S_1 and S_2 are the MOSFETs used as synchronous rectifiers. S_{A1} and S_{A2} are the auxiliary switches (NMOS) used to discharge the gate of the MOSFET synchronous rectifier. The auxiliary switches (PMOS) S_{A3} and S_{A4} control the charge path of S_{A1} and S_{A2}. The diodes D_1 or D_2 provide the channels to charge the gate of the main switches. The timing of the waveforms is shown in Fig. 7. The gates of S_1 and S_2 are charged by the auxiliary winding of the inductor through D_1 or D_2 during the deadtime. Then the gate voltage is kept when the diodes are reverse-biased. When one auxiliary winding of the transformer has positive output, the auxiliary discharging switch (S_{A1} or S_{A2}) is turned on and discharges the gate of the main switch (S_1 or S_2). Thus, each SR is turned off in time. The main challenge is to prevent the voltage spike from triggering S_{A1} and S_{A2} without affecting the normal operation. The gate voltage of S_1 in Fig. 6 can be an example to describe the principle. During time interval $t_0 - t_1, V_{L\_\rm delay}$ still exceeds the gate threshold and keeps S_{A3} on. $V_{\rm AUX}$ turns on S_{A1} through S_{A3}. The main switch S_1 is turned off in time. At time $t_1, V_{L\_\rm delay}$ reaches the threshold and S_{A3} is turned off. The condition during $t_6 - t_7$ explains how to block the unexpected voltage spike. Since $V_{L\_\rm delay}$ is a delayed signal from the inductor, it takes time to reach the threshold and trigger S_{A3}. During this period, S_{A3} remains off and blocks the voltage from the auxiliary winding of the transformer. Therefore, S_{A1} is not influenced by the voltage spike and S_1 has no undesired gate voltage discharge. The same condition holds for the gate voltage of S_2.

Fig. 8. is a suggested circuit which can generate the demanded signal $V_{L\_\rm delay}$. The voltage from an auxiliary winding of the inductor goes through an RC filter, and is added to a negative voltage dc bias. The output is the produced signal that can be used to control S_{A3} and S_{A4}.

IV. Experimental Results

To verify the principle and wide range operation of the proposed scheme, a prototype is built by using conventional half-bridge topology switched at 150 kHz without soft switching. Both the original and improved schemes are applied in the prototype to obtain the comparison. The specifications are:

- $V_{\rm in}$: 36–75 V;
- V_o: 2.5 V;
- I_o: 30 A.

IRF7495 (100 V, 22 mΩ, SO-8) is used for the primary switches. Each synchronous rectifier (S_1 and S_2) uses three SI4320DYs (SO-8s) in parallel. SI4320DY has an on-resistance of 3 mΩ. E18 magnetic core is used for both the power transformer and output inductor. The cross-sectioned area of the magnetic core is 39.5 mm^2. The power transformer has 5 turns for the primary winding and 1 turn for the secondary winding.

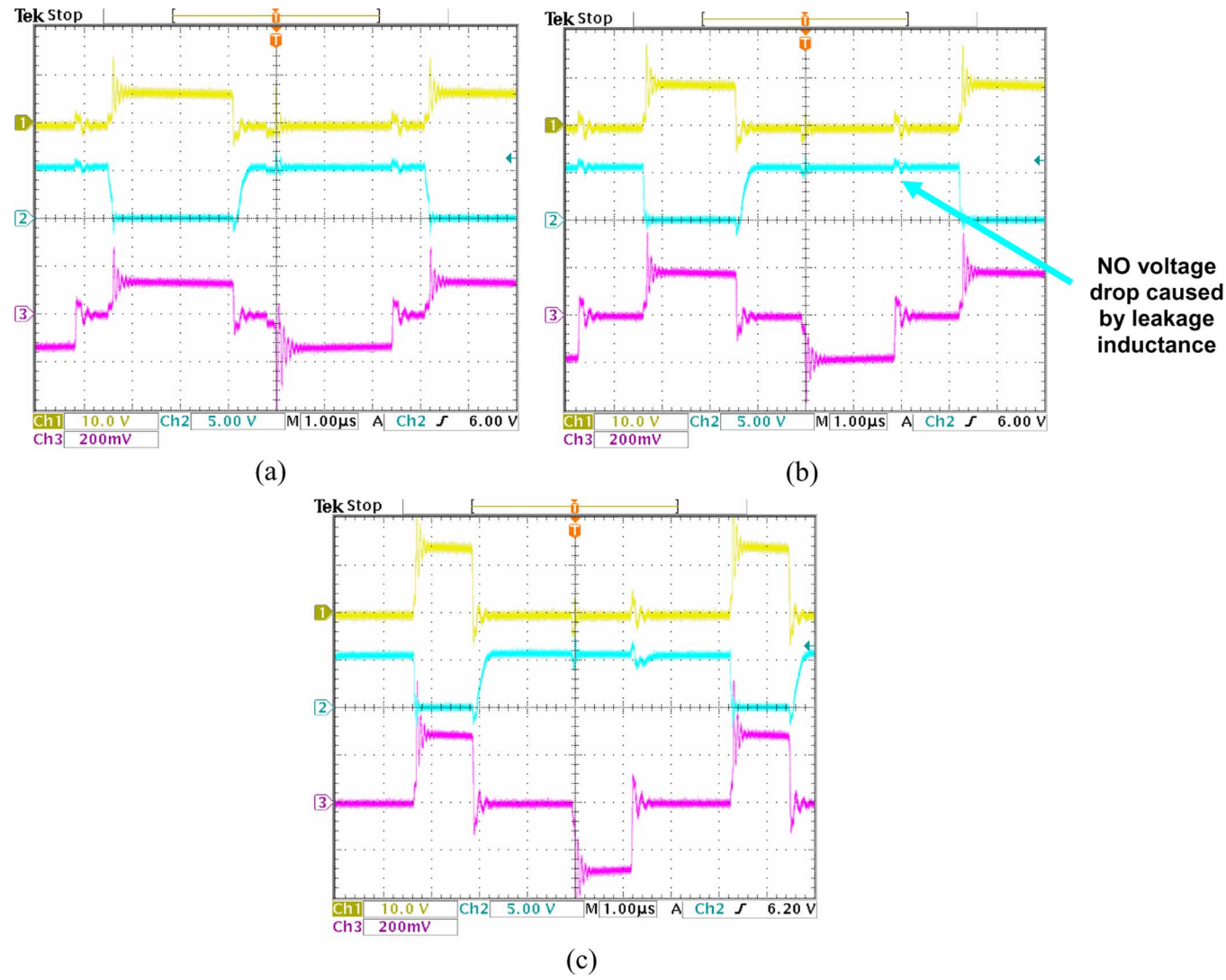

Fig. 9. Waveforms of Vds (Channel 1, 10 V/div), Vgs (Channel 2, 5 V/div) of the SR (S1) and the voltage of the secondary winding (Channel 3, 10 V/div) when using the improved driving scheme. (a) Waveforms when Vin is 36 V, (b) Waveforms when Vin is 48 V, (c) Waveforms when Vin is 75 V.

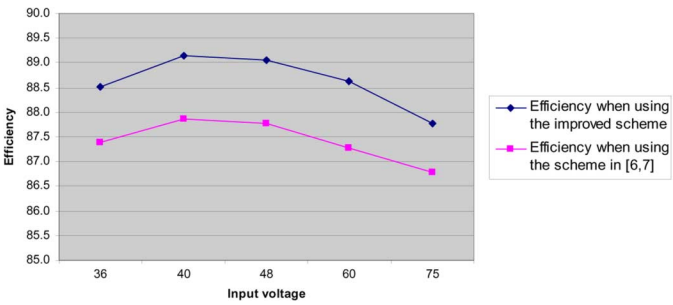

Fig. 10. Efficiency comparison between the original and improved self-driven scheme.

TABLE I
EFFICIENCY IMPROVEMENT AFTER USING THE NEW SCHEME

Vin	Efficiency improvement	Difference
36V	87.4% → 88.5%	1.1%
40V	87.9% → 89.2%	1.3%
48V	87.8% → 89.1%	1.3%
60V	87.3% → 88.7%	1.4%
75V	86.8% → 87.8%	1.0%

Fig. 9. shows the waveforms of the SR (S_1) and the secondary winding when using the proposed improved scheme. Channel 1 and Channel 2 show the drain-source and gate-source driving voltage, respectively, of S_1. Channel 3 represents the output voltage of the transformer. The waveforms are obtained when the transformer is not so tightly coupled. From the figure, the undesired short-time gate-voltage discharge has already been removed. It can be clearly seen that gate retention is fulfilled during the entire operation period.

By applying the proposed self-driven scheme to the conventional half-bridge, an efficiency of 89.1% at 48 V input and 2.5 V–30 A output is obtained. Fig. 10 shows the efficiency curves under different input voltages at full load for both the original and improved self-driven scheme. Also, efficiency improvements after using the new scheme are shown in Table I. The improvements are 1.3% at 48 V input.

V. Conclusion

Utilizing the signal from the output inductor and transformer to fulfill gate charge and retention is helpful for wide-input-voltage-range converters with symmetrically driven transformers. One open challenge, which was seriously preventing this method from obtaining high efficiency, is the undesired gate-voltage discharge problem caused by the leakage inductance. This paper proposes a new, improved scheme to avoid the short-period gate discharge. This method can achieve substantial efficiency improvements and is suitable for practical application. The experimental results verify the principle and performance of the new scheme.

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