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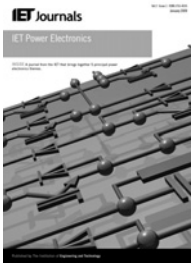

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Buck/half-bridge input-series two-stage converter

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Abstract: This study presents a concept of connecting two-stage DC–DC converters in an input-series connection. An application example is discussed in detail where the first stage utilises two series connected buck converters that have reduced voltage stress. A single second stage is a half-bridge converter and is able to regulate the charge balance of the first stage. The benefits of the topology include: reduced primary switch voltage stress, simple self-driven synchronous rectification for wide input voltage range, self-voltage balancing on intermediate bus capacitors and simple housekeeping power supply. Further, the topology exhibits an unusual ripple match concept that can be utilised to suppress the current ripple of the second stage. Based on the detailed analysis, prototypes with 500–700 V input and 5 V/30 A output are built. Experimental results verify the principle and performance of the new topology.

1 Introduction

Although a formal framework for connecting the inputs in DC–DC converters in series was presented in the early 1990s [1, 2], it is only recently that widespread applications are being seen of these topologies [3–12]. When using an input-series connection, a high-voltage input can be shared among different power supplies, thereby reducing voltage stress on the input switches. For example, in [3] input-series connection for an electric train with a 700 V DC bus is used to reduce the switch stress on series connected full-bridge converters, thereby allowing the replacement of the IGBTs with MOSFETs. This had the benefit of permitting higher switching frequency to reduce magnetic size, as well as improve power efficiency. Similar benefits are noted in series ('stacked') connections in electric trains in [9]. Other high-voltage bus applications that benefit from input-series and output-parallel connections include converters utilised in hybrid-electric vehicles (~300–600 V DC bus) [10, 11], a second step-down DC–DC converter (for traditional AC/DC converter) that is connected with single-phase power factor correction (PFC) (~400 V DC bus) or three-phase PFC (~800 V DC bus).

Of course, conventional topologies, such as zero voltage switching (ZVS) phase-shifted full bridge [13, 14] are favourable when the voltage stress is not too high, because of their high efficiency and lower part count. However, it is often desirable to have voltage stresses of the main switches to be less than or equal to half of the input voltage, which cannot be achieved by such topologies. Further, there has been intriguing discovery that the input-series connections [12] lead to reduction of total MOSFET switch losses, particularly in Class E converters. This is primarily because of the fact that the $R_{on}C_{oss}$ figure of merit is proportional to non-linear term $(V_{BR})^{4/3}$, where V_{BR} is the substantially reduced blocking voltage of the individual MOSFET. The benefit of the series input is that as breakdown voltage decreases, C_{oss} gets bigger for a given die area, but Ron gets smaller faster than C_{oss} gets bigger. In fact, this has led to the utilisation of input-series connections in very high frequency (VHF) converters at the 30–300 MHz band.

The purpose of this paper is to explore a new topology of input series and self-balanced DC–DC converters. Our original motivation was for the development of a $V_{in} = 600$ V, $V_{out} = 28$ V, 100 W driver for IGBT inside an electric vehicle, such as those being investigated by the US Army [10, 11]. Our approach is to combine the ideas of input-series output-parallel converters with two-stage converters [15–20]. At the same time, we borrow concepts from multi-level DC–DC converters and inverters to solve

the capacitor self-balancing voltage problem for input-series connections. That is, whenever the inputs of two converters are connected in series, their input capacitors may have voltage imbalances that may lead to transformer saturation, increased losses because of ringing and difficult control regulation [3, 12, 21–24]. To achieve voltage balancing, both active and passive balancing circuits are often added, unless the specific topology has self-balancing properties [22], which we claim for our proposed topology. Some other interesting performance features of the topology include:

- *Lower switch stress:* When two buck circuits are connected in series for the first stage, the voltage stress is reduced to half of the input voltage. The voltage stress of the switches in the second stage is also lower than half of the input voltage when the duty ratio of each buck is below 50%. Thus, the approach maintains the advantages of traditional input-series (or 'stacked') output-parallel converters [1–12].

- *Output-inductorless half-bridge can be utilised for the second stage:* As in traditional two-stage converters, this leads to the benefits of reduced board space, simple self-driven synchronous rectifier (SR) driving for wide input voltage range and simple design of housekeeping power supply [15–20].

- *No charge balance consideration is needed since the second stage can regulate the balance:* This eliminates the need for auxiliary charge balance circuits for multilevel circuits [21–24].

- *The voltage ripple across the intermediate capacitors can be reduced because synchronised operation of the two stages:* Reducing output capacitors and size of the magnetic cores is beneficial for the cost and volume reduction of high-density power supplies. By synchronising the switching of the two stages, the voltage ripple across the intermediate capacitors can be decreased, which leads to reduced current and voltage ripple of the second stage. This is a novel property of the proposed topology, and as a result, the output capacitor and size of the magnetic cores is reduced accordingly. The voltage ripple across the intermediate capacitors can be significantly suppressed with proper discontinuous mode operation, which is analysed in Section 3 and verified in Section 4.

Of course, a primary disadvantage of input-series output-parallel and/or two-stage DC–DC converters is their increased switch component count and their complexity compared to conventional topologies for high-input voltage application. So, there are design trade-offs to be considered.

1.1 Relation of proposed topology to existing state of the art

1.1.1 Background of input-series and multi-level DC–DC converters:

Fig. 1*a* shows the conventional concept of input-series output-parallel scheme [1–12] that can reduce the voltage stress. Fig. 1*b* shows an example using two half-bridge circuits. As shown in Fig. 1, the converters are connected in series on the primary side. As with the topology proposed in this paper, both input-series converters have an input voltage of $V_{in}/2$. Meanwhile, paralleling the secondary side is beneficial for low-output voltage and high-output current. However, there are also technical drawbacks for the circuit in Fig. 1*b* that do not appear in our proposed topology in Figs. 2 and 3, which is shown in Section 2. (This circuit in Fig. 1*b* is mentioned because it represents a fair comparison to one implementation of the new topologies proposed.) First, each of the two stacked converters has one inductor and one transformer. These total four magnetic cores take up significant board space. Further, when the input voltage has wide range, efficient driving of the SRs becomes more difficult and higher voltage-rated MOSFETs are usually required. This leads to numerous challenges for fulfilling suitable self-driven SRs schemes as well as increases in the conduction power loss for SRs. The proposed circuit in Fig. 3 has only one transformer and this operates at 50% duty ratio, making self-driven SR simpler with reduced

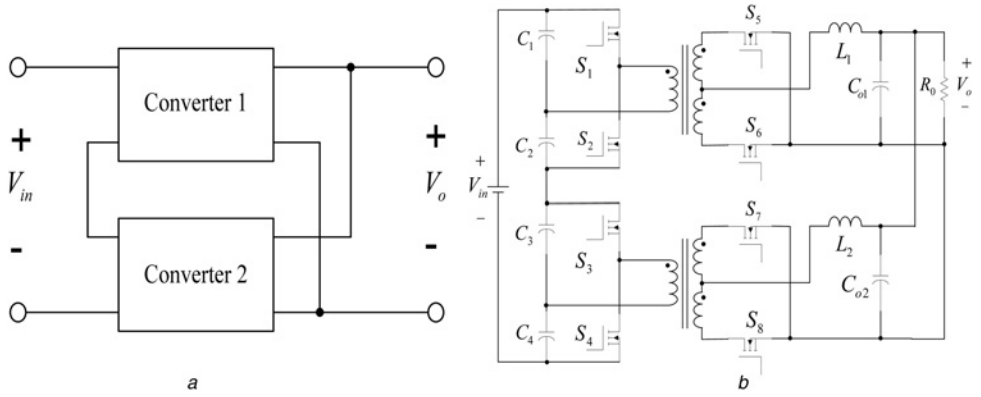

Figure 1 *Traditional input-series output-parallel scheme [1–12]*

a Simplified input-series output-parallel scheme
b Example of input-series output-parallel scheme

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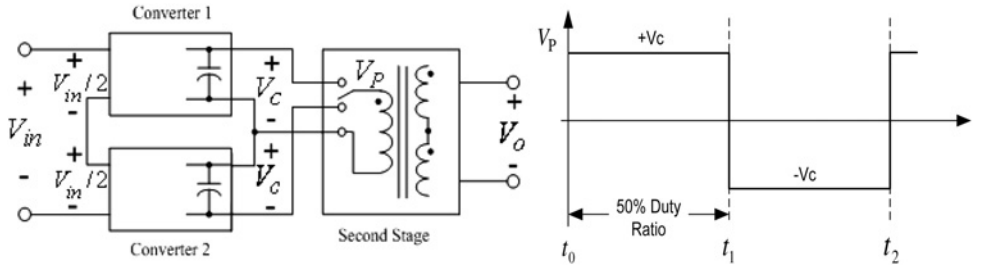

Figure 2 *General concept of the input-series output-parallel two-stage topology*

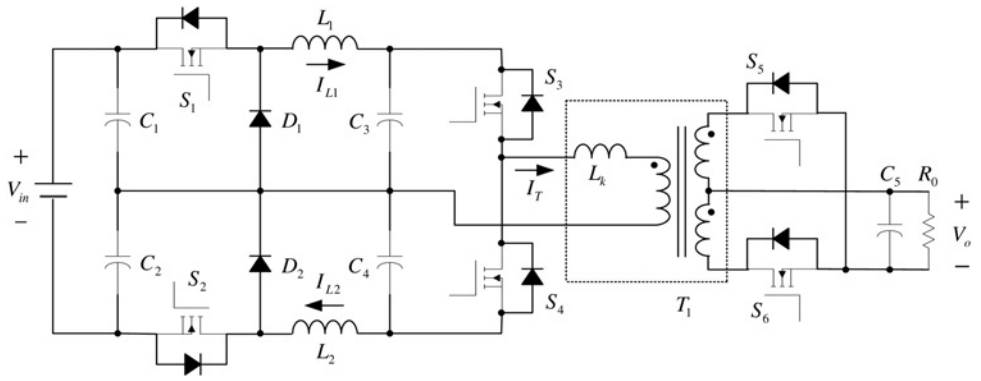

Figure 3 *Proposed input-series two-stage topology*

board space because of one less transformer and two fewer secondary side SRs.

The concept of multi-level converters is also peripherally related to the proposed topology [20–27]. Generally speaking, these topologies utilise switches and capacitors (in series) to reduce input voltage stress, but as noted in [20–24], there is normally a need for auxiliary capacitor charge balance equalisation circuits. Similarly, three-level buck converters are peripherally related to the first stage of Fig. 3 ([25–28], and references therein), which tend to utilise a single inductor and a single flying capacitor to achieve lower voltage stress. In either case, when three-level bucks or other multi-level circuits are used in a first stage of a two-stage converter, they do not exhibit the benefits of the capacitor charge balance or unique intermediate capacitor ripple cancellation features described in Section 3 [24].

1.1.2 Background of two-stage DC–DC converters: This research proposes to make input-series output-parallel concepts for two-stage converters. It is well documented that two-stage DC–DC converters have benefits that include [15–20]: (i) Fixed duty cycle operation of the second stage helps to improve the performance of the synchronous rectifiers (SRs). The voltage and current stress of the SRs are reduced when the input voltage range is wider. Also, it is convenient to directly obtain the driving signal from the transformer to turn on the SRs during the entire operation period. This is because a traditional two-stage low-voltage converter utilises a buck circuit in the first stage to regulate the output. The second stage uses an isolated topology as a 'DC transformer' [19] to drop the output voltage of the buck. The second stage operates with a fixed duty ratio, such as 50% for half-bridge, and the driving signals for the SRs can be directly taken from the secondary transformer, reducing complexity and cost of control-driven SRs [15–20]. (This is, perhaps, one of the main reasons that two-stage converters have become widespread in telecommunication power supplies [20].) (Two-stage converters are not to be confused with 'two-stage architectures' that cascade two separately operating and independent DC/DC converters together, each having separate control loops, control pwm hardware, EMI filters etc. Two-stage converters have single pwm controller with one duty ratio.)

For two-stage converters, another important benefit is that the second stage relies only on an external small inductor or just the leakage inductor to suppress the current ripple, because of the 50% duty ratio operation. For example, output-inductorless half-bridge with 50% duty can be utilised in the second stage to minimise the output inductor and fasten the response speed [19, 20]. The drawback is that even small voltage variations on the intermediate capacitors can lead to a noticeable current ripple. The ripple current subsequently leads to more conduction loss and forces the designer to select a high-capacitance value for the output. Therefore reducing the voltage ripple on the intermediate capacitors is beneficial for the performance of the two-stage converter. The

proposed topology in Fig. 3 maintains the benefits of two-stage converters but also has lower voltage ripple because of the ripple cancellation benefits discussed in Section 3.

Finally, it is important to mention that neither traditional input-series output-parallel converters nor two-stage converters necessarily claim improved power efficiency over traditional topologies, such as full bridge. Further, there is increased component count because of more switches. Thus, there are design trade-offs to consider when using all these topologies. The benefits of reduced input voltage stress with self-driven SR for wide and high-input voltage range seem to be the important application area for Fig. 3.

2 Operation principles and design

2.1 General principle

Fig. 2 describes the concept of the proposed input-series two-stage topology. Any two non-isolated converters (buck, boost, buck–boost etc.) are input-series connected for the first stage to regulate the output voltage, shown in the figure as Converter 1 and Converter 2 (each with the same duty ratio). Because of the input-series connection, each non-isolated converter in the first stage shares half of the input voltage. Therefore lower voltage stress is achieved. Interleaved operation is used for the first stage, and voltage ripple on the intermediate capacitors can be reduced, as discussed in Section 3.

A symmetrically driven transformer is utilised for the second stage operating at 50% duty ratio, as shown in Fig. 1. V_c is the voltage across the intermediate capacitors in Fig. 1. The candidate topologies of the second stage typically have two input capacitors connected in series, such as half-bridge or dual input-series output-parallel. Each intermediate capacitor is connected to the primary winding of the transformer for 50% of the time, that is the primary transformer voltage, V_p, is equal to $+V_c$ 50% of the time and $-V_c$ the other 50% of the time. As a result, the voltage balance of the two intermediate capacitors can be automatically regulated by the magnetising inductance of the transformer because of voltage-second balance of the inductor. This is a benefit of the proposed approach over most multi-level switching converters. As noted in [21–24], most multi-level topologies require external circuitry to balance intermediate capacitor voltages. Further, there are also additional documented benefits (from two-stage converters [17–20]) of transformer waveforms that we further discuss in Section 4.

2.2 Specific series buck + half-bridge implementation

For the purpose of illustration, we now focus on one specific implementation of the concept, as shown in Fig. 3. Fig. 4 illustrates the circuit's related waveforms. V_{gs1}, V_{gs2}, V_{gs3} and V_{gs4} are the driving signals for the switches on the primary side. As can be seen in the figure, the first stage contains

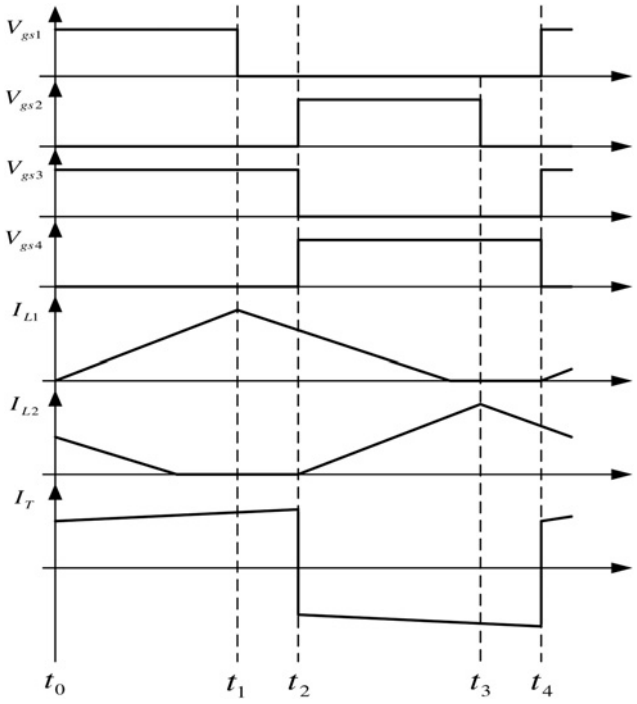

Figure 4 *Waveforms of the proposed topology*

dual interleaved buck converters. One channel consists of C_1, C_3, S_1, D_1 and L_1; the other consists of C_2, C_4, S_2, D_2 and L_2. The intermediate capacitors (C_3 and C_4) supply the dual outputs of the first stage, which for this topology will have self-regulating charge balance. The second stage is an isolated output-inductorless half-bridge, which consists of C_3, C_4, S_3, S_4, T_1, S_5, S_6 and L_k, with fixed operation (50% duty ratio). L_k can be an external small inductor or just the leakage inductance of the transformer.

The purpose of using output-inductorless half-bridge is to reduce the converter's size as well as improve the response of the converter. Since the primary switches of the second stage operate complementarily, by utilising the energy stored in the leakage inductance (or adding small external inductance), zero-voltage turn-on can be realised for S_3 and S_4. Fixed duty ratio helps to achieve high efficiency for SRs (S_5 and S_6). It is convenient to directly obtain the driving signal from the transformer to turn on the SRs during the entire operation period as traditional two-stage circuit does. Also, taking the advantage of the half-bridge circuit, the second stage keeps the charge balance of the dual intermediate capacitors. As a result, charge balance of C_1 and C_2 are also maintained. Interval t_0–t_4 is defined as the switching period T. The lengths of t_0-t_1 and t_2-t_3 are defined as DT, which represents the duty ratio, and thus, the duty ratio D will always be less than one-half.

For the purpose of reducing the voltage ripple across the intermediate capacitors, the first stage operates at discontinuous mode. As a result, S_1 and S_2 have zero-current turn-on. Fig. 5 shows different operation modes of the circuit during different periods in one switching cycle.

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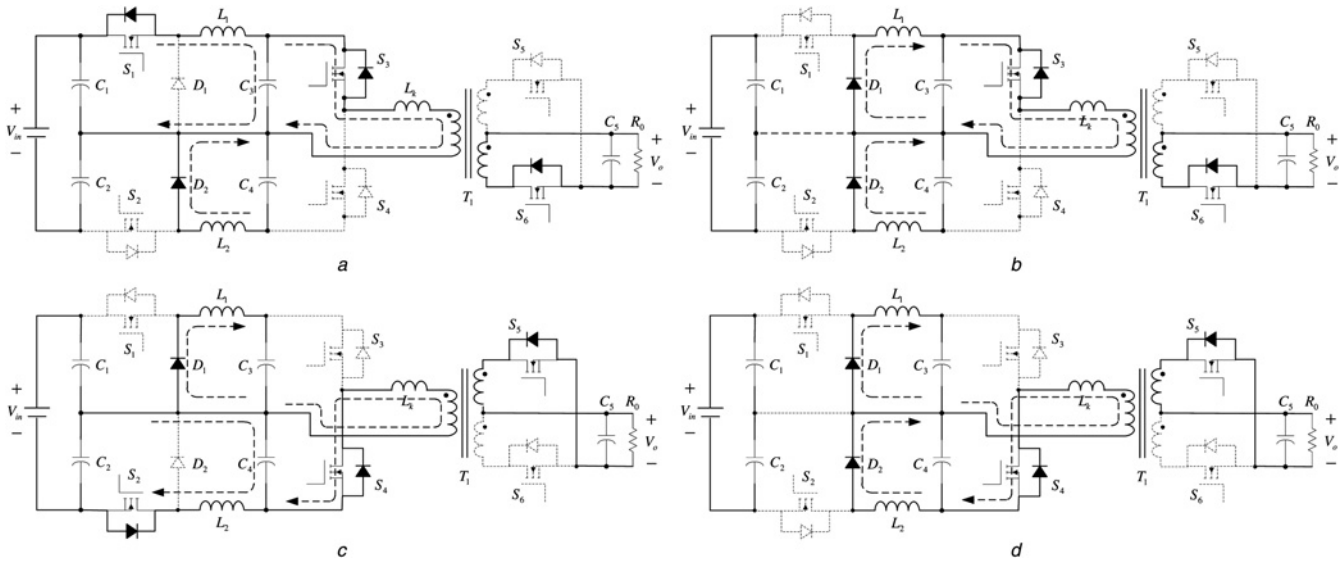

Figure 5 *Detailed description of the operation principle of the proposed topology*

a Interval 1 (t_0–t_1)
b Interval 2 (t_1–t_2)
c Interval 3 (t_2–t_3)
d Interval 4 (t_3–t_4)

For the convenience of description, the short transition time of the second stage is not included. Obviously, ZVS for S_3 and S_4 can be fulfilled during the transition time just as traditional circuits [15–20]. The following description explains the detailed operation principle of this topology.

The length of t_0–t_1 and t_2–t_3 are defined as DT, where D represents the duty ratio.

Interval 1 (t_0–t_1): The condition of this period is shown in Fig. 5*a*. In this interval, S_1 is turned on. The upper buck circuit transfers energy from C_1 to C_3 through L_1. The charging current I_{L1}, which is shown in Fig. 5, increases linearly according to $L_1(\mathrm{d}I_{L1}/\mathrm{d}t) = (V_{\mathrm{in}}/2) - V_1$. ($V_1$ is the voltage across the intermediate capacitors.) At the same time, the current of the bottom buck circuit, which is I_{L2}, flows through the freewheeling diode D_2 and charges C_4. The current decreases according to $L_2(\mathrm{d}I_{L2}/\mathrm{d}t) = -V_1$ until zero during this interval. For the second stage, S_3 is turned on. The transformer current I_{T} flows through S_3. The intermediate capacitor C_3 transfers power, the load through the transformer and S_6.

Interval 2 (t_1–t_2): As shown in Fig. 5*b*, S_1 is turned off during this interval. Therefore current I_{L1} goes through the freewheeling diode D_1 and starts to decrease linearly according to $L_1(\mathrm{d}I_{L1}/\mathrm{d}t) = -V_1$, which is shown in Fig. 8. Also, the current of the bottom buck is zero because of the discontinuous mode operation. The second stage still transfers energy from C_3 to the load through the transformer and S_6.

Interval 3 (t_2–t_3): The condition of this interval, which is shown in Fig. 5*c*, is similar to interval 1. The two buck circuits switch the conditions. During this interval, S_2 is turned on. The bottom buck transfers energy from C_2 to C_4 through L_2. Its output current, which is I_{L2}, starts to increase linearly according to $L_2(\mathrm{d}I_{L2}/\mathrm{d}t) = (V_{\mathrm{in}}/2) - V_1$ through S_2 and L_2. Also, the current of the upper buck, which is I_{L1}, still flows through the freewheeling diode and decreases linearly according to $L_1(\mathrm{d}I_{L1}/\mathrm{d}t) = -V_1$ until zero. In this case, S_3 is turned off. The transformer current I_{T} flows through S_4. The power is transferred from C_4 to the secondary side through transformer and S_5.

Interval 4 (t_3–t_4): Fig. 5*d* shows the condition of the last interval. In this case, S_2 is turned off. I_{L2} transfers to the freewheeling diode and decreases linearly. The current of the upper buck is zero because discontinuous mode operation. Current I_{T} still circulates through S_4. The second stage continues transferring energy from C_4 to the secondary side through transformer and S_5.

The first stage buck converters operate in discontinuous conduction mode. Thus, their duty ratios are given as

$$D = \sqrt{\frac{2L(I_{\mathrm{d}}/2)V_1}{(V_{\mathrm{in}}/2)(V_{\mathrm{in}}/2 - V_1)T}}$$

[16], where $I_{\mathrm{d}} = (n_{\mathrm{s}}/n_{\mathrm{p}})I_{\mathrm{out}}$; n_{p} and n_{s} are the turn number of the primary and secondary windings. Ignoring the short transition time, the duty ratio of the entire proposed two-stage topology is

$$D = \sqrt{\frac{4L\,I_{\mathrm{out}}\,V_{\mathrm{o}}}{V_{\mathrm{in}}[V_{\mathrm{in}} - 2V_{\mathrm{o}}(n_{\mathrm{p}}/n_{\mathrm{s}})]T}}$$

The non-linear relation between duty ratio and output voltage indicates that control design will be more complicated. In fact, the difficulty of modelling and controlling two-stage converters is demonstrated in [19, 20] and robust controller design for circuits in Figs. 2 and 3 is an open research topic.

3 Ripple match design

An interesting and unique aspect of two-stage stacked converters is that it is possible to synchronise the two first stage converters to suppress the voltage ripple of the second stage. This cannot be achieved by using previously reported topologies [1–12] or multi-level two-stage converters [24], although there are benefits to the multi-level two-stage converters because the first stage may be simplified to a single inductor [23] in some cases. The major benefit of this is it enables lower output voltage ripple, even without output inductor in the second stage. Notice despite the fact that a two-stage concept is being used, this leads to one fewer magnetic core (reduced board space) compared to input-series output-parallel full bridge, forward or push–pull converters that each have four magnetic cores [3, 4].

Fig. 6 shows the charge and discharge condition of one intermediate capacitor (C_3) of the proposed converter in Fig. 3. The same condition occurs in the other capacitor (C_4). I_1 is the charging current from the first stage whose current ripple can be changed by adjusting the inductance value of L_1. I_2 is the discharge current that flows to the second stage. When S_3 is turned on, I_2 is equal to a DC value $I_d = (n_s/n_p)I_{out}$, where n_p and n_s are the turn number of the primary and secondary windings. When S_3 is off, I_2 is zero. Since S_3 is on for 50% of the time, I_2 is equal to I_d for half of the time. Since the averaged value of I_1 and I_2 are equal, the voltage ripple on the intermediate capacitor can be reduced if I_1 has higher current value when $I_2 = I_d$, but lower value when $I_2 = 0$.

Thus, because the two stages can be synchronised, regulating the current ripple has the effect of reducing the intermediate capacitor voltage ripple. Therefore to achieve an optimised current ripple that results in minimum voltage ripple, a proper inductance value should be chosen for the first stage. As derived below in Sections 3.1–3.4

$$L = \frac{1}{4}\frac{V_{in}/2 - V_c}{I_{d\,max}}\sqrt{\frac{2V_c}{V_{in}}}T$$

is an optimised inductance value, which can fulfil the above minimum voltage ripple condition for intermediate capacitor voltage such that

$$\Delta V_C \le \frac{I_{d\,max}}{2C}\sqrt{\frac{V_c}{V_{in}}}T$$

In fact, increasing the inductance value beyond this recommended value does not (surprisingly) help to further suppress the voltage ripple. In this case, the first stage operates at a discontinuous mode. Although discontinuous current increases the conduction loss of the first stage, the switching loss is greatly reduced, which is good for high-input voltage situation. The analysis is based on two assumptions:

- $V_C < \tilde{V}_i/2$, where V_C and $\tilde{V}_i$ are same as in Fig. 6.
- The current ripple of the second stage is not big, and its effect can be approximated by a square waveform (i.e. $I_{out} \simeq$ const.).

3.1 Continuous current mode for the first stage

One possible mode of operation is to operate both buck converters in continuous conduction mode. As shown in Fig. 7*a*, I_1 is the current through the inductor of the first stage, which represents the charging current for the intermediate capacitor. I_2 is the discharging current from the second stage. It discharges the capacitor for half of the duty cycle with a value I_d. The charge on the intermediate capacitor increases when $I_1 > I_2$, but decreases when $I_1 < I_2$. Therefore Area I and Area II in Fig. 6*a* represent the amount of charge variation on the capacitor defined as ΔQ_1 and ΔQ_2, respectively. Thus

$$\Delta Q_1 = \Delta Q_2 = \int_{T/2}^{T} I_1 \mathrm{d}t = \left[\frac{I_d}{2} - \frac{V_c}{2L}(1-D)T + \frac{V_c}{L}\frac{T}{4}\right]\frac{T}{2}$$
$$= \left[I_d - \frac{V_c}{L}\left(\frac{1}{2} - D\right)T\right]\frac{T}{4} \quad (1)$$

where we also remember the relation between capacitor ripple voltage and charge variation $\Delta V_C = \Delta Q_1/C$. From (1), charge variation decreases when L decreases. (L is the inductance of the buck.) Therefore for continuous mode, the voltage ripple keeps decreasing as L decreases until the first stage reaches discontinuous current mode.

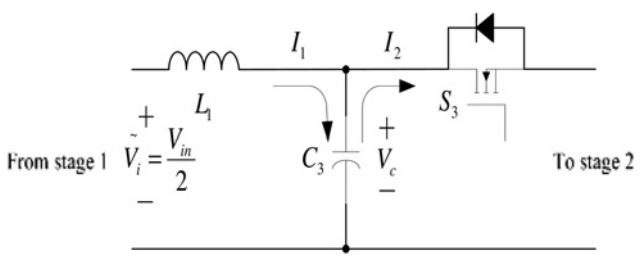

Figure 6 *Simplified diagram showing the charge and discharge condition of the intermediate capacitor*

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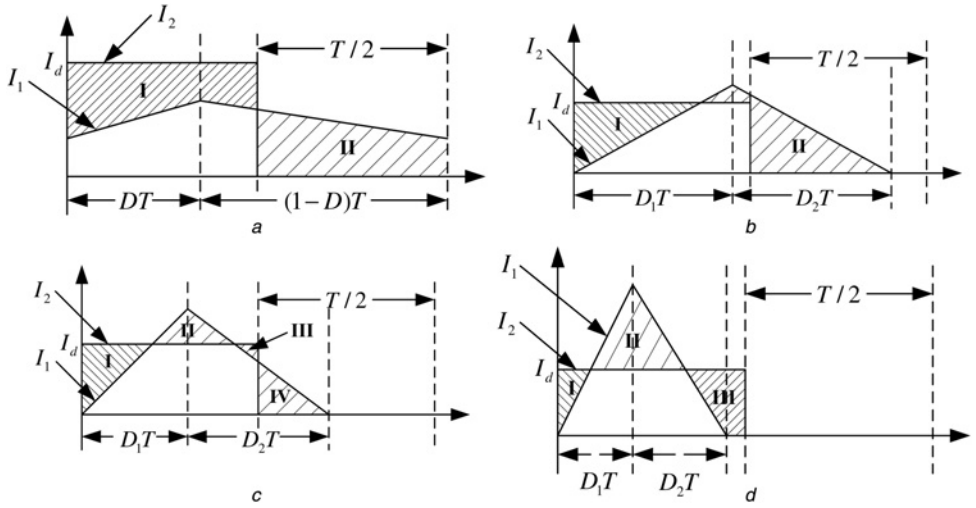

Figure 7 *Currents from the circuit in Fig. 6*

a Continuous current mode for first stage
b Discontinuous current mode I for the first stage
c Discontinuous current mode II for the first stage
d Discontinuous current mode III for the first stage

3.2 Discontinuous current mode I for the first stage

Fig. 7*b* shows the discontinuous current mode I. In this case $I_1 > I_2$ at $t = T/2$. Similar to the continuous current mode, the charge variation is

$$\Delta Q_1 = \Delta Q_2 = \frac{LI_{\mathrm{d}}}{\tilde{V}_{\mathrm{i}} - V_c}\frac{I_{\mathrm{d}}}{2} = \frac{LI_{\mathrm{d}}^2}{2(\tilde{V}_{\mathrm{i}} - V_{\mathrm{c}})} \tag{2}$$

where $\tilde{V}_{\mathrm{i}} = V_{\mathrm{in}}/2$ is the input voltage to the buck converter. From (2), the voltage ripple still keeps decreasing with the decreasing of L until the first stage reaches discontinuous current mode II. Thus, lower voltage ripple is obtained in this mode when compared with continuous current mode.

3.3 Discontinuous current mode II for the first stage

Fig. 7*c* shows the discontinuous current mode II. In this case, Area I or Area II determines the maximum charge variation in one duty cycle. By computing the charge variation separately, the following equations are obtained

$$\Delta Q_1 = \frac{LI_{\mathrm{d}}}{\tilde{V}_{\mathrm{i}} - V_{\mathrm{c}}}\frac{I_{\mathrm{d}}}{2} = \frac{LI_{\mathrm{d}}^2}{2(\tilde{V}_{\mathrm{i}} - V_{\mathrm{c}})} \tag{3}$$

$$\begin{aligned}\Delta Q_2 &= \frac{1/(D_1+D_2)-1}{1/(D_1+D_2)}(D_1+D_2)T\frac{1}{2}\left(\frac{I_{\mathrm{d}}}{D_1+D_2} - I_{\mathrm{d}}\right)\\ &= \frac{1}{2}(1-D_1-D_2)^2 I_{\mathrm{d}}T\end{aligned} \tag{4}$$

From the above equations, ΔQ_1 decreases with the decreasing of L, whereas ΔQ_2 increase when L decreases. Therefore minimal voltage ripple is obtained when $\Delta Q_1 = \Delta Q_2$. At that time, $\Delta Q_3 = \Delta Q_4$. Since

$$\frac{D_1}{D_1 + D_2} = \frac{V_{\mathrm{c}}}{\tilde{V}_{\mathrm{i}}} \tag{5}$$

$$\frac{\tilde{V}_{\mathrm{i}} - V_{\mathrm{c}}}{L}D_1T = \frac{I_{\mathrm{d}}}{D_1 + D_2} \tag{6}$$

The value of L can be represented as

$$L = \frac{\tilde{V}_{\mathrm{i}} - V_{\mathrm{c}}}{I_{\mathrm{d}}}D_1(D_1 + D_2)T \tag{7}$$

Combining (3), (4) and (7), let $\Delta Q_1 = \Delta Q_2$, minimal voltage ripple is realised when

$$D_1(D_1 + D_2) = (1 - D_1 - D_2)^2 \tag{8}$$

3.4 Discontinuous current mode III for the first stage

Also, the discontinuous current mode III, which is shown in Fig. 7*d*, is checked. This time, Area II determines the maximum charge variation in one duty cycle. Similar to the discontinuous current mode II, the value of ΔQ_2 can be obtained from (4). ΔQ_2 decreases when L increases. Thus, this mode has higher voltage ripple than discontinuous current mode II has.

3.4.1 Derivation of optimal inductance value:

Based on the above analysis, for a constant input voltage and load current, the minimal intermediate voltage ripple can be obtained when the converter operates in discontinuous mode II and (8) is satisfied.

If only considering the full load condition, the value of L can be obtained by combining (5)–(7)

$$L_{\text{opt}} = \frac{\tilde{V}_{\text{i}} V_{\text{c}}}{(\tilde{V}_{\text{i}} - V_{\text{c}}) I_{\text{d max}}} \left(1 - \sqrt{\frac{V_{\text{c}}}{\tilde{V}_{\text{i}}}}\right)^2 T \tag{9}$$

where $\tilde{V}_{\text{i}} = V_{\text{in}}/2$. But considering the total load range (9) is not the inductance value for minimal ripple.

For a constant L, ΔQ_1 has the maximum value at full load by using (3). At that time

$$\Delta Q_{1\,\text{max}} = \frac{L I_{\text{d max}}^2}{2(\tilde{V}_{\text{i}} - V_{\text{c}})} \tag{10}$$

On the other hand, ΔQ_2 does not obtain maximum value at full load. By combining (4)–(6)

$$\Delta Q_2 = \frac{1}{2} \frac{(\tilde{V}_{\text{i}} - V_{\text{c}}) V_{\text{c}}}{\tilde{V}_{\text{i}} L} (1 - D_1 - D_2)^2 (D_1 + D_2)^2 T \tag{11}$$

Thus, the maximal Q_2 happens when $D_1 + D_2 = (1/2)$

$$\Delta Q_{2\,\text{max}} = \frac{1}{32} \frac{(\tilde{V}_{\text{i}} - V_{\text{c}}) V_{\text{c}}}{\tilde{V}_{\text{i}} L} T^2 \tag{12}$$

Since the increasing of L results in the increasing of $\Delta Q_{1\,\text{max}}$ and the decreasing of $\Delta Q_{2\,\text{max}}$, minimal voltage ripple occurs when $\Delta Q_{1\,\text{max}} = \Delta Q_{2\,\text{max}}$. Thus, the optimised inductance value is achieved for a total load range

$$L_{\text{opt}} = \frac{1}{4} \frac{\tilde{V}_{\text{i}} - V_{\text{c}}}{I_{\text{d max}}} \sqrt{\frac{V_{\text{c}}}{\tilde{V}_{\text{i}}}} T \tag{13}$$

If the input voltage V_{in} has a variation range, the value of L should be chosen based on the condition of different V_{in}. A simple consideration is to determine L when V_{in} is in the mid-point or perhaps on the nominal input voltage conduction. The implication of using (13) is that the voltage ripple on the intermediate capacitors can be significantly reduced. This also leads to the significant reduction of the current ripple on the second stage. As a result, the size for the output filtering inductor is minimised and the transient response is improved. Specifically, substituting (13) into (10) and using the fact that $C \cdot V = Q$ leads to the capacitor voltage ripple

$$\Delta V_{\text{C}} \le \frac{I_{\text{d max}}}{2C} \cdot \frac{\sqrt{V_{\text{c}}}}{V_{\text{in}}} \cdot T$$

4 Experimental results

To verify the principle of the proposed topology, a prototype is built with the following specifications: V_{in}: 500–700 V; output voltage V_{o}: 5 V; output current I_{o}: 30 A; switching frequency: 150 kHz. STD5NK50ZT4 (500 V, 4.4 A, DPAK) is used for the first stage switches (S_1 and S_2). STD5NM50T4 (500 V, 7.5 A, DPAK) is used for the second stage switches (S_3 and S_4). Note that the voltage ratings of all these primary switches are lower than the 700 V maximum input voltage, which illustrates the benefits of the lower voltage stress in this topology. Each synchronous rectifier (S_5 and S_6) uses two STS25NH3LL (SO-8) in parallel. STS25NH3LL has an on-resistance of 3.2 mΩ. Two E18 magnetic cores are used for the first stage inductors and E22 is utilised for the second stage power transformer. The cross areas of E18 and E22 are 39.5 and 78.5 mm^2. The power transformers have 20 turns for the primary winding, 1 turn for the secondary winding. (No output inductor is used for the second stage.)

Fig. 8 shows the waveforms of the primary side. Channel 1 shows the drain–source voltages of the first stage switches (S_1 and S_2). Channel 2 represents the drain–source voltages of

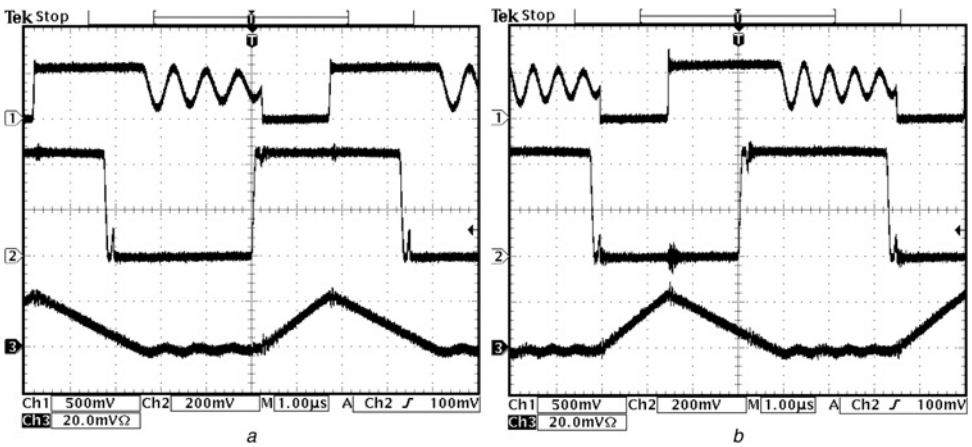

Figure 8 *Waveforms of V_{ds} (Channel 1, 250 V/div in the Y-axis) and the inductor current (Channel 3, 2 A/div in the Y-axis) of the first stage and V_{ds} (Channel 2, 100 V/div in the Y-axis) of the second stage*

a Waveforms of the upper buck when V_{in} is 600 V
b Waveforms of the under buck when V_{in} is 600 V

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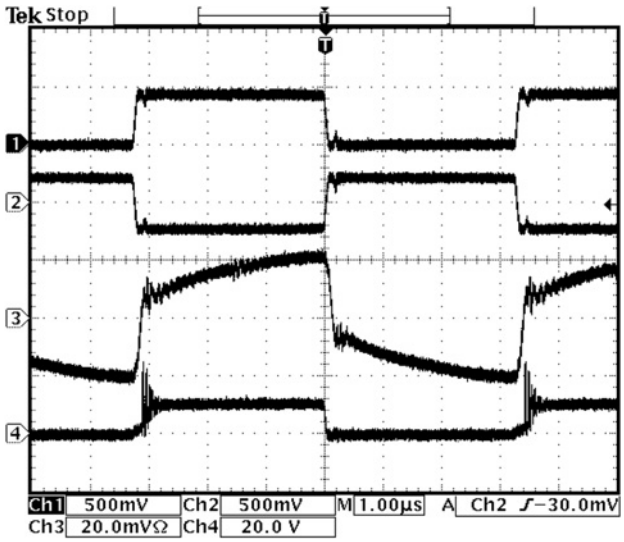

Figure 9 *Waveforms of V_{ds} (Channel 1, 250 V/div in the Y-axis), V_p (Channel 2, 250 V/div in the Y-axis) and the primary current I_p (Channel 3, 2 A/div in the Y-axis) of the second stage and V_{ds} (Channel 4, 20 V/div in the Y-axis) of the secondary SR (V_{in} is 600 V)*

the second stage switch (S_4). Channel 3 shows the current (I_1 or I_2) flowing through the first stage inductor. As designed and seen in Fig. 8, the first stage has discontinuous inductor current at full load. As previously explained, this both reduces the size of the inductor and the switching power loss. By choosing the optimal inductance value derived as (13), the voltage ripple on the intermediate capacitor can be reduced. Also, it can be clearly seen that the drain–source voltages of S_3 and S_4 drop to zero before the currents start to increase. Therefore zero-voltage turn-on is fulfilled for the second stage switches (S_3 and S_4). Fig. 9 shows the drain–source voltages of the second stage switch (S_4), the voltage across the primary winding of the transformer, the current through the primary winding of the transformer and the drain–source voltage of the secondary synchronous rectifier (S_5). The current ripple of the second stage is suppressed to a reasonable value although only leakage inductor of the transformer is utilised for filtering.

We will now experimentally demonstrate the benefits of operating the converter in discontinuous mode II, as theoretically demonstrated in Section 3 for the ripple match

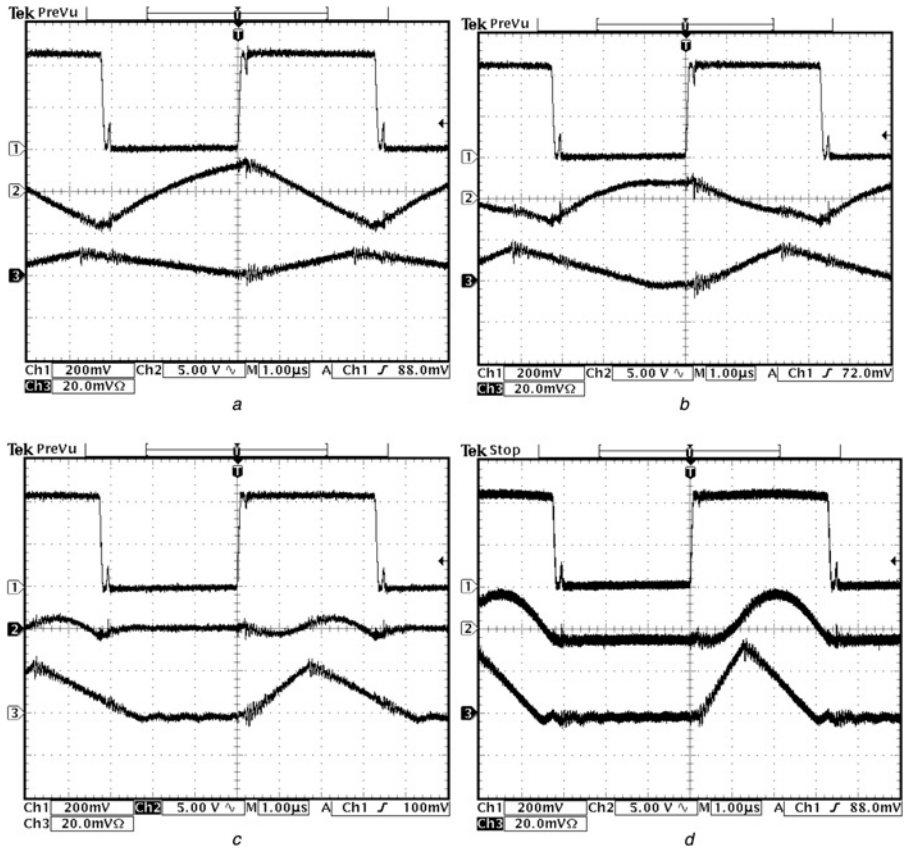

Figure 10 *Waveforms of V_{ds} (Channel 1, 100 V/div in the Y-axis) of the second stage, voltage ripple on the intermediate capacitor C_3 (Channel 2, 5 V/div in the Y-axis) and the inductor current (Channel 3, 2 A/div in the Y-axis) of the first stage (V_{in} is 600 V)*

a Waveforms in continuous current mode
b Waveforms in discontinuous current mode I
c Waveforms in discontinuous current mode II
d Waveforms in discontinuous current mode III
Notice how the voltage ripples in Channel 2 are smaller in discontinuous current mode II

design. For the different modes of operation, Fig. 10 shows the drain–source voltages of the second stage switch (S_4), voltage ripple on the intermediate capacitor (C_3), the current through the primary winding of the transformer and the inductor current of the first stage. Fig. 10*c* shows the lowest ripple voltage across the intermediate capacitor compared to the three other modes. Using (13), an inductance value of 128 μH is obtained. In this experiment, the values of the inductors in the first stage are approximately: 450 μH for continuous current mode, 240 μH for discontinuous current mode I, 128 μH for discontinuous current mode II and 68 μH for discontinuous current mode III. By comparing the voltage ripple across the intermediate capacitor, it can be clearly seen that minimal voltage ripple is achieved in discontinuous current mode II. Specifically, even though continuous current mode inductor is 3.5 times the value as the 128 μH inductance for discontinuous current mode II, its capacitor peak-to-peak ripple voltage is more than three times as much (8 V against 2.5 V). In other words, for this example, it would take over three times the inductance value to keep the operation in the continuous conduction mode to have the same intermediate bus voltage ripple even though the inductance value is already much larger. (This voltage ripple subsequently reflected through the transformer to the output voltage.) These experimental results are in accordance with the (unique to this topology) detailed theoretical analysis on ripple cancellation in Section 3 and demonstrate clear benefits of the approach over prior state of the art, as previously discussed.

Although the conduction loss of the first stage increases when using discontinuous current because of the increased ac current components, the switching loss of the first stage are reduced, since the switches are turned on with zero current. Also, ignoring the effect of the short transition time, the size of secondary voltage ripple is directly determined by the voltage ripple on the intermediate capacitors. Since the second stage relies only on the leakage inductor of the transformer to suppress the secondary current ripple, even small voltage variations can lead to a noticeable current ripple. Therefore by operating at the proposed discontinuous current mode II to suppress the voltage ripple, the conduction power loss of the second stage (especially the secondary side) can be significantly reduced. An additional benefit of discontinuous operation is that the first stage has smaller size and quicker transient response. By applying the proposed topology in the built prototype, an efficiency of 88.3% at 600 V input and 5 V/30 A output is obtained. The efficiency is higher at low line (89.5% at 500 V input) and decreases to its lowest value at high line (87.25% at 700 V input). Although the major benefits of this topology proposed in this paper are for reduced voltage ripple and low switch stress, we remark that the power efficiency compares favourably to previously reported (80–90% in the literature [1–16]) two-stage or series input power converters – particularly for high-voltage inputs. In summary, the experimental results verify the principle and performance of the topology.

5 Conclusion and generalisations

This paper proposes a new topology of input-series connected two-stage converters suitable for high-input voltage applications. The voltage stress is greatly reduced (in half) by connecting two non-isolated converters in series for the first stage. At the same time, the second stage regulates the charge balance and fulfilled ZVS by using half-bridge with 50% duty cycle. Of course, a disadvantage of all input-series DC–DC converters is their extra number of switches required. Comparable input-series connected converters, as shown in Fig. 7, also need eight switches: four primary and four secondary SRs. Of course, traditional full-bridge converter, often used in higher voltage applications, require only four primary switches and two secondary SRs. Thus, there is a cost and performance design trade-off to be made. However, for high-input voltage, with wide input voltage range, the proposed topology has the benefit of enabling self-driven SR and reducing primary switch stress by one-half. In many cases, this may lead to the utilisation of MOSFETs instead of IGBTs, which may justify using the additional number of switches.

This paper focuses on the concept of input-series self-balanced connected two-stage converters is illustrated using a series buck + half-bridge implementation, but the idea can also be extended to derive multiple other new topologies. That is, from Fig. 1, it can be seen that the two-stage stacking approach can lead to multiple new topologies by selecting different non-isolated first stage

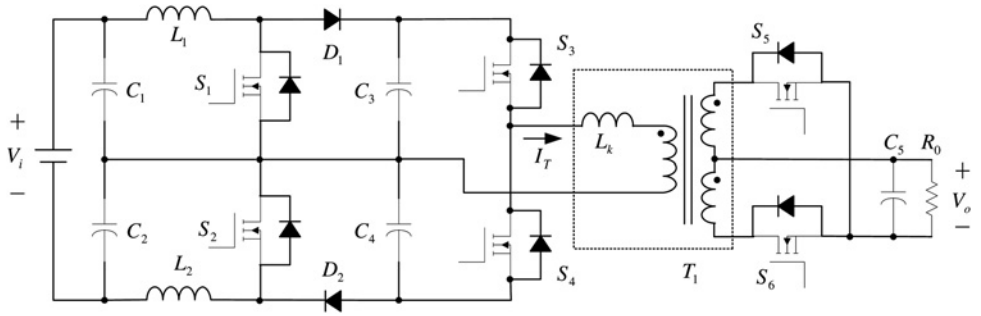

Figure 11 *Extension of ideas: self-balanced input-series two-stage scheme by using boost as the first stage*

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converters combined with various second stage dual ended isolated converters, such as dual ended forward converters or push–pull topologies. Also, any non-isolated converters can be used as the input-series converters, as demonstrated in Fig. 11 with boost converters. Future research will examine the detailed operation and benefits of these other specific topologies. However, conceptually, their methods are derived from the same concepts presented in this paper derived from Fig. 1: the input voltage is divided into half by the series capacitor connection. The two boost converters are connected in such a way that the second stage half-bridge would operate at 50% duty ratio, while the boost converter outputs are regulated.

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