Performance Prediction of DC–DC Converters With Impedances as Loads

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***Abstract*—This paper presents a method of predicting the outer loop gain of dc–dc converters when there is a general (nonresistive) impedance as a load. Based on this prediction, it is possible to then derive a corresponding phase margin, gain margin and bandwidth in order to define a dc–dc converter's stable operating area. Two applications of the method are presented for performance prediction in:**

1) **dc–dc converters with additional capacitors placed across their load;**
2) **source converters in a distributed power system.**

In both applications, the theoretical predictions match closely to the experimental data.

***Index Terms*—Bandwidth, dc–dc converters, gain margin, outer loop gain, phase margin.**

I. Introduction and Problem Motivation

DATASHEETS for switching power converters are rated for resistive loads. However, dc–dc converters are commonly used with loads that have capacitive or inductive components. For example, telecommunication and datacommunication users often add large filter capacitors across the output of commercially available dc–dc converters to meet the target impedance [4]. This is particularly necessary in applications involving large step output current disturbances [5], [6]. The additional filter capacitors will reduce the output voltage peak deviation to load disturbances.

However, the additional capacitor bank may cause some problems: All capacitors have parasitic equivalent series resistance (ESR), which introduces a (RC) zero in the transfer function of the feedback loop of the power module. The phase and gain margins of loop gains in today's power modules depend largely on the location of this zero. Adding a capacitor bank across the load will, therefore, greatly influence the relative stability properties of the converter, as well as its performance. Also, the additional capacitors will lower the corner frequency of the filter and thereby change crossover frequencies of loop gains.

Another important application of when a dc-dc converter is connected to an (complex valued) impedance is in a distributed power system (DPS). For instance, in telecommunication and datacommunication applications, on-board DPS's are attracting more attention, and examples of these DPS's include Intel's New Power Supply Architecture (NPSA) and Intermediate Bus Architecture (IBA) [7]–[12]. In such a DPS, a source dc–dc converter is connected to several load converters in parallel. The load converters work as a negative resistor at low frequency. Fortunately, its deteriorating effects on the source converter can be easily addressed at the stand-alone module design phase [13]. However, the interaction among power modules at high frequency mainly depends on the input filters of the load converters and may degrade system performance. In the worst case, the power system may become unstable. Therefore, it is important to carefully evaluate the DPS performance in the system design phase.

In both examples, it is vital that the load impedance does not cause internal stability problems for the source converter. This leads to the concept of defining a Stable Operating Area (SOA) for the source converter [5], i.e., defining the load impedances of the source converter that maintain "acceptable" system performance. Normally, "acceptable" performance for the source converter is defined as when its outer loop gain has phase margin above a pre-specified value, e.g., 60°.

One obvious way to determine the SOA is to use trial and error experimentation, where various impedances are used as loads to a power module [5]. Then phase margin and crossover frequency are directly measured on a loop gain, often the outer loop gain. The method can obtain precise results. However, it is exhaustive since hundreds of experiments might be necessary to fully characterize all the relevant load combinations. As a result, the method has primarily seen applications in the capacitor bank problem, described above, where the users are normally able to provide ranges of data for the additional output filter that they add to the power converter. Fig. 1(a) shows a typical SOA for the capacitor bank application that characterizes acceptable operation regions in the ESR versus Capacitance parameter space.

It is also possible to predict converter behavior by software such as SPICE. Software permits changing of circuit parameters, and hence, the effects of load changes are easily studied. However, accuracy of simulations is always suspect. For example, SOA regions are often based on minimum acceptable phase margin. For these calculations, averaging methods must be used. Averaging almost always assumes ideal switching, ignoring the nonlinear effects of the PWM, rectifiers and MOSFETs. Hence, errors will inevitably occur.

In an alternative approach, researchers have suggested that an SOA can be characterized in terms of impedances [14], [15]. If a converter has output impedance Z_O with load Z_L, then an impedance ratio can be defined as $T_m = Z_O/Z_L$. A SOA can be characterized in terms of a Nyquist plot of T_m, as shown in Fig. 1(b). Load impedance specifications do not require exhaustive experiments. However, the results tend to be conservative,

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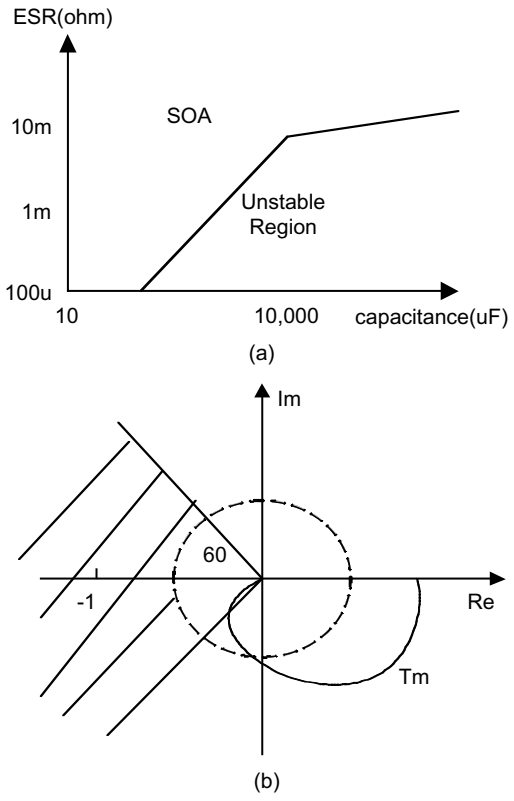

Fig. 1. SOA of dc–dc converters Fig. 1(a) illustrates an SOA for a capacitor bank for external capacitance versus ESR. In Fig. 1(b) the impedance ratio $T_m = Z_O/Z_L$ is forbidden to have Nyquist plot in the shaded region.

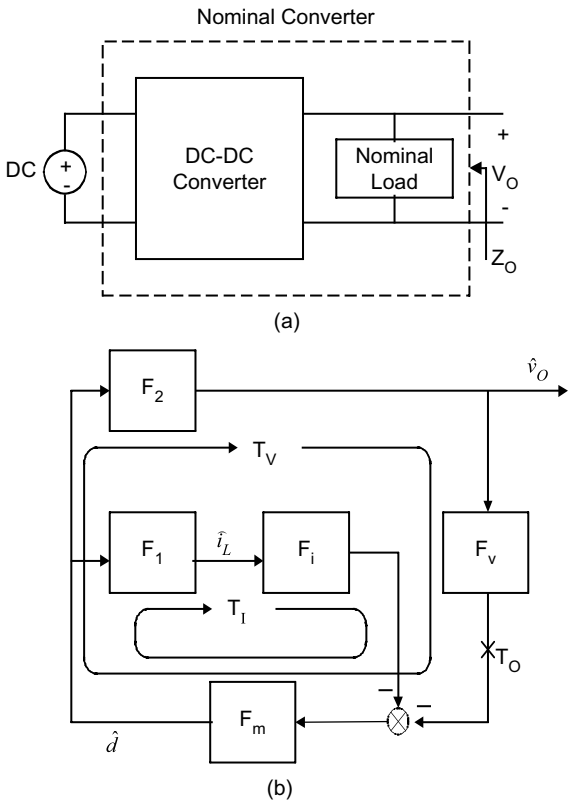

Fig. 2. (a) Defines the nominal converter under a specified operating condition/load. (b) Shows measurement of outer loop gain T_O for the converter.

and there is ongoing research that focuses on how to reduce conservativeness [16], [17].

The purpose of this paper is to present a new method to guarantee performance of dc-dc converters that have general impedances as loads. Our approach, however, is different from what has been previously presented in the literature [5], [14]–[18]. For example, instead of creating conditions that guarantee stability [14], [18], we show how to *predict* the outer loop gain for the source converter when its load is not a purely resistive impedance. That is, we assume that the nominal loop gains and nominal output impedance for the dc-dc converters are known, where "nominal" indicates a measurement with a resistive or dc current sink load (as we describe later). Then, using the developed theory in this paper, the new loop gains for the dc-dc converter are predicted for loads with arbitrary impedance.

Although the proposed theory can be implemented entirely in theory and simulation, improved accuracy is achieved when experimental data is included to characterize the dc-dc converter's nominal behavior. Thus, we first measure the nominal loop gains and nominal output impedance of the converter. Then, this data is imported into a software program and manipulated according to theoretical formula derived in this paper. The advantages of this approach are clear: increased modeling accuracy, flexibility in calculation, performance prediction, just to name a few. In essence, benefits of simulation have been combined with benefits of experiments. However, the proposed analysis tools presented in this paper can be implemented purely by analysis and simulation, if so desired.

The outline of the paper is as follows: In Section II the problem statement is formally given, and then, a mathematical theory is presented to derive an analytic prediction of the new outer loop gain for arbitrary load impedance. A step-by-step algorithm describes how an engineer might implement the procedure. Engineering insight is given for current mode control converters. The hope is that this insight, along with the design algorithm, allows the method to be used by the practicing engineers. Section III applies the results of Section II to the specific (important) problem of performance degradation for dc–dc converters with a capacitor bank. Three-dimensional plots are used to separately explain the influence of ESR and capacitance on the outer loop gain phase margin and crossover frequency. SOAs can be created as well. The experimental results substantiate the theory derived in Section II. Section IV presents an additional application of the results of Section II by predicting performance of the outer loop gain of a source converter in a DPS. The result is accurate for both on-line evaluation and prediction in the design phase. Conclusions are given in Section V.

II. Problem Statement and Solution [1]

A. Problem Statement

Fig. 2(a) defines a 'nominal' system for the source converter. That is, the nominal system represents the dc–dc converter with a specified (resistive or dc current sink) nominal load, specified

[1]The Results of Sections II and III previously appeared in [1] and [2]

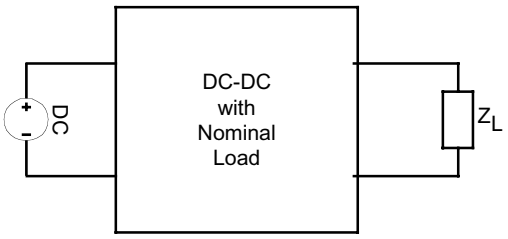

Fig. 3. DC–DC converter with arbitrary load.

output voltage, and specified input voltage. Hence, the operating point of the nominal source converter is uniquely defined.

Now, assume that the nominal systems in Fig. 2(a) has a known outer (voltage) loop gain T_O and closed loop output impedance Z_O for a given operating point (output current, output voltage, input voltage). The outer loop gain, T_O, is the loop gain obtained by injecting a small signal voltage disturbance as shown in Fig. 2(b). Current mode control converters are multi-loop control systems [19]. Using the notation of [19], F_1 is the duty-cycle-to-inductor-current transfer function. F_2 is the duty-cycle-to-output-voltage transfer function. F_i represents the current compensator, and F_V the voltage compensator. F_m is the control-to-duty-cycle transfer function. The current feedback loop gain is $T_I = F_1F_iF_m$ and the voltage feedback loop gain is $T_V = F_2F_VF_m$. In current mode control, $T_O = T_V/(1+T_I)$. In voltage mode control, T_O is equal to the voltage feedback loop gain. Typically, manufacturers design their converters so that T_O has sufficient phase and gain margin for all nominal operating points. The nominal load is almost always taken as an electric load, behaving either as a resistor or as a dc current sink.

Now consider the system in Fig. 3, which has an impedance Z_L connected as the load to the nominal converter. The impedance Z_L is arbitrary and can have capacitive or inductive components in it. The question answered in this paper is as follows:

Problem Statement: What is the new outer loop gain, denoted as T'_O, for the dc–dc converter with the added load, Z_L, assuming the same operating point as the nominal converter?

B. Problem Solution

Because the dc–dc converter is a feedback control system, the relationship between the output impedance and the outer loop gain can be addressed by using control theory. For dc–dc converters, the closed loop output impedance is given as

$$Z_O = \frac{Z_{\rm Oi}}{1+T_O} \tag{1}$$

where $Z_{\rm Oi}$ is the output impedance with the current loop closed and the voltage loop open in current mode control converters. For voltage mode control converters, $Z_{\rm Oi}$ is the open loop output impedance.

Viewing the loads as part of the source converter, a new, total source output impedance is given as $Z_{\rm total} = Z_O//Z_L$. On the other hand, we can also view the new system as having $Z_{\rm Oi}$ in parallel with Z_L with the voltage loop open. Therefore, the power module can be viewed as having $Z'_{\rm Oi} = Z_{\rm Oi}//Z_L$ subject to feedback. That is

$$\begin{aligned} Z_O//Z_L = Z_{\rm total} &= \frac{Z'_{\rm Oi}}{1+T'_O} = \frac{Z_{\rm Oi}//Z_L}{1+T'_O} \\ &= \frac{Z_{\rm Oi}}{(1+T'_O)(1+Z_{\rm Oi}/Z_L)} \end{aligned} \tag{2}$$

where T'_O is the outer loop gain with the influence of the load, and $Z'_{\rm Oi}$ represents the output impedance of the dc–dc converter with its voltage loop open with Z_L. Combining (1) and (2) leads to the new analysis equation that predicts the outer loop gain T'_O for arbitrary load Z_L

$$T'_O = \frac{T_O}{(1+T_O)Z_O/Z_L + 1}. \tag{3}$$

Hence, the outer loop gain of a dc–dc converter with an impedance load Z_L can be derived based on values of

1) the converter's nominal output impedance (without impedance Z_L);
2) the converter's nominal loop gain (without impedance Z_L);
3) the impedance, Z_L.

The first two quantities are easily obtained by measurement or directly from the manufacturer. Alternatively, they can be estimated by theory or simulation. The third quantity, the load impedance, is either provided by the user or manipulated in software.

It is interesting to note that according to (3), when $|Z_O/Z_L| \ll 1$, there is $T'_O = T_O$, and the stability of the source converter will be guaranteed. This is the same conclusion as the classic results of [18]. However, when the magnitudes of Z_O and Z_L are comparable, the conditions of [18] are no longer applicable. On the other hand, T'_O can be calculated from (3) using the proposed method and the changed loop gain can still be calculated. Since precise values of loop gain can be *predicted*, design conditions need not be conservative. Hence, this represents a fundamental different approach to creating sufficient condition for a SOA as in [5], [14], [15], [18].

Remark 1: The results of this section originally appeared in conferences [1], [2]. After [1], [2] appeared, another group independently submitted and published equivalent results [20]–[22] as our (3). Together with the results in this paper, [20]–[22] provide complimentary discussion on the new stability analysis approach. Further, the article in [6] explains how the methods explained in this section of the paper have seen technological transfer to telecommunication power supplies. (As a matter of reference, [1] first appeared 7/18/00.)

C. Simplification for Current Mode Control DC–DC Converters

The above method only considers the outer loop gain of the system. Although there are two control loops in current mode control dc–dc converters, no attempt is made to predict what occurs in the inner loop.

Fig. 4(a) shows a typical schematic of dc–dc converters. C is the output filter capacitor. A current mode control dc–dc converter can be regarded simply as a current source in parallel

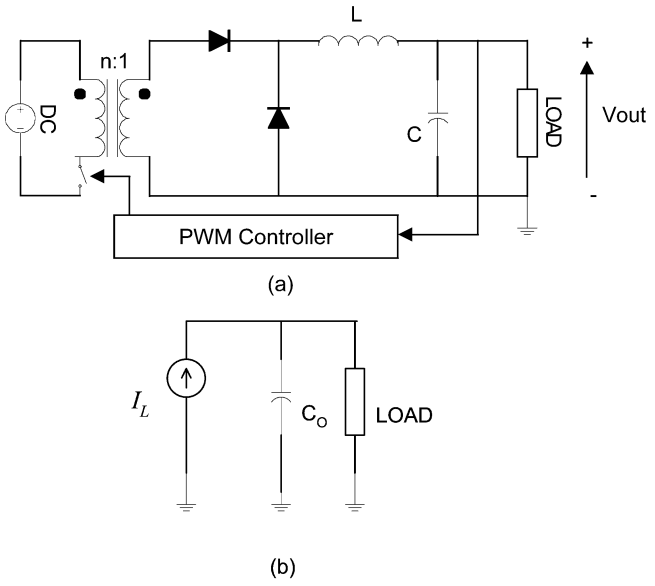

Fig. 4. (a) Typical schematic of dc–dc converter and (b) current source model of current mode control dc–dc converter.

with the output filter capacitor because the inner current control loop is much quicker than the outer voltage loop [19], [23]. The inductor and all parts to its left in Fig. 4(a) are modeled as the current source in Fig. 4(b). Additionally, input impedance of the PWM controller is assumed much larger than that of C in parallel with the load. Therefore, $Z_{\rm Oi}$ is approximately equal to the impedance of the output filter capacitor in parallel with the nominal load. Since $Z_{\rm Oi} = Z_O(1+T_O)$, the formula is simplified as

$$T_O' = \frac{T_O}{Z_{\rm Oi}/Z_L + 1}. \tag{4}$$

Practically, the impedance, Z_C, of the output filter capacitor of a dc–dc converter is much smaller than that of the nominal load, and, so, often we can simply take the impedance of the output filter capacitor as $Z_{\rm Oi} = Z_C//R_{\rm Load} \approx Z_C$. For the forward converter shown in Fig. 4, the impedance $Z_C(\approx Z_{\rm Oi})$ can be measured by turning the dc–dc converter off and measuring its output filter impedance.

Remark 2: Equation (4) corrects the typographical error in [2] which incorrectly replaced $Z_{\rm Oi}$ with Z_O.

D. Step-by-Step Implementation

In this section, we show how it is possible to implement the above theory to predict small signal changes from nominal behavior in dc–dc converters.

Step 1) Take sample measurements of nominal small signal behavior.

Measure the nominal output impedance, Z_O, and the nominal outer loop gain, T_O, of the dc–dc converter for sample load and line conditions. Specifically, we measure for high line/low load, high line/medium load, high line/low load, medium line/low load, ... low line/medium load, and low line/low load. Hence, we are attempting to characterize the nominal dc–dc converter behavior without the impedance load, Z_L.

Step 2) Import measurement data into software program.

In our work, we select MATLAB for data manipulation. Other programs such as MathCad, Maple, or Mathematica could as easily be selected. Alternatively, it is possible to write programs in C or Fortran. The important aspect of the software is that the user should be able to manipulate experimental data without too much effort. MATLAB provides a powerful simulation environment for data manipulation and graphical display of results, which is why it is utilized in this research.

Step 3) Manipulate the experimental data with theoretical prediction formula

$$T_O' = \frac{T_O}{(1+T_O)Z_O/Z_L + 1}.$$

Experimental data for output impedance, Z_O, and outer loop gain, T_O, are already known. We are interested in understanding the effects of the impedance Z_L on the new loop gain T_O'. Hence, a software program has been designed that calculates the loop gain for any possible Z_L. The program utilizes the above formula to predict T_O'. With this new loop gain, the program can then predict the new phase margin, crossover frequency, and gain margin, for different impedances Z_L. Likewise, it is a simple calculation to derive a SOA for the converter, e.g., when the phase margin of the outer loop gain is greater than 60°.

Step 4) Display the results, perhaps by using scientific visualization tools such as those found in MATLAB.

The above step-by-step procedure shows how it is possible to combine experimental data with theoretical calculations in a simulation environment. Of course, (3) and (4) can be used without experimental data, that is, completely with software. A user can theoretically calculate nominal loop gains and output impedance of the source converter. Then software can be used to predict the changes in the outer loop gain when a load impedance is specified.

III. Influence of Capacitive Load on DC–DC Converters

Section II presents fundamental theory to predict the new loop gain of a dc-dc converter when it has a general load impedance Z_L. In this section, we apply the theoretical results to the important practical problem of when the load impedance is a capacitor bank placed across a resistor. As previously mentioned in the introduction, it is common practice in telecommunication's and datacommunication's power supply design to add this capacitor bank across the output of power modules in order to reduce the output peak deviation to load disturbances [4], [5].

In this case, we assume that the nominal loop gain T_O, nominal output impedance Z_O, and added load Z_L are as shown in Fig. 5. Experimental results have indicated that it is pos-

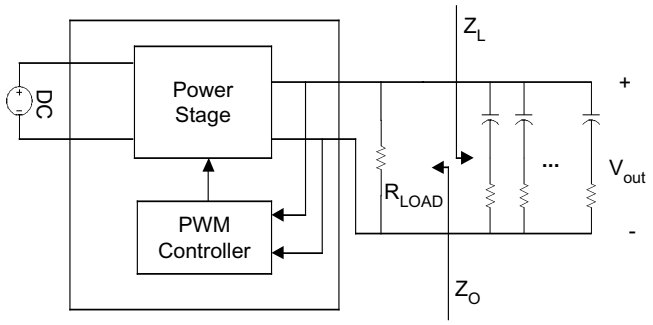

Fig. 5. Feedback diagram of dc–dc converter with capacitor bank.

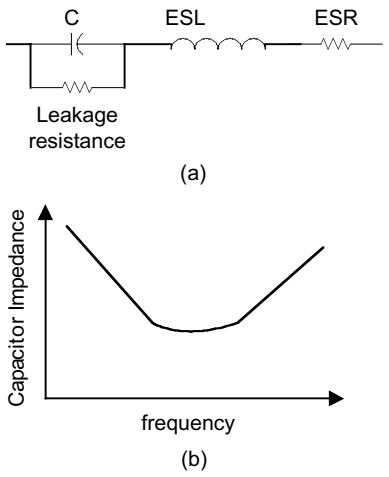

Fig. 6. Model of a capacitor and its impedance characteristics.

sible to lump all the capacitors together and model $Z_L(j\omega) = R + (1/j\omega C)$, where R and C are equivalent series resistance and capacitance, respectively. Of course, a real model of a capacitor includes the capacitance (C), the equivalent series inductance (*ESL*), leakage resistance, and R [24]. The model and its impedance characteristics are shown in Fig. 6. However, the frequency around the crossover frequency is of interest, and the effect of ESL is seen at high frequency. It is reasonable to consider only capacitance and ESR in the model.

Experiment 1: As a benchmark experiment, we have added a capacitor bank to a nonisolated, voltage mode control, boost converter with up to 20 W of output power. The input voltage range is from 3.0 VDC to 4.0 VDC and the output voltage is 5.0 VDC. It operates at a switching frequency of 400 kHz and has an efficiency of approximately 90%. We apply the step-by-step procedure presented in Section II: First, the nominal outer (voltage) loop gain and the nominal output impedance are experimentally measured when the load is a resistor. This experimental data is imported into a MATLAB program. Using MATLAB and (3), we calculate the loop gain for different values of $Z_L(j\omega) = R + (1/j\omega C)$. That is, the capacitance value is first fixed and loop gains T'_O are computed for incremental values of R. Then the capacitor value is incremented, and the entire procedure is repeated over and over again. The final result is hundreds of different loop gains for different R, C combinations. Obtaining phase margin, gain margin, and crossover frequency is also performed in MATLAB. This is

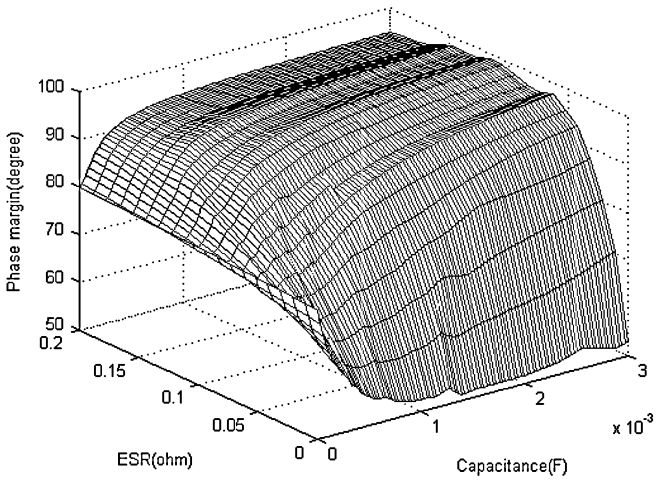

Fig. 7. Phase margin prediction of dc–dc converter with capacitor bank. Experimental measurements match prediction to within $\pm 1.5°$.

straightforward since these quantities are derived from T'_O. The prediction of T'_O is subsequently compared to the actual T'_O that is experimentally measured.

Because MATLAB has scientific visualization capabilities, it is possible to provide interesting graphs of the predictions. Fig. 7 shows a three-dimension plot of phase margin versus ESR and C of the boost converter. Fig. 8 shows the crossover frequency versus ESR and C. The predicted phase margin and crossover frequency shown in these figures are within 5% error from the actual measured values. For example, *predicted phase margin is within* ± 1.5 *degrees from its measured values*. (We have sampled over 30 data points to compare predicted data with measured data. The figures present an infinite number of data points, so it is not possible to test all possible impedance conditions.) For this experiment, input voltage is 3.3 V, and the nominal load resistor is 2 Ω.

Figs. 7 and 8 give practical insight on the influence the capacitor bank has on performance. For this example, low ESR reduces phase margin dramatically. As ESR is increased, the phase margin will slowly increase, giving a stabilizing effect. Crossover frequency of the outer loop gain initially decreases when capacitance increases. For low ESR values, the crossover frequency continues to decrease. For large values of ESR, however, the crossover frequency levels off, for example, above 6 kHz for 200 mΩ.

These frequency domain characteristics can be correlated to time domain performance. General rules of thumb are that the phase margin divided by 100 gives the damping ratio and therefore can be used to estimate percent overshoot. That is, lower phase margin will increase percent overshoot to step responses (load or input voltage disturbances). Likewise, lower crossover frequency increases the settling time.

These figures demonstrate possible design tradeoffs when using a capacitor bank: Additional capacitance can sometimes reduce the phase margin if the ESR is not sufficiently high. Hence, overshoot to step output current disturbances may actually increase, which is contrary to the purpose of adding the capacitor bank. Likewise, settling time can become slow since crossover frequency is sometimes reduced. However, as the

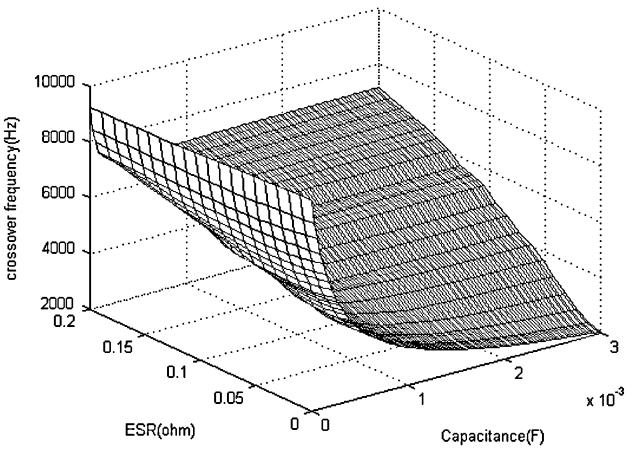

Fig. 8. Crossover frequency prediction of dc–dc converter with capacitor bank. Experimental measurements match prediction to within 5%.

figures show, proper design of the capacitor bank can guarantee high phase margin as well as sufficient crossover frequency, since phase margin can actually increase for sufficiently high capacitance.

IV. Distributed Power Systems (DPS)

Evaluation of DPS with (3) also provides useful information. In this paper, DPS always refers to on-board DPS such as Intel's New Power Supply Architecture (NPSA) and Intermediate Bus Architecture (IBA) [7]–[12]. The on-board DPS uses isolated dc–dc converter to transfer the energy from the backbone to the board. Other point-of-load converters use the output of the isolated converter as input and are nonisolated. For such DPS, the load is actually one or more dc–dc converter. Each load converter has an associated input impedance (including its input filter). The total load impedance, Z_L, seen by the source converter would be the total impedance of all these input impedances in parallel.

As in the capacitor bank application, it is possible to predict changes in the source converter's outer loop gain, relying on measurements of nominal characteristics. The procedure to do this is the same as before: Measure nominal outer loop gain and the nominal output impedance of the source converter. Then import the data into a simulation program to manipulate the load Z_L according to (3). The designer can, therefore, predict phase margin and crossover frequency of the source converter's outer loop gain by simulating (3) for all possible Z_L. In this case, the method is exactly the same as before, and therefore, we do not present details of the approach in this section.

Instead, this section illustrates how (3) can be helpful in DPS for on-line evaluation and for a special instance of performance prediction. Specifically, in Section IV-A, we develop a method based on (3) to measure the outer loop gain of the source converter in a DPS. The interesting aspect of the approach is that users do not need to "break the loop," as suggested in Fig. 2(b), in order to obtain measurements. The method is simple and can be performed by users or designers, since it does not require making connections to internal circuitry of the source converter. In Section IV-B, the experimental method is utilized to predict

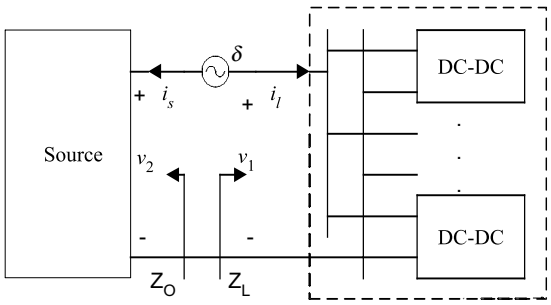

Fig. 9. Impedance ratio measurement, $(\mathrm{Z_o}/\mathrm{Z_L})$.

the outer loop gain of the source converter for the specific case when there are n identical load converters in parallel.

A. On-Line Evaluation [2]

This subsection describes a method to use simple measurements, along with (3), to predict the outer loop gain of the source converter in a DPS that has already been built. Normally, it is not possible for a customer to measure the outer loop gain of the source converter unless they decide to "break open" the source converter and cut internal circuitry. This is cumbersome and has the undesirable effect of physically altering the source converter. Hence, it is beneficial to develop an on-line method of outer loop gain measurement that does not require penetration into the source converter.

Notice that, in (3), the new loop gain depends on the impedance ratio Z_O/Z_L. Hence, it is not actually necessary to measure both Z_O and Z_L separately, especially if it is possible to measure the ratio directly. Fig. 9 shows a way to measure this ratio directly. A small signal perturbation, δ, is injected into the connection cables. δ can be either a small signal voltage source or a small signal current source.

Therefore, the output impedance of the source, Z_O, and the input impedance, Z_L, are

$$\mathrm{Z}_O = \frac{v_2}{i_s}; \quad \mathrm{Z}_L = \frac{v_1}{i_l}.$$

Meanwhile, because $i_s = -i_l$, there is

$$\frac{\mathrm{Z}_O}{\mathrm{Z}_L} = -\frac{v_2}{v_1} \equiv \text{impedance ratio}.$$

Then (3) is simplified as

$$T_O' = \frac{T_O}{(1+T_O)(-v_2/v_1)+1}. \tag{5}$$

This method to obtain T_O' is simple and can be performed by users or designers, since it does not require making connections to internal circuitry in any of the converters. The user, however, must have access to the nominal loop gain of the source converter, which might be available from the manufacturer. This leads to the following procedures to evaluate the outer loop gain of the source dc-dc converter in an existing DPS.

[2]The results of this subsection previously appeared in IEEE APEC 2001, 3/4/01-3/8/01 [3].

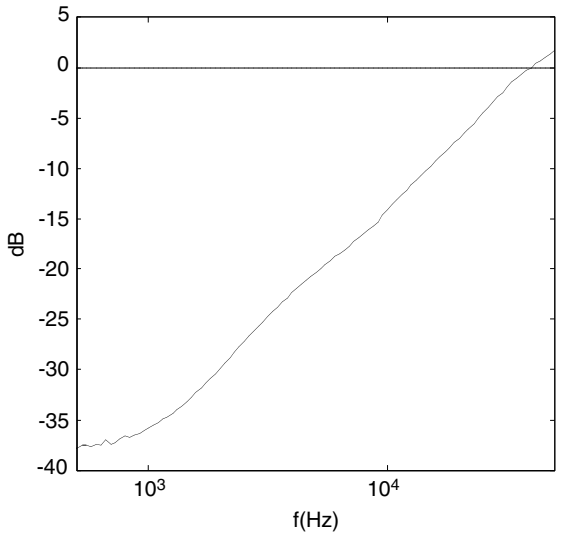

Fig. 10. Experimental measurements of the magnitude of impedance ratio for Example 2.

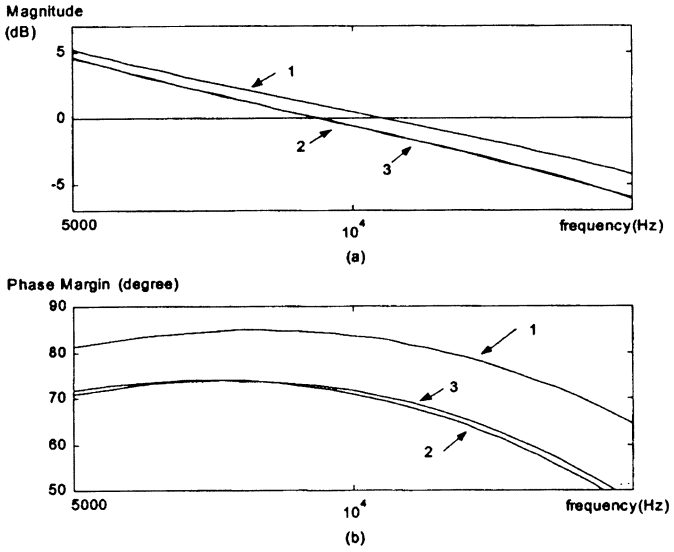

Fig. 11. Nominal outer loop gain (1); calculated (2); and experimentally measured (3) outer loop gain with load converters. (a) Magnitude in dB. (b) Phase margin in degrees.

Step 1) Measure the impedance ratio of the DPS, as described earlier.

Step 2) Import manufacturer nominal loop gain measurements for the source converter and the measured impedance ratio into software.

Step 3) Use (5) to calculate the new loop gain, T_O', in a software program (MATLAB is used in this research).

Phase margin, gain margin and crossover frequency can be derived directly from T_O'.

Experiment 2: To demonstrate the accuracy of the on-line evaluation, an experimental DPS system with a forward converter as a source with output current 5 A, and a load consisting of four buck converters in parallel is built. The source converter has a 34 V–75 V input and a 3.3 V output. The load converters consist of four dc-dc converters, three of which have 3.3 V input and 1.9 V output, and one of which has 3.3 V input and 2.5 V output.

Fig. 10 shows the measured magnitude of impedance ratio. The magnitude below 1 kHz is much smaller than one and the change of the loop gain is negligible at that frequency range. For frequencies above 1 kHz, the magnitude becomes closer to one and the magnitude is greater than one at higher frequency. Therefore, classical impedance matching method [18] is not applicable since $|Z_O/Z_L| \approx 1$ in the frequency range near the crossover frequency of T_O of the source converter. Formula (5) is applied to evaluate the performance. Fig. 11 shows the accuracy of the method. Curve 3 is the measured outer loop gain of the source converter with loads and Curve 2 is the calculated outer loop gain using the three-step procedure described above. Curve 1 represents the nominal loop gain of the source converter. Experimental results closely match predicted results, i.e., Curve 3 almost superimposes Curve 2.

Notice that the original outer loop gain without the load converter (nominal loop gain) is different from the loop gain of the source converter when connected to the load converters. Although the system is still stable, there is clearly performance degradation. The crossover frequency reduces from 10.80 kHz to 9.21 kHz, while the phase margin reduces from 82.8° to 72.7°. As show in Fig. 11, the predicted values are 9.24 kHz and 72.2°.

B. DPS Having (n) Identical DC–DC Converters as the Load

In this subsection, the special case of having n identical load converters is examined. (This is common in practice.) For this case

$$Z_L = \frac{Z_{L1}}{n}$$

where Z_{L1} is the input impedance of one load converter.

Then (3) can be rewritten as

$$T_O' = \frac{T_O}{(1+T_O)nZ_O/Z_{L1}+1}. \tag{6}$$

Therefore, the performance of the source converter can be predicted if the impedance ratio of the output impedance of the source converter and that of one load converter are known. The multiplication of Z_O/Z_{L1} by n can be performed in software. This implies that a scaled, benchmark DPS can be built, with one load converter, in order to predict the performance when there are n identical load converters, where n is arbitrary. This is particularly helpful when designing the DPS.

Fig. 12 shows a possible implementation of the impedance ratio for one load converter. Fig. 12 is the same as Fig. 9 except that a dc current sink I is used, which ensures that the source converter works at the same operating point as when n load converters are applied. A dc current sink has infinite output impedance, therefore

$$\frac{Z_O}{Z_{L1}} = -\frac{v_2}{v_1} \equiv \text{Individual impedance ratio A.}$$

The outer loop gain for a DPS system with n identical load converters can then be predicted using (6), and software manipulation (as we have previously described).

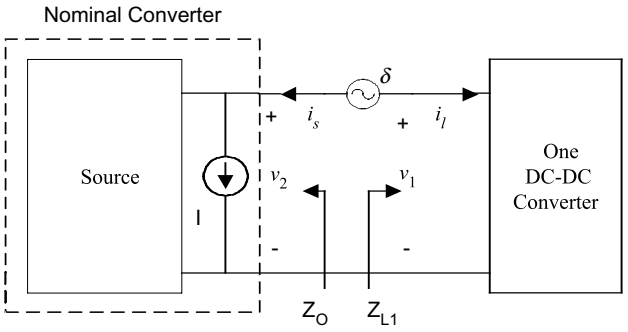

Fig. 12. Impedance ratio measurement for DPS with one load converter.

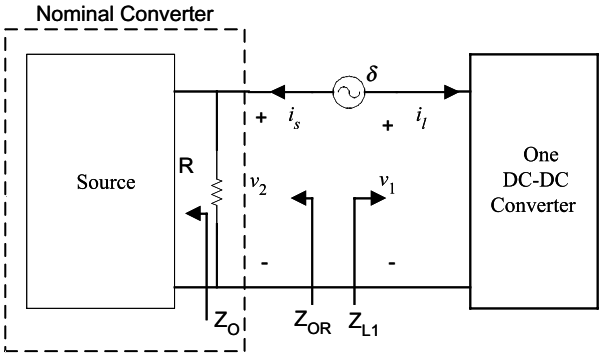

Fig. 13. Alternative individual impedance ratio measurement.

Fig. 13 shows an alternative implementation. A resistor, R, is used to adjust the operating point. In this case, the measured impedance ratio is

$$\frac{Z_{\rm OR}}{Z_{L1}} = -\frac{v_2}{v_1} \equiv \text{Individual impedance ratio B}$$

where $Z_{\rm OR} = Z_O//R$. In many cases, $|Z_O| < 0.1R$, so

$$\frac{\rm Z_O}{\rm Z_{L1}} \approx -\frac{v_2}{v_1}.$$

This approximation simplifies the implementation although it will bring some errors.

Experiment 3: A benchmark system is built to verify the proposed approach. The DPS consists of a forward source converter and four buck load converters. The source converter has a 34 V–75 V input, 3.3 V output, and an output current of 6 A. The four identical load converters have 3.3 V input and 1.9 V output, and each has resistive load 0.8 Ω.

First, nominal loop gains and individual impedance ratios (as in Figs. 12 and 13) are measured. Using (6), the prediction of the phase margins and crossover frequency of the DPS is then obtained. The magnitude and phase of the predicted loop gains are plotted in Fig. 14.

The nominal outer loop gain has phase margin 69.9° and crossover frequency 3.47 kHz; in the DPS, the measured source converter has phase margin 58.6° and crossover frequency 3.17 kHz. Using individual impedance ratio A, the predicted phase margin is 58.9°, and the predicted crossover frequency is 3.12 kHz; using individual impedance ratio B, the predicted phase margin is 59.9°, and the predicted crossover frequency is 3.32 kHz.

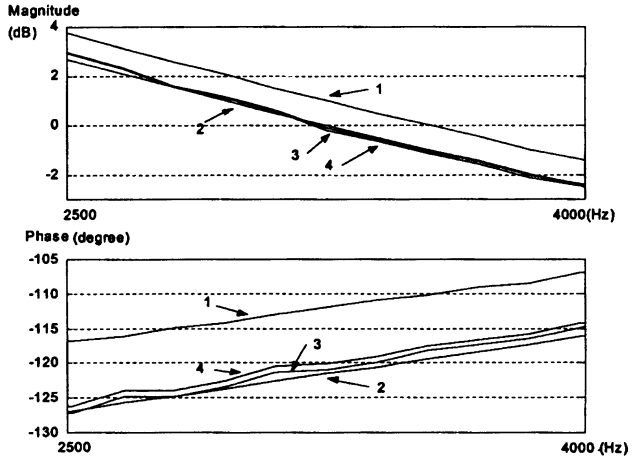

Fig. 14. Curve (1) is the nominal outer loop gain of source converter. Curves (2)–(4) consider four identical buck converters as the load. Curve (2) is the experimentally measured outer loop gain of source converter. Curve (3) is the predicted outer loop gain using individual impedance ratio A. Curve (4) is the predicted outer loop gain using individual impedance ratio B.

V. Conclusion

Performance of dc–dc converter with loads that are not purely resistive is discussed. With the proposed methods, it is possible to predict the outer loop gain of the dc–dc converter when it has arbitrary (complex valued) load impedance. The results depend on knowledge of the nominal loop gain and nominal output impedance of the converter.

Since the method to predict the outer loop gains is valid for arbitrary load impedances, the approach is valid for many important applications. For example, Section III describes how it is possible to predict phase margin and crossover frequency for dc-dc converters that have a capacitor bank across their load. Section IV applies the method to predict the outer loop gain of a source converter in DPS. Experiments in both cases support the theory presented.

One interesting aspect of the proposed approach is that it is possible (although not necessary) to combines experimental measurements and theoretical predictions within a software environment. First, nominal outer loop gains and nominal output impedance are measured. The data is then imported into a MATLAB program and manipulated according to theoretical algorithms [(3) or (4)]. Software is used to vary the impedance load, and hence the proposed method has flexibility in changing the load. On the other hand, the method is also accurate since it is only predicting changes in performance and not the nominal performance itself. The results suggest that when experimental data is available for a power electronic system, it is beneficial to use this data to improve modeling accuracy. Future research will investigate other possibilities of combining experiments and simulation, such as measuring the behavior of the power switches and using this data within a SPICE large signal transient simulation.

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