

David R. Kaeli

Dept. of Electrical and Computer Engineering

Northeastern University

Boston MA 02115

email: kaeli@ece.neu.edu

phone: (617) 373-5413

Education

BS EE 1981 Rutgers University
MS CE 1985 Syracuse University
PhD EE 1992 Rutgers University

Positions Held

1981-1986 Staff Engineer, IBM Enterprise Systems, Poughkeepsie, NY
1986-1993 Advisory Engineer, IBM T.J. Watson Research Center, Yorktown Heights, NY
1993-1999 Assistant Professor, Northeastern University, Boston, MA
1999-2005 Associate Professor, Northeastern University, Boston, MA
2001-2002 Visiting Professor, Universitat Politecnica de Catalunya, Barcelona, Spain
2005-present Full Professor, Northeastern University, Boston, MA
2010-2013 Associate Dean, College of Engineering, Northeastern University, Boston, MA
2011-present Honorary Professor, City University, London, England
2014-present Courtesy Appointment, CCIS, Northeastern University, Boston MA
2018-present Courtesy Appointment, BioEngineering, Northeastern University, Boston MA
2014-present Distinguished Full Professor, COE, Northeastern University, Boston MA

Leadership Experience

- Associate Dean of Undergraduate Programs, College of Engineering, Northeastern University, 2010-2013
- Editor-in-Chief, ACM Transactions on Architecture and Code Optimization, 2020-present
- Chair, IEEE Technical Committee on Computer Architecture, 2009-2015
- Chair, IEEE Technical Committee on Microarchitecture and Microprogramming, 2007-2010
- Executive Committee, IEEE Technical Committee on Computer Architecture, 2000-2006, 2015-present

- Executive Committee, IEEE Transactions on Multi-Scale Computing Systems, 2016-2018
- Member, NSF TeraGrid Scientific Advisory Board, 2007-2010
- Member, CRA Computing Community Consortium, 2007-2010
- Chair, Northeastern University Faculty Senate Academic Policy Committee, 2016-2018
- Massachusetts Green High Performance Computing Center Research Committee, member 2010-2014, co-chair 2015-present

University/College/Department Service and Leadership

- Co-Director of the Institute for Information Assurance - 2005-2012
- Co-Director of the MS Program in Data Science - 2018-present
- University Faculty Senate Agenda Committee - 2018-2019
- University Faculty Senate IT Policy Committee (co-chair) - 2017-2018
- University Undergraduate Curriculum Committee - 2010-2013, 2017-2018
- University Faculty Senate Member, 2017-2019
- University Faculty Senate Academic Policy Committee (chair) - 2016-2018
- University Faculty Senate Academic Policy Committee - 2015-2016
- University CIO Search Committee - 2017-2018
- University IT Cloud Strategy Taskforce - 2018
- University Academic Research Computing Users Group (chair) - 2006-2008
- University Goldwater Scholarship Award Committee - 2009-present
- University Undergraduate Research Committee - 2014
- University International Student Success Task Force (chair) - 2011-2013
- University Research Computing Advisory Committee - 2015-present
- University Research Computing Advisory Committee (co-chair) - 2012-2015
- University Intellectual Property Committee - 2007-2013
- University Retention Taskforce - 2010-2013
- University Provost Search Committee - 2019-2020
- University Associate Vice Provost Search Committee (co-chair) - 2023-present

- University Cadre of Marshals - 2015-present
- COE Tenure and Promotion Committee - 2017-2021, (co-chair 2019-2020)
- COE Research Computing Group (co-chair) - 2014
- COE Computer Committee, 1994-2000, 2002-2003
- COE Diversity, Equity and Inclusion Committee - 2018-present
- ECE Diversity Equity and Inclusion Committee (chair) - 2020-present
- ECE Department Council (chair) - 2014-2016
- ECE Undergraduate Study (chair) - 2005-2010, 2013
- ECE Faculty Search Committee in Intelligent, Secure, Autonomous and High Performance Systems Chair - 2018
- Data Science Search Committee, Chair - 2018-2020
- ECE Tenure and Promotion Committee - 1999-2000, 2002-2006, 2009 (chair), 2014-2016, 2018, 2019 (chair), 2022 (chair)
- ECE Faculty Search Committee in Architecture and Computation (chair) - 2014-2016
- ECE Faculty Search Committee in NeuroComputing (chair) - 2013-2014
- ECE Teaching Faculty Search Committee - 2016-2018
- ECE Graduate Admissions Chair - 1995-2000
- ECE Undergraduate Study Committee - 1999-present
- ECE Faculty Search Committee (chair) - 1994-1998
- ECE Faculty Search Committee - 1998-2000, 2005, 2009, 2013
- Data Science Faculty Search Committee (chair) - 2023
- Khoury College of Computer Sciences Dean Search Committee - 2021
- Bouve College of Nursing Dean Search Committee - 2018-2019

Journal Publications

1. "A Framework for Enhancing Monte Carlo Photon Transport Simulations Using Machine Learning," with M.R. Ardakani, L. Yu and Q. Fang, *Multimodal Biomedical Imaging XVIII*, PC12371, 2023, <https://doi.org/10.1117/12.2659549>.
2. "Accelerating Finite Field Arithmetic for Homomorphic Encryption on GPUs," with N. Livesay, G. Jonaton, E. Mora, K. Shivdikar, R. Agrawal, J. Joshi, J.L. Abellan, and J. Kim, *IEEE Micro Magazine*, 3(8), 2023, pp. 55-63, <https://doi.org/10.1109/MM.2023.3253052>.
3. "SECDA-TFLite: A Toolkit for Efficient Development of FPGA-based DNN Accelerators for Edge Inference," with J. Haris, P. Gibson, J. Cano and N.b. Agostini, *Journal of Parallel and Distributed Computing*, Vol. 173, March 2023, <https://doi.org/10.1016/j.jpdc.2022.11.005>.
4. "Supply Chain Resilience: Impact of Stakeholder Behavior and Trustworthy Information Sharing with a Case Study on Pharmaceutical Supply Chains," with O. Ergun, J. Griffin, N. Chicoine, M. Gong, O. Mohaddesi, Z. Raziiei, C. Harteveld and S. Marsella, *INFORMS Tutorials in Operatio Research*, Oct. 2022, <https://doi.org/10.1287/educ.2022.0246>.
5. "Machine Learning-based Determination of Sampling Depth for Complex Environmental Systems: Case Study with Single-Cell Raman Spectroscopy Data in EBPR Systems," with G. Li, C. Wu, D. Wang, V. Srinivasan, J.G. Dy and A.Z. Gu, *Environmental Science and Technology*, 56(18), 2022, pp. 13473-13484, <https://doi.org/10.1021/acs.est.1c08768>.
6. "Machine Learning-based Biomarkers Identification from Toxicogenomics-Bridging to Regulatory Relevant Phenotypic Endpoints," with S.M. Rahman, J. Lan, J. Dy, A. Alshawabkeh and J.G. Dy, *Journal of Hazardous Materials*, Vol. 423, Issue B, 2022, <https://doi.org/10.1016/j.jhazmat.2021.127141>.
7. "VCSR: An Efficient GPU Memory-aware Sparse Format," with E. Karimi, *IEEE Transactions on Parallel and Distributed Systems*, 33(12), 2022, pp. 3977-3989, DOI:10.1109/TPDS.2022.3177291.
8. "Framework for Denoising Monte Carlo Photon Transport Simulations Using Deep Learning," with M.R. Ardakan, L. Yu and Q. Fang, *Journal of Biomedical Optics*, 27(8), 2022, <https://doi.org/10.1117/1.JBO.27.8.083019>.
9. "Machine Learning-based Biomarker Identification from Toxicogenomics - Bridging to Regulatory Relevant Phenotypic Endpoints, with S.M. Rahman, J. Lan, J. Dy, A. Alshawabkeh and A.Z. Gu, *Journal of Harzardous Materials*, Vol. 423B, 2022.
10. "Spartan: A Sparsity-Adaptive Framework to Accelerate Deep Neural Network Training on GPUs," with S. Dong, Y. Sun, N. Bohm-Agostini, E. Karimi, D. Lowell, J. Zhou, J. Cano-Reyes and J.L. Abellan, *IEEE Transactions on Parallel and Distributed Systems*, Vol. 32, No. 10, 2021, pp. 2448-2463.
11. "Exploring GPU Acceleration of Deep Neural Networks Using Block Circulant Matrices," with S. Dong, P. Zhao, and X. Lin, *Parallel Computing*, Vol. 100, 2020.

12. "Characterizing and Exploiting Soft Error Vulnerability Phase Behavior in GPU Applications," with F.G. Previlon and C. Kalra, *IEEE Transactions on Dependable and Secure Computing*, 2020, DOI: 10.1109/TDSC.2020.2991136.
13. "Nacre: Durable, Secure and Energy-Efficient Non-Volatile Memory Utilizing Data Versioning," with M.K. Tavana and Y. Fei, *IEEE Annals of the History of Computing*, Vol. 8, 2020, pp. 897-906.
14. "Effects of Trust-based Decision Making in Disrupted Supply Chains," with R. Doroudi, P. Sequeira, S. Marsell, O. Ergun, R. Azghandi, Y. Sun and J. Griffin, *PLOS ONE*, 15(2), Feb. 2020.
15. "ArmorAll: Compiler-based Resilience Targeting GPU Applications," with C. Kalra, F. Previlon and N. Rubin, *ACM Transactions on Architecture and Code Optimization (TACO)*, 17(2), 2020, pp. 1-24.
16. "Exploiting Bank Conflict based Side-channel Timing Leakage of GPUs," with Z.H. Jiang and Y. Fei, *ACM Transactions on Architecture and Code Optimization (TACO)*, 16(4), 2019, pp. 1-24.
17. "Priority-Based PCIe Scheduling for Multi-Tenant Multi-GPU Systems," with C. Li, Y. Sun, L. Jin, L. Xu, Z. Cao, P. Fan, S. Ma, Y. Guo and J. Yang, *IEEE Computer Architecture Letters*, 18(2), 2019.
18. "Intra-Cluster Coalescing and Distributed-Block Scheduling to Reduce GPU NoC Pressure", with L. Wang, X. Zhao, Z. Wang and L. Eeckhout, *IEEE Transactions on Computers*, 68(7), 2019, pp. 1064-1076.
19. "Analyzing and Increasing the Reliability of Convolutional Neural Networks on GPUs," with F. dos Santos, P.F. Pimenta, C. Lundardi, L. Draghetti, L. Carro and P. Rech *IEEE Transactions on Reliability*, 68(2), 2019, pp. 663-677.
20. "Side-channel Timing Attack on RSA on a GPU," with C. Luo and Y. Fei, *ACM Transactions on Architecture and Code Optimization (TACO)*, 16(3), 2019, pp. 1-32.
21. "HAWS: Accelerating GPU Wavefront Execution through Selective Out-of-Order Execution," with X. Gong, X. Gong and L. Yu, *ACM Transactions on Architecture and Code Optimization (TACO)*, 16(2), February 2019.
22. "Effect of Hydrogeological and Anthropogenic Factors on the Spatial and Temporal Distribution of CVOCs in the Karst System of Northern Puerto Rico," with N.I. Torres, V.L. Rivera, I.Y. Padilla, D. Macchiavelli and A.N. Alshawabkeh, *Environmental Earth Science*, Springer Verlag, 2019.
23. "Reproducing Performance of a Multi-Physics Simulation of the Tsunamigenic 2004 Sumatra MegaThrust Earthquake on the AMD EPYC 7551 Architecture," with C. Bunn, H. Barclay, A. Lazarev, F. Yusuf, J. Fitch, J. Booth and K. Shivdikar, *Parallel Computing*, Elsevier, 90(102568), December 2019.

24. "Analyzing and Increasing the Reliability of Convolutional Neural Networks on GPUs," with F.F. Dos Santos, P.F. Pimenta, C. Lunardi, L. Draghetti, L. Carro and P. Rech, *IEEE Transactions on Reliability*, Nov. 2018, pp. 1-15.
25. "Student Cluster Competition 2017, Team Northeastern University: Reproducing Vectorization of the Tersoff Multi-Body Potential on the NVIDIA V100," with Z. Marcus, J. Booth, C. Bunn, M. Leger, S. Hance, T. Sweeney, and C. McCardwell, *Parallel Computing*, Vol. 78, Oct. 2018, pp. 67-71.
26. "Power Analysis Attack of an AES GPU Implementation," with C. Luo, Y. Fei, A.A. Ding, P. Luo, and S. Mukherjee, *Journal of Hardware and Systems Security*, 2018, Springer International, pp. 1-14.
27. "On the Efficacy of ECC and the Benefits of FinFET Transistor Layout in GPU Reliability," with R.P. Luncardi, F. Previlon and P. Rech, *IEEE Transactions on Nuclear Science*, 65(8), 2018, pp. 1843-1850.
28. "Student Cluster Competition 2017, Team Northeastern University: Reproducing Vectorization of the Tersoff Multi-Body Potential on the NVIDIA V100," with Z. Markus, J. Booth, C. Bunn, M. Leger, S. Hance, T. Sweeney and C. McCardwell, *Parallel Computing*, Vol. 27, 2018, pp. 67-71.
29. "The Influence of Hydrogeological and Anthropogenic Variables on Phthalate Contamination in Eogenetic Karst Groundwater Systems," with N.I. Torres, X.Yu, I.Y. Padilla, R.E. Macchiavelli, R. Ghasemizadeh, J.F. Corder, J.D. Meeker and A.N. Alshawabkeh, *Environmental Pollution*, Vol. 237, June 2018, pp. 298-307.
30. "Block Cooperation: Advancing Lifetime of Resistive Memories by Increasing Utilization of Error Correcting Codes," with M.K. Tavana and A.K. Ziabari, *ACM Transactions on Architecture and Code Optimization (TACO)*, 15(3), 2018, pp. 1-16.
31. "Scalable and Massively Parallel Monte Carlo Photon Transport Simulations for Heterogeneous Computing Platforms," with L. Yu, F. Nina-Paravecino, and Q. Fang, *Journal of Biomedical Optics*, 23(2), 2018.
32. "Fast Monte Carlo Photon Transport Simulations for Heterogeneous Computing Systems," with L. Yu, F. Nina-Paravecino, and Q. Fang, *Clinical and Translational Biophotonics*, OSA Technical Digest, 2018.
33. "Accelerated Design of Strong, Highly Conductive Carbon Nanotube-based Fibers via Electrical Fusion," with Y.J. Jung, M. Upmanyu, and C. Livermore, *Materials Genome Initiative - Accelerating Materials Research*, Vol. 4. 2018, pp. 172-174.
34. "Team Science Applied to Environmental Health Research: Karst Hydrogeology and Preterm Birth in Puerto Rico," with J.F. Cordero, J.D. Meeker, R. Loch-Caruso, R. Giese, I. Padilla, D. Vesper, T. Sheahan, P. Brown, C.M. Velez-Vega and A. Alshawabkeh, *Karst Groundwater Contamination and Public Health*, Springer, 2018, pp. 17-25.

35. "Lightweight Hardware Transactional Memory for GPU Scratchpad Memory," with A. Villegas, R. Asenjo, A. Navarro, and O. Plata, *IEEE Transactions on Computers*, 67(9), 2018, pp. 816-829.
36. "Nacre: Durable, Secure and Energy-efficient Non-volatile Memory Utilizing Data Versioning," with M. Khavari-Tavana and Y. Fei, *IEEE Transactions on Emerging Technologies*, December 2017.
37. "UMH: A Hardware-based Unified Memory Hierarchy for Systems with Multiple Discrete GPUs," with A.K. Ziabari, Y. Sun, Y. Ma, D. Schaa, J.L. Abellan, R. Ubal, J. Kim, and A. Joshi, *ACM Transactions on Architecture and Code Optimization (TACO)*, 13(4), 2016, pp. 1-35.
38. "A Framework for Big Metabolomic Data Management and Analysis," with X. Li, L. Yu, Y. Yao, P. Wang, R. Giese, V. Yusa and A. Alshawabkeh, *International Journal on Advances in Software*, 9(1-2), 2016, pp. 50-61.
39. "Diffraction Pattern Simulation of Cellulose Fibrils using Distributed and Quantized Pair Distance," with Y. Zhang, H. Inouye, M. Crowley, L. Yu, and L. Makowski, *Journal of Applied Crystallography*, 49(6), 2016.
40. "A Framework for Studying New Approaches to Anomaly Detection," with E.N. Yolacan, *International Journal of Information Security Science*, 5(2), 2016, pp. 39-50.
41. "Patterns of Temporal Scaling of Groundwater Level Fluctuation," with X. Yu, R. Ghasemizadeh, I.Y. Padilla and A. Alshawabkeh, *Journal of Hydrology*, vol. 536, 2016, pp. 485-495.
42. "Using Benchmarks for Radiation Testing of Microprocessors and FPGAs," with H. Quinn, W.J. Robinson, P. Rech, M. Aquirre, A. Barnard, M. Desogus, L. Entrena, M. Garcia-Valderas, S.M. Guertin, F. Lima Kastensmidt, B.T. Kiddie, A. Sanchez-Clemente, M. Souza Reorda, L. Sterpone and M. Wirthlin, *IEEE Transactions on Nuclear Science*, Vol. 62, No. 6, 2015, pp. 2547-2554.
43. "Spatiotemporal Changes of CVOC Concentrations in Karst Aquifers: Analysis of Three Decades of Data from Puerto Rico," with X. Yu, R. Ghasemizadeh, I. Padilla, C. Irizarry and A. Alshawabkeh, *Science of the Total Environment*, 2015, pp. 1-10.
44. "A Reuse-Based Refresh Policy for Energy-Aware eDRAM Caches," with A. Valero, S. Petit, J. Sahuquillo and J. Duato, *Microprocessors and Microsystems*, Elsevier, 39(1), 2015, pp. 37-48.
45. "Analyzing Power Efficiency of Optimization Techniques and Algorithms Design Methods for Applications on Heterogeneous Platforms," with Y. Ukidave, A. Kavyan Ziabari, P. Mistry and G. Schirner, *International Journal of High Performance Computing Applications*, 28(2), 2014.
46. "Harnessing the Power of GPUs to Speed Up Feature Selection for Outlier Detection," with F. Azmandian, A. Yilmazer, J. Dy and J.A. Aslam, *Journal of Computer Science and Technology*, 29(3):408-422, 2014.

47. "Aggressive Value Prediction on a GPU," with E. Sun, *International Journal of Parallel Processing*, Springer, 42(1):30-48, 2014.
48. "Accelerated Mesh-based Monte Carlo Methods for Modern CPU Architectures," with Q. Fang, *Biomedical Optics Express*, 3(12):3223-3230, 2012.
49. "Local Kernel Density Ratio-Based Feature Selection," with F. Azmandian, J. Dy, and J.A. Aslam, *Journal of Machine Learning Research*, Vol. 25, pp. 49-64, 2012.
50. "A Sequentially Consistent Multiprocessor Architecture for Out-of-Order Retirement of Instructions," with R. Ubal, J. Sahuquillo, S. Petit and P. Lopez, *IEEE Transactions on Parallel and Distributed Systems*, 23(8):1361-1368, 2012.
51. "Guest Editor's Introduction: Special Issue on High-Performance Computing with Accelerators," with D. Bader and V. Kindratenko, *IEEE Transactions on Parallel and Distributed Systems*, 22(1):3-6, January 2011.
52. "Virtual Machine Monitor-based Lightweight Intrusion Detection," with F. Azmandian, M. Moffie, M. Alshawabkeh, J. Dy and J. Aslam, *ACM Operating Systems Reviews*, July 2011.
53. "Data Structures and Transformations for Physically Based Simulations on a GPU," with P. Mistry, D. Schaa, B. Jang, A. Dvornik and D. Meglan, *High Performance Computing for Computational Science*, Lecture Notes in Computer Science, No. 6449, Springer 2011.
54. "Exploiting Memory Access Patterns to Improve Memory Performance in Data Parallel Architectures," with B. Jang, D. Schaa and P. Mistry, *IEEE Transactions on Parallel and Distributed Computing*, 22(1): 105-118, 2011.
55. "Design and Simulation of Self-Biased Circulators in the Ultra High Frequency Band," with J. Wang, A. Geiler, P. Mistry, V. Harris and C. Vittoria, *Journal of Magnetism and Magnetic Materials*, 324(6): 991-994, 2011.
56. "Accelerating an Imaging Spectroscopy Algorithm for Submerged Marine Environments Using Graphics Processing Units," with J. Goodman and D. Schaa, *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing*, 4(3): 669-676, 2011.
57. "Adventures in Desktop Supercomputing," *Journal of Computing Sciences in Colleges*, 26(2):172, 2010.
58. "AGAMOS: A Graph-Based Approach to Modulo Scheduling for Clustered Microarchitecture," with A. Aleta, J.M. Codina and A. Gonzalez, *IEEE Transactions on Computers*, 58(6):770-783, 2009.
59. "Special issue: General-purpose Processing Using Graphics Processing Units," with M. Leeser, *Journal of Parallel and Distributed Computing*, 68(10): 1305-1306, 2008.
60. "Soft Error Susceptibility Analysis of SRAM-Based FPGAs in High-Performance Information Systems," with G. Asadi, V. Sridharan, T. Tahoori and K. Granlund, *IEEE Transactions on Nuclear Science (TNS)*, 54(6): 2714-2726, Dec. 2007.

61. "Characterization of File IO Activity for SPEC CPU2006," with D. Ye and J. Ray, *Special Issue of ACM SIGARCH Computer Architecture News: SPEC CPU2006 Analysis*, 35(1):112-117, 2007.
62. "Towards the Development of an Error Checker for Radiotherapy Treatment Plans: A Preliminary Study," with F. Azmandian and S. Jiang, *Physics in Medicine and Biology*, 52/2007, pp. 6711-6524.
63. "Addressing a Workload Characterization Study of the Design of Consistency Protocols," with S. Petit, J. Sahuquillo and A. Pont, *Journal of Supercomputing*, Springer-Verlag, 38(1): 49-72, 2006.
64. "Reducing Data Cache Susceptibility to Soft Errors," with V. Sridharan, G. Asadi and M. Tahoori, *IEEE Transactions on Dependable and Secure Computing*, 3(4): 353-364, 2006.
65. "An Adjustable Linear Time Parallel Algorithm for Maximum Weight Bipartite Matching," with M. Fayyazi and W. Meleis, *Information Processing Letters*, Elsevier, 97(5): 185-190, 2006.
66. "Power-Aware External Bus Arbitration for System-on-Chip Embedded Systems," with K. Ning, *Transactions on High-Performance Embedded Architectures and Compilers*, Springer-Verlag, 1(1):94-113, 2006.
67. "Bus Power Estimation and Power-Efficient Bus Arbitration for System-on-a-Chip Embedded Systems," with K. Ning, *Lecture Notes in Computer Science*, Springer-Verlag, Vol. 3471, pp. 95-106, 2005.
68. "Removing Communications in Clustered Microarchitectures Through Instruction Replication," with A. Aleta, J.M. Codina and A. Gonzalez, *ACM Transactions on Architecture and Code Optimization (TACO)*, 1(2): 127-151, June 2004.
69. "A Finite State Model for Respiratory Motion Analysis in Image-guided Radiation Therapy," with H. Wu, S. Jiang, G. Sharpe, and B. Salzberg, *Journal of Physics in Medicine and Biology*, 49(23): 5357-5372, 2004.
70. "Developing Object-Oriented Parallel Iterative Methods," with C. Ouarraoui, *International Journal of High Performance Computing and Networking*, Vol. 1, Issue 1/2/3, 2004, pp. 85-90.
71. "Levo - A Scalable Processor With High IPC," with A. Uht, D. Morano and A. Khalafi, *Journal of Instruction Level Parallelism*, Vol. 5, August 2003, pp. 1-35.
72. "A Database System to Advance Subsurface Sensing and Imaging," with H. Wu, B. Norum and B. Salzberg, *Journal of Subsurface Sensing Technologies and Applications*, 4(4): 395-408, October 2003.
73. "Profile-Based Characterization and Tuning for Subsurface Sensing and Imaging Applications," with M. Ashouei, D. Jiang, W. Meleis, M. El-Shenawee M., E. Mizan, Y. Wang and C. Rappaport, *International Journal of Systems, Science and Technology*, September 2002, pp. 40-55.

74. "Electromagnetics Computations Using the MPI Parallel Implementation of the Steepest Descent Fast Multipole Method (SDFMM)," with M. El-Shenawee, C. Rappaport, D. Jiang and W. Meleis, *ACES Journal*, , 17(2): 112-122, July 2002.
75. "Introduction to the Special Section on High Performance Memory Systems," with H. Hadimioglu and F. Lombardi, *IEEE Transactions on Computers*, 50(11): 1103-1105, 2001.
76. "Welcome to the Opportunities of Binary Translation," with E. Altman and Y. Sheffer, *IEEE Computer*, special issue on Binary Translation, March 2000, pp. 40-46.
77. "Indirect Branch Prediction Using Data Compression Techniques," with J. Kalamatianos, *Journal of Instruction Level Parallelism*, (1), 1999, <http://www.jilp.org/vol1/index.html>.
78. "Analysis of Temporal-based Program Behavior for Improved Cache Performance," with J. Kalamatianos, A. Khalafi, and W. Meleis, Special Issue on Cache Memory, *IEEE Transactions on Computers*, 48(2): 168-175, 1999.
79. "VLSI Design in the 3rd Dimension," with S. Strickland, E. Ergin, and P. Zavracky, *Integration: The Journal of VLSI*, Elsevier, North-Holland, 25(1): 1-16, September 1998.
80. "Tracing and Characterization of NT-based System Workloads," with J. Casmira, and D. Hunter, *Digital Technical Journal*, 10(1): 6-21, December 1998.
81. "Program Remapping Using Estimated Profiles," with H. Hashemi, B. Calder, J. Kalamatianos and W. Meleis, *Digital Technical Journal*, 10(2), 1999.
82. "Branch-directed and Pointer-based Data Cache Prefetching," with Y. Liu and M. Dimitri, *Journal of Systems Architecture*, Vol. 45, 1999, pp. 1047-1073.
83. "Creating 3D Circuits Using Transferred Films," with P. Sailer, P. Singhal, J. Hopwood, P.M. Zavracky, K. Warner and P.P. Vu, *IEEE Circuits and Devices Magazine*, November 1997, pp. 27-30.
84. "Performance Analysis on a CC-NUMA Prototype," with L. Fong, D. Renfrew, K. Imming, and R. Booth, *IBM Journal of Research and Development, Special Issue on Performance Tools*, 41(3): 205-214, May 1997.
85. "Improving the Accuracy of History-Based Branch Prediction," with P. Emma, *IEEE Transactions on Computers*, 46(4): 469-472, April 1997.
86. "Modeling Cache Pollution," with J. Casmira, *International Journal of Modeling and Simulation*, 19(2): 132-138, May 1998.
87. "Real-Time Trace Generation," with O. LaMaire, W. White, P. Hennes, and W. Starke, *International Journal of Computer Simulation*, 6(1): 53-68, 1996.
88. "Issues in Trace-Driven Simulation," *Lecture Notes in Computer Science No. 729, Performance Evaluation of Computer and Communication Systems*, L. Donatiello and R. Nelson eds., Springer-Verlag, 1993, pp. 224-244.

89. “Contrasting Instruction-Fetch and Instruction-Decode Time Branch Prediction Mechanisms: Achieving Synergy Through Their Cooperation Operation,” with P. Emma, J. Knight, and T. Puzak, *EuroMicro Journal*, Vol. 35, September 1992, pp. 401-408, also appearing in *Proc. of EuroMicro 92 Software and Hardware Specification and Design*, September 1992.

Textbooks, Edited Books and Book Chapters:

1. “Accelerated Computing with HIP,” with Y. Sun and T. Baruah, December 2022, ISBN: 9798218107444.
2. “Proceedings of the IEEE International Symposium on Performance Analysis and System Software,” *IEEE ISPASS 2020*, with K. Shaw, 2020.
3. “NSF Workshop on Side Channel and Covert Channels in Computing Systems,” with G. Venkataramani, P. Schaumont, M. Prvulovic, S. Devadas, D. Ponomarev and G. Qu, *NSF Visioning Workshop Report*, August, 2018.
4. “Proceedings of the 15th ACM International Conference on Computing Frontiers,” with M. Pericas, *ACM Computing Frontiers*, Ischia, Italy, May 2018.
5. “GPGPU-11: Proceedings of the 11th Annual Workshop on General Purpose Processing with Graphics Processing Units,” with J. Cavazos and T. Baruah, *ACM Online Conference Proceedings*, Vienna, Austria February 2018.
6. “High-performance Monte Carlo Simulations for Photon Migration and Applications in Optical Brain Functional Imaging,” with F. N. Paravecino, L. Yu and Q. Fang, *Handbook of Large-scale Distributed Computing in Smart Healthcare*, March 2017.
7. “GPGPU-10: Proceedings of the 10th Annual Workshop on General Purpose Processing with Graphics Processing Units,” with J. Cavazos and S. Dong, *ACM Online Conference Proceedings*, February 2017.
8. “GPGPU-9: Proceedings of the 9th Annual Workshop on General Purpose Processing with Graphics Processing Units,” with J. Cavazos and Y. Sun, *ACM Online Conference Proceedings*, February 2016.
9. “Simulating HSA,” with S. Hung, T.B. Jablin, Y. Sun, and R. Ubal, a book chapter in *Heterogeneous System Architecture: Practical Applications for Industry*, 1st edition, Elsevier Nov. 2015.
10. “Computer Organization,” book chapter in *Encyclopedia of Computer Science and Technology*, with P. Mistry, Y. Ukidave, and Z. Chen, Chapter 28, Dec. 2016, pp. 1-14.
11. “GPGPU-8: Proceedings of the 8th Annual Workshop on General Purpose Processing with Graphics Processing Units,” with J. Cavazos and X. Gong, *ACM Online Conference Proceedings*, February 2015.
12. “Heterogeneous Computing with OpenCL 2.0,” with P. Mistry, D. Schaa and D.P. Zhang, *Morgan Kaufmann Publishers*, 3rd Edition, January 2015.
13. “Special Issue on Applications for the Heterogeneous Computing Era,” with J. Meng et al., *International Journal of High Performance Computing Applications*, 28(3) 2014.
14. “Fast Fourier Transform (FFT) on GPUs,” with Y. Ukidave and G. Schirner, *Numerical Computations with GPUs*, Springer International Publishing, pp. 339-361, 2014.

15. "Proceedings of the 12th Annual IEEE/ACM International Symposium on Code Generation and Optimization, CGO," *ACM Digital Library*, February 2014.
16. "GPGPU-7: Proceedings of the 7th Annual Workshop on General Purpose Processing with Graphics Processing Units," with J. Cavazos and X. Gong, *ACM Online Conference Proceedings*, March 2014.
17. "Heterogeneous Computing with OpenCL 1.2," with B. Gaster, L. Howes, P. Mistry and D. Schaa, *Morgan Kaufmann Publishers*, 2nd Edition, January 2013.
18. "GPGPU-6: Proceedings of the 6th Annual Workshop on General Purpose Processing with Graphics Processing Units," with J. Cavazos and X. Gong, *ACM Online Conference Proceedings*, 2013.
19. "Topic 16: GPU and Accelerators Computing," with A. Ramirez, D.S. Nikolopoulos and S. Matsuoka, *Proceedings of Europar*, 2012.
20. "Third Joint WOSP/SIPEW International Conference on Performance Engineering," with J. Rolia, L. John and D. Krishnamurthy, *ACM Digital Library*, April 2012.
21. "GPGPU-5: Proceedings of the 5th Annual Workshop on General Purpose Processing with Graphics Processing Units," with J. Cavazos and E. Sun, *ACM Online Conference Proceedings*, 2012.
22. "Heterogeneous Computing with OpenCL," with B. Gaster, L. Howes, P. Mistry and D. Schaa, *Morgan Kaufmann Publishers*, 1st Edition, August 2011.
23. "GPU Acceleration of Iterative Digital Breast Tomosynthesis," with D. Schaa, B. Brown, B. Jang, P. Mistry, R. Dominguez, R. Moore, and D.B. Koppans, *GPU Computing Gems*, Morgan Kaufmann, 2011, pp. 647-659
24. "Proceedings of the Fourth Workshop on General Purpose Processing on Graphics Processing Units," with J. Cavazos, *ACM Online Conference Proceedings*, March, 2011.
25. "Special Issue on High Performance Computing with Accelerators," with D.A. Bader and V. Kindratenko, *IEEE Transactions on Parallel and Distributed Systems*, 22(1), 2011, pp. 3-6.
26. "Computer Organization and Design: The Hardware/Software Interface," D.A. Patterson and J.L. Hennessy, 4th edition, contributed the problem set for Chapter 7 on Multicores, Multiprocessors and Clusters.
27. "Computer Organization and Design: The Hardware/Software Interface," D.A. Patterson and J.L. Hennessy, 5th edition, contributed updates to the problem set for Chapter 7 on Multicores, Multiprocessors and Clusters.
28. "Computer Performance Evaluation and Benchmarking," D. Kaeli and K. Sachs, editors, *Lecture Notes in Computer Science*, Vol. 5419, January 2009.
29. "General Purpose Computing on Graphics Processing Units," D. Kaeli and M. Leeser, guest editors, *Journal of Parallel and Distributed Computing*, Elsevier, October 2008.

30. "High Performance Embedded Architectures and Compilers," K. DeBosschere, D. Kaeli, P. Stentrom, D. Whalley and T. Ungerer, editors, *Springer Verlag*, January 2007.
31. "Recent Speculative Architectures," with D. Morano, a book chapter in "Speculative Execution in Modern Computer Architectures," *CRC Press*, D. Kaeli and P. Yew, editors, 2005.
32. "Speculative Execution in Modern Computer Architectures," *CRC Press*, co-editor with P. Yew, 2004.
33. "Microprogramming," a book chapter in *The Wiley Encyclopedia of Electronic and Electrical Engineering*, 3rd edition, edited by John Webster, *John Wiley*, 2004.
34. "High Performance Memory Systems," co-editor with H. Hadimioglu, J. Kuskin, A. Nanda and J. Torrellas, eds., *Springer Verlag*, New York, 2003, ISBN: 03870010X.
35. "Microprogramming," in *Encyclopedia of Life Sciences*, UNESCO, 2005.
36. "Computer Architecture," in *Encyclopedia of Life Sciences*, UNESCO, 2005.
37. "Microprogramming," a book chapter in *The Wiley Encyclopedia of Electronic and Electrical Engineering*, 2nd edition, edited by John Webster, *John Wiley*, 2001.
38. "Parameter Value Characterization of Windows NT-based Applications," with J. Kalamatianos, *Workload Characterization: Methodology and Case Studies*, IEEE Computer Society, 1999, pp.142-149.
39. "Profile-Tuned Heap Access," with E. Yardimci, in *High Performance Memory Systems*, Springer Verlag, New York, 2003, pp. 153-162.
40. "Digital Computer Architecture," in *The Computer Science and Engineering Handbook*, Allen Tucker, editor, *CRC Press*, June 2004.
41. "Microprogramming," a book chapter in *The Wiley Encyclopedia of Electronic and Electrical Engineering*, 1st edition, edited by John Webster, *John Wiley*, 1999.
42. "Proceedings of FTPDS'98," with D. Avresky, edited by J. Rolim, *Lecture Notes in Computer Science*, No. 1388, Springer-Verlag, April 1998, pp. 564-789.
43. "Fault-Tolerant Parallel and Distributed Systems," co-edited with D. Avresky, *Kluwer Academic Press*, 1998.
44. "Digital Computer Architecture," a book chapter in *The Computer Science and Engineering Handbook*, edited by A.B. Tucker, *CRC Handbook*, 1997, pp. 412-425.
45. "The DLX Instruction Set Architecture Handbook," with P.M. Sailer, *Morgan Kaufmann Publishing*, San Francisco, CA. 1996.
46. *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications, PDPTA'96*, Volumes 1, 2 and 3, co-editor with H.R. Arabnia, B.J. d-Auriol, T. Hazra, R.A. Olsson, Y. Pan, and R. Pande, August 1996.

Conference Publications:

1. “MaxK-GNN: Towards Theoretical Speed Limits for Accelerating Graph Neural Networks,” with H. Peng, X. Xie, K. Shivdikar, MDA Hasan, J. Zhao, S. Hung, O. Khan and C. Ding, *ACM International Conference on Architectural Support for Programming Languages and Operating Systems*, to appear, 2024.
2. “Energy-Aware Tile Size Selection for Affine Programs on GPUs,” with M. Jayaweera, M. Kong and Y. Wang, *IEEE/ACM International Symposium on Code Generation and Optimization*, to appear, 2024.
3. “AXI4MLIR: User-Driven Automatic Host Code Generation for Custom AXI-Based Accelerators,” with N. Agostini, J. Haris, P. Gibson, M. Jayaweera, N. Rubin, A. Tumeo, J. Abellan and J. Cano, *IEEE/ACM International Symposium on Code Generation and Optimization*, to appear, 2024.
4. “Scalability Limitations of Processing-in-Memory Using Real System Evaluations,” with G. Jonaton, H. Cho, H. Son, W. Xiangyu, N. Livesay, E. Mora, K. Shivdikar, J. Abellan, A. Joshi and J. Kim, *ACM SIGMETRICS - Special Interest Group on Performance Evaluation*, to appear, 2024.
5. “GME: GPU-based Microarchitectural Extensions to Accelerate Homomorphic Encryption,” with K. Shivdikar, Y. Bao, R. Agrawal, M. Shen, G. Jonaton, E. Mora, A. Ingare, N. Livesay, J.L. Abellan, J. Kim and A. Joshi, *56th IEEE/ACM International Symposium on Microarchitecture*, Oct. 2023, pp. 670-684, <https://doi.org/10.1145.3613424.3614279>.
6. “Thought Bubbles: A Proxy Into Players’ Mental Model Development,” with O. Mhaddesi, J. Griffin, O. Ergun, S. Marsella and C. Harteveld, *ACM CHI Conference on Human Factors in Computing Systems (CHI)*, April 2023, pp. 1-21, <https://doi.org/10/1145/3544548.3581570>.
7. “An MLIR-based Compiler Flow for System Level Design and Hardware Acceleration,” with N. Bohm Agostini, S. Curzel, V. Amalya, C. Tan, M. Minutoli, V.G. Castellana, J. Manzano and A. Tumeo, *ACM International Conference on Computer-Aided Design*, Oct. 2022, pp. 1-9, <https://doi.org/10.1145/3508352.3549424>.
8. “NaviSim: A Highly Accurate GPU Simulator for AMD RDNA GPUs,” with Y. Bao, Y. Sun, Z. Feric, M.T. Shen, M. Weston, J.L. Abellan, T. Baruah, J. Kim and A. Joshi, *31st ACM International Conference on Parallel Architecture and Compilation Techniques*, Oct. 2022, pp. 333-345, <https://doi.org/10.1145/3559009.3569666>.
9. “Accelerating Polynomial Multiplication for Homomorphic Encryption on GPUs,” with K. Shivdikar, G. Jonatan, E. Mora, N. Livesay, R. Agrawal, A. Joshi, J.L. Abellan and J. Kim, *IEEE International Symposium on Secure and Private Execution Environment Design (SEED)*, Sept. 2022, DOI: <https://ieeexplore.ieee.org/document/9935033>.
10. “A High-Performance Computing GNSS-aware Path Planning Algorithm for Safe Urban Flight Operations,” with J. Gutierrez, N. Neogi and E. Dill, *AIAA Aviation Forum*, June 2022, <https://doi.org/10.2514/6.2022-3461>.

11. "Hardware/Software Co-Design of Edge DNN Accelerators with TFLite," with J. Haris, P. Gibson, J. Cano and N. Bohm Agostini, *18th International Summer School on Advanced Computer Architecture and Compilation for High-Performance Embedded Systems*, July 2022, <https://www.dcs.gla.ac.uk/josecr/pub/>.
12. "SODA-OPT: An MLIR based Flow for Co-Design and High Level Synthesis," with N. Bohm Agostini, Cuzel and A. Tumeo, *ACM International Conference on Computing Frontiers*, pp. 201-202, 2022, DOI:10.1145/2528416.3539866.
13. "Performance and Accuracy Assesment of Line Marching Algorithm Computations Utilizing GPUs Within A Predictive GNSS Quality of Service," with J. Guiterrez, E. Dill and P. Closas, AIAA, Dec. 2022, <https://doi.org/10.2514/6.2022-0029>.
14. "To Trust or to Stockpile: Moduling Human-Simulation Interaction in Supply Chain Shortages," with O. Mohaddesi, J. Griffin, O. Ergun, S. Marsella and C. Harteveld, *ACM CHI Conference on Human Factors in Computing Systems*, 2022, DOI: 10.1145/3491102.3502089.
15. "GPU Overdrive Fault Attacks on Neural Networks," with M. Sabbagh and Y. Fei, *IEEE/ACM International Conference on Computer-Aided Design*, 2021, Nov. DOI:10.1109/NAS51552.2021.
16. "SODA-OPT: System-level Deign in MLIR for HLS," with N. Bohm Agostini and A. Tumeo, *IEEE/ACM International Conference for High Performance Computing, Networking, Storage and Analysis*, 2021, Research Poster Session.
17. "A Content-Aware Learning Cache for Storage Systems," with M. Kachmar, *Proc. of the 15th IEEE International Conference on Networking, Architecture and Storage (NAS)*, 2021, DOI:10.1109/NAS51552.2021.
18. "A Secure and Reusable Software Architecture for Supporting Online Data Harmonization," with Z. Feric, N. Bohm Agostini, D. Beece, A.J. Signes-Pastor, Y. Halchenko, D. Watkins, D. MacKenzie, M. Karagas, J. Manjouridis and A. Alshawabkeh, *8th International Workshop on Big Data Analytic Technology for Bioinformatics and Health Informatics*, 2021, DOI:10.1109/BigData525589.2021.9671538.
19. "SECDA: Efficient Hardware/Software Co-Design of FPGA-based DNN Accelerators for Edge Inference," with J. Haris, P. Gibson, J. Cano and N. Bohm Agostini, *International Symposium on Computer Architecture and High Performance Computing*, 2021, arXiv:2110.00478.
20. "JAXED: Reverse Engineering DNN Architectures Leveraging JIT GEMM Libraries," with M. Jayaweera, K. Shivdikar and Y. Wang, *Proc. of IEEE Symposium on Secure and Private Execution Environment Design (SEED)*, 2021, pp. 189-202.
21. "Achieving On-Mobile Real-Time Super Resolution with Neural Architecture and Pruning Search," with Z. Zhang, Y. Gong, P. Zhao, G. Yuan, W. Niu, Y. Wu, T. Zhang, M. Jayaweera, B. Ren, X. Lin and Y. Wang, *Proc. of IEEE/CVF International Conference on Computer Vision*, 2021, pp. 4821-4831.
22. "Overdrive Fault Attacks on GPU," with M. Sabbagh and Y. Fei, *Proc. of the 51st IEEE/IFIP International Conference on Dependable Systems*, 2021, pp. 68-69.

23. "Secure Speculative Execution via RISC-V Open Hardware Design," with M. Sabbagh and Y. Fei, *Proc. of the 5th Workshop on Computer Architecture Research with RISC-V (CARRV)*, 2021.
24. "Daisen: A Framework for Visualizing Detailed GPU Execution," with Y. Sun, Y. Zhang, A. Mosallaei, C. Shah, M.D. Shah and C. Dunne, *Proc. of EuroVis: 23rd EG Conference on Visualization*, 2021.
25. "A Novel GPU Overdrive Fault Attack," with M. Sabbagh and Y. Fei, *Proc. of the 17th Workshop on Silicon Errors in Logic - System Effects (SELSE)*, 2021.
26. "GNNMark: A Benchmark Suite to Characterize Graph Neural Network Training on GPUs," with T. Baruah, K. Shivdikar, S. Dong, Y. Sun, S. Mojumder, K. Jung, J.L. Abellan, Y. Ukiave, A. Joshi and J. Kim, *Proc. of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2021, pp. 13-23.
27. "Performance Evaluation and Improvement of Real-time Computer Vision Applications for Edge Computing Devices," with J. Gutierrez and N. Bohm Agostini, *Proc. of the Workshop on Challenges in Performance Methods for Software Development*, 2021, pp. 139-144.
28. "Trident: A Hybrid Correlation-Collision GPU Cache Timing Attack for AES Key Recovery," with J. Ahn, C. Jin, J. Kim, M. Rhu, Y. Fei and J. Kim, *Proc. of the 27th International Symposium on High-Performance Computer Architecture*, March 2021, pp. 332-344.
29. "ArmorAll: Compiler-based Resilience Targeting GPU Applications," with C. Kalra, F. Previlon and N. Rubin, *Proc. of the High-Performance Embedded Architecture and Compilation*, Jan. 2021.
30. "Griffin: Hardware-Software Support for Efficient Page Migration in Multi-GPU Systems," with T. Baruah, Y. Sun, A.T. Dincer, S. Mojumder, J. Abellan, Y. Ukiave, A. Joshi, N. Rubin and J. Kim, *Boston-Area Computer Architecture Workshop* Jan. 2021.
31. "Using Undersampling with Ensemble Learning to Identify Factors Contributing to Preterm Birth," with S. Dong, Z. Feric, C. Wu and J. Dy, *Proc. of the IEEE International Conference on Machine Learning and Applications*, 2020, pp. 759-764.
32. "Introducing Gamettes: A Playful Approach for Capturing Decision-Making for Information Behavior Models," with O. Mohaddesi, Y. Sun, R. Azghandi, R. Doroudi, S. Snodgrass, O. Ergun, J. Griffin and S. Marsella, *Proc. of the Conference on Computer-Human Interaction*, April 2020, pp. 1-13.
33. "Associating Exposures to Adverse Health Outcomes Using Decision Trees," with A. Purandar, H. Yap, Z. Feric, M. Powers and J. Dy, *Proc. of the IEEE MIT Undergraduate Research Conference*, Oct., 2020.
34. "The Path to Multi-GPU Computing," D. Kaeli, *Proc. of the 13th Annual Workshop on General Purpose Processing Using Graphics Processing Units*, Feb. 2020.

35. "A Smart Background Scheduler for Storage Systems," with M. Kachmar, *IEEE Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems*, 2020, pp. 1-8.
36. "Valkyre: Leveraging Inter-TLB Locality to Enhance GPU Performance," with T. Baruah, Y. Sun, S. Mojumder, J. Abellan, A. Joshi, N. Rubin and J. Kim, *Proc. of the International Conference on Parallel Architectures and Compilation Techniques*, 2000, pp. 455-566.
37. "Design Space Exploration of Accelerators and End-to-end DNN Evaluation with TFLITE-SOC," with N.B. Agostini, S. Dong, E. Karimi, M. Torrents, J. Cano, J.L. Abellan and D. Kaeli, *Proc. of the IEEE 32nd Symposium on Computer Architecture and High Performance Computing*, Vol. 32, Sept., 2020, pp. 1-10.
38. "A Novel GPU Overdrive Fault Attack," with M. Sabbagh and Y. Fei, *Proc. of the ACM/IEEE Design Automation Conference*, June, 2020.
39. "Hardware/Software Obfuscation Against Timing Side-channel Attack on a GPU," with E. Karimi and Y. Fei, *Proc. of IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2020, pp. 121-131.
40. "Machine Learning Kernel Divergence-based de Novo Sampling Size Optimization for Environmental Applications: A Case Study of Single-Cell Raman Spectroscopic Phenotyping of EBPR," with C. Li, G. Wu, D. Wang, J. Dy and A. Gu, *ACS National Meeting and Expo*, 2020.
41. "Griffin: Hardware-Software Support for Efficient Page Migration in Multi-GPU Systems," with T. Baruah, Y. Sun, A. Dincer, S. Mojumder, J. Abellan, Y. Ukidave, A. Joshi, N. Rubin and J. Kim, *Proc. of the 26th IEEE International Symposium on High Performance Computer Architecture*, 2020, pp. 596-609.
42. "Vega: A Computer Vision Processing Enhancement Framework with Graph-based Acceleration," with J. Gutierrez and S. Dong, *Hawaii International Conference on System Sciences, Systems and Applications of Video Analytics Track*, January, 2020, pp. 1-10.
43. "Discovering Programmer Intention Behind Written Source Code," with G. Sznaier-Camps and N. Bohm-Agostini, *International Conference on Machine Learning and Applications*, December, 2019.
44. "Sample Size Assessment via Kernel Divergence: A Case Study with Single-cell Raman Spectroscopic Datasets," with G. Li, C. Wu, D. Wang, J.G. Dy and A.Z. Gu, *Proc. of the 8th IWA Microbial Ecology and Water Engineering Specialist Conference*, November, 2019.
45. "A Comprehensive Evaluation of the Effects of Input Data on the Resilience of GPU Applications," with F. Previlon, C. Kalra and P. Rech, *32nd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, Oct. 2019, pp. 1-6.
46. "Using Machine Learning for Data Imputation to Support Environmental Health Studies in Northern Puerto Rico," with A. Aboelela and Z. Feric, *Proc. of the IEEE MIT Undergraduate Research Technology Conference*, August, 2019.

47. "Machine Learning-based Malware Detection using Recurrent Neural Networks," with M. Oyler-Castrillo, N. Bohm-Agostini and G. Sznaier, *Proc. of the IEEE MIT Undergraduate Research Technology Conference*, August, 2019.
48. "MGPU-Sim: Enabling Multi-GPU Performance Modeling and Optimization," with Y. Sun, T. Baruah, S. Mojumder, S. Dong, X. Gong, S. Treadway, Y. Bao, S. Hance, C. McCardwell, V. Zhao, H. Barclay, A. Kavyan Ziabari, Z. Chen, R. Ubal, J. Abelln, J. Kim and A. Joshi, *Proc. of the 46th ACM/IEEE International Conference on Computer Architecture*, June, 2019, pp. 197-209.
49. "GIPSim: Low-level Power Modeling for Resiliency from Side Channel Attacks on GPUs," with S. Mukherjee and Y. Fei, *Proc. of the IEEE Symposium on Security and Privacy*, May 2019, Poster paper.
50. "Exploiting Adaptive Data Compression to Improve Performance and Energy-efficiency of Compute Workloads in Multi-GPU Systems," with M. Khavari Tavana, Y. Sun, and N. Bohm-Agostini, *Proc. of the 33rd IEEE International Parallel and Distributed Processing Symposium*, May 2019, pp. 665-674.
51. "PCFI: Program Counter Guided Fault Injection for Accelerating GPU Reliability Assessment," with F. Previlon, C. Kalra and D. Tiwari, *IEEE Design Automation and Test in Europe*, March 2019, pp. 308-311.
52. "Evaluation of Volta-based DGX-1 System Using DNN Workloads," with S.A. Mojumder, M.S. Louis, Y. Sun, A.K. Ziabari, J.L. Abellan, J. Kim and A. Joshi, *Proc. of the Boston Area Computer Architecture Workshop*, January 2019.
53. "An Integrated Simulation Framework for Examining Resiliency in Pharmaceutical Drug Supply Chain Considering Human Behaviors Component," with R. Doroudi, R. Azghandi, Z. Feric, O. Mahaddesi, P. Sequeira, Y. Sun, J. Griffin, O. Ergun, C. Harteveld and S. Marsella, *Winter Simulation Conference*, Dec. 2018, pp. 88-99.
54. "A Hybrid Approach to Identifying Key Factors in Environmental Health Studies," with S. Dong, Z. Feric, L. Yu, J. Meeker, I. Padilla, J. Cordero, C. Velez Vega, Z. Rosario and A. Alshwabkeh, *5th Workshop on Big Data Analytic Technology for Bioinformatics and Health Informatics (KDDBHI)*, Dec. 2018, pp. 2855-2862.
55. "PRISM: Predicting Resilience of GPU Applications Using Statistical Methods," with C. Kalra, F. Previlon, X. Li and N. Rubin, *ACM International Conference for High Performance Computing, Networking, Storage and Analysis*, No. 69, Nov. 2018, pp. 1-14.
56. "An Efficient Data Management Framework for Puerto Rico Testsite for Exploring Contamination Threats (PROTECT), with S. Dong, Z. Feric, L. Yu, J. Meeker, I. Padilla, J. Cordero, C. Velez Vega, Z. Rosario and A. Alshwabkeh, *IEEE Big Data Conference*, Nov. 2018, pp. 5316-5318.

57. "Peachy Parallel Assignments (EduHPC 2018)," with E. Ayguade, L. Alvarez, F. Banchelli, M. Burtscher, A. Gonzalez-Escribano, J. Gutierrez, D.A. Joiner, F. Previlon, E. Rodriguez-Gutierrez and D.P. Bunde, *Proc. of the IEEE/ACM Workshop on Education for High Performance Computing (EduHPC)*, Nov. 2018, pp. 78-85.
58. "Employing Student Retention Strategies for an Introductory GPU Programming Course," with J. Gutierrez and F. Previlon, *Proceedings of the Workshop on High Performance Computing (EduHPC)*, Nov. 2018.
59. "Defensive Dropout for Hardening Deep Neural Networks under Adversarial Attacks," with S. Wang, X. Wang, P. Zhao, W. Wen, P. Chin and X. Lin, *ACM 37th International Conference on Computer Aided Design*, Nov. 2018, pp. 71:1-78:8.
60. "Effective Simple-Power Analysis Attacks of Elliptic Curve Cryptography on Embedded Systems," with C. Luo and Y. Fei, *ACM 37th International Conference on Computer Aided Design*, Nov. 2018, pp. 115:1-115:8.
61. "GPU Acceleration of RSA is Vulnerable to Side-channel Timing Attacks," with C. Luo and Y. Fei, *ACM 37th International Conference on Computer Aided Design*, Nov. 2018, pp. 113:1-113:8.
62. "A Timing Side Channel Attack on a Mobile GPU," with E. Karimi, Z.H. Jiang and Y. Fei, *IEEE International Conference on Computer Design*, October 2018, pp. 67-74.
63. "Evaluating the Resilience of Parallel Applications," with M. Wilkening, F. Previlon, S. Gurumruthi, S. Raasch and V. Sridharan, *IEEE 31st International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, Oct. 2018, pp. 1-6.
64. "Profiling DNN Workloads on a Volta-based DGX-1 System," with S.A. Mojumder, M.S. Louis, Y. Sun, A.K. Ziabari, J.L. Abellan and J. Kim, *IEEE International Symposium on Workload Characterization*, Oct. 2018, pp. 122-133.
65. "Iterative Kernel Dimension Alternative Clustering on GPUs," with X. Li, C. Wu, S. Dong and J. Dy, *International Symposium on Foundations and Applications of Big Data Analytics*, August 2018, pp. 885-892.
66. "Intra-Cluster Coalescing and CTA Scheduling to Reduce GPU NoC Pressure," with L. Wang, X. Zhao and L. Eeckhout, *IEEE International Parallel and Distributed Processing Symposium*, May, 2018, pp. 990-999.
67. "Evaluating Performance Tradeoffs on the Radeon Open Computing Systems," with Y. Sun, S. Mukherjee, T. Baruah, S. Dong, J. Gutierrez and P. Mohan, *IEEE International Symposium on Performance Analysis and Systems Software*, April 2018, pp. 209-218.
68. "Iterative Spectral Method for Alternative Clustering," with C. Wu, S. Ioannidis, M. Sznaiier, X. Li and J. Dy, *International Conference on Artificial Intelligence and Statistics*, March 2018, pp. 115-123.

69. "Evaluating the Impact of Execution Parameters on Program Vulnerability in GPU Applications," with F. Previlon, C. Kalra, and P. Rech, *IEEE Design Automation and Test in Europe*, March 2018, pp. 809-814.
70. "Airavat: Improving Energy Efficiency of Heterogeneous Applications," with T. Baruah, Y. Sun, S. Dong, and N. Rubin, *IEEE Design Automation and Test in Europe*, March 2018, pp. 731-736.
71. "Characterizing the Microarchitectural Implications of a Convolution Neural Network (CNN) on GPUs," with S. Dong, X. Gong, Y. Sun and T. Baruah, *ACM International Conference on Performance Engineering*, **Best Paper Award**, April 2018, pp. 96-106.
72. "Comparing HPC Application Kernel Application Vulnerability Using LLFI-GPU," with B. Egbantan and F. Previlon, *Boston Area Computer Architecture Workshop*, Jan. 2018.
73. "Speeding up DNNs Using HPL-based Fine-grained Tiling for Distributed Multi-GPU Training," with K. Shivdikar and K. Paneri, *Boston Area Computer Architecture Research Workshop*, Jan. 2018.
74. "Nacre: Durable, Secure and Energy-efficient Non-volatile Memory Utilizing Data Versioning," with M. Khavari-Tavana and Y. Fei, *IEEE International Conference on Computer Design*, **Best Paper Award**, Nov. 2017.
75. "On the Efficacy of ECC and the Benefits of FinFET Transistor Layout in GPU Reliability," with R.P. Luncardi, F. Previlon and P. Rech, *Radiation Effects on Components and Systems*, 2017.
76. "Moka: Model-based Concurrent Kernel Analysis," with L. Yu, X. Gong, Y. Sun, Q. Fang and N. Rubin, *IEEE International Symposium on Workload Characterization*, Oct. 2017, 197-206.
77. "Hardware Support for Scratchpad Memory Transactions on GPU Architectures," with A. Villega, R.A. Asenjo, A. Navarro, O. Plata and R. Ubal, *European Conference on Parallel Processing*, Aug. 2017, pp. 273-286
78. "Exploring the Potential for Collaborative Data Compression and Hard-error Tolerance in PCM Memories," with A. Jadidi, M. Arjomand, M.K. Tavan, M.T. Kandemir and C.R. Das, *47th Annual IEEE/IFIP Dependable Systems and Networks (DSN)*, June, 2017, pp. 85-96.
79. "Exploiting Nested Parallelism to Accelerate Parallel Recursive Graph Algorithms," with F. Nina-Paravecino, J. Gutierrez, N. Rubin and Q. Fang, *International Workshop on Architecture for Graph Processing*, 2017.
80. "Multi2Sim Kepler: A Detailed Architectural GPU Simulator," with X. Gong and R. Ubal, *IEEE International Symposium on Performance Analysis and Systems Software*, May, 2017, pp. 269-278.
81. "A Novel Side-channel Timing Attack on GPUs," with J.H. Jiang and Y. Fei, *27th ACM Great Lakes Symposium on VLSI*, May, 2017, pp. 167-172.

82. "Evaluating the Effects of Input Parameters on Program Vulnerability on GPU Applications," with F. Previlon and P. Rech, *13th Workshop on Silicon Errors in Logic - System Effects*, March 2017.
83. "DNNMark: A Deep Neural Network Benchmark Suite for GPUs," *10th Workshop on General Purpose Processing on GPUs*, Feb. 2017, pp. 62-72.
84. "TwinKernels: An Execution Model to Improve GPU Hardware Scheduling at Compile Time," with X. Gong, Z. Chen, A.K. Ziabari and R. Ubal, *Proc. of the IEEE/ACM International Symposium on Code Generation and Optimization*, March 2017, pp. 39-49.
85. "Live Together or Die Alone: Block Cooperation to Extend Lifetime of Resistive Memories," with M. Tavana and A.K. Ziabari, *Proc. of IEEE/IFIP Design, Automation and Test in Europe (DATE)*, March 2017, pp. 1090-1103.
86. "REMAP: A Reliability/Endurance Mechanism for Advancing PCM," *ACM International Symposium on Memory Systems*, Oct. 2017, pp. 385-398.
87. "Side-Channel Analysis on the ARM Cortex A9 Microprocessor," with L. Liu, Z.H. Zang and Y. Fei, *Boston Area Computer Architecture Workshop*, Jan. 2017.
88. "21st Century Computer Architecture," with M.D. Hill, S. Adve, L. Ceze, M.J. Irwin, M. Martonosi, J. Torrellas, T.F. Wenisch, D. Wood and K. Yelick, *A Computing Community Consortium (CCC) White Paper*, Sept. 2016, pp. 1-16.
89. "Hardware Thread Reordering to Boost OpenCL Throughput on FPGAs," with A. Momeni, H. Tabkhi and G. Schirner, *Proc. of the International Conference on Computer Design*, Oct 2016, pp. 257-264.
90. "Hetero-mark, A Benchmark Suite for CPU-GPU Collaborative Computing," with Y. Sun, X. Gong, A.K. Ziabari, L. Yu, S. Mukherjee, C. McCardwell and A. Villegas, *Proc. of the IEEE International Symposium on Workload Characterization*, Oct. 2016, pp. 1-10.
91. "Mystic: Predictive Scheduling for GPU-based Cloud Servers Using Machine Learning," with Y. Ukidave and X. Li, *Proc. of the IEEE Parallel and Distributed Processing Symposium*, May 2016, pp. 353-362.
92. "A Fast Level-Set Segmentation Algorithm for Image Processing Designed for Parallel Architectures," with J. Gutierrez and F. Nina-Paravecino, *Proc. of the 6th Workshop on Irregular Applications: Architectures and Algorithms*, Nov. 2016, pp. 66-69.
93. "Balancing Scalar and Vector Execution on GPU Architecture," with Z. Chen, *Proc. of the IEEE Parallel and Distributed Processing Symposium*, May 2016, pp 973-982.
94. "A Comprehensive Performance Analysis of HSA and OpenCL 2.0," with S. Mukherjee, Y. Sun, P. Blinzer and A. Kavyan Ziabari, *Proc. of the IEEE International Symposium on Performance Analysis, Software and Systems*, April 2016, pp. 183-193.
95. "Modeling Player Decisions in a Supply Chain Game," with Y. Sun, C. Liang, S. Sutherland and C. Harteveld, *IEEE Computational Intelligence and Games Conference*, Sept. 2016.

96. "Portable Performance for Monte Carlo Simulations of Photon Migration in 3D Turbid Media for Single and Multiple GPUs," with L. Yu, F. N. Paravecino and Q. Fang, *NVIDIA GPU Technology Conference*, March 2016.
97. "Performance Evaluation of Compiler-based Redundant Multithreading in an HSA Environment," with C. Kalra, D. Lowell, J. Kalamatianos and V. Sridharan, *Proc. of the 12th Workshop on Silicon Errors in Logic - System Effects*, March 2016.
98. "Evaluating the Resilience of Highly Parallel Applications," with M. Wilkening, F. Previlon and V. Sridharan, *Proc. of the 12th Workshop on Silicon Errors in Logic - System Effects*, March 2016.
99. "OpenCL-based Optimizations for Acceleration of Object Tracking on FPGAs and GPUs," with A. Momeni, H.T. Tabkhi and G. Schirner, *Proc. of the Workshop on Architectures and Systems for Real-time Mobile Vision Applications*, March 2016.
100. "A Complete Key Recovery Timing Attack on a GPU," with Z.H. Jiang and Y. Fei, *Proc. of the 22nd International Symposium on High Performance Computer Architecture*, March 2016, pp. 395-405.
101. "CLIP: An IP-based GPU Clustering Framework," with C. McCardwell, *Proc. of the Boston Area Computer Architecture Workshop*, Jan. 2016.
102. "Memory Characterization of Embedded Applications," with T. Gale, S. Hance, Y. Ukidave, C. Kalra and K. Sanghai, *Proc. of the Boston Area Computer Architecture Workshop*, Jan. 2016.
103. "Correlation Timing Attack on a GPU," with Z.H. Jiang and Y. Fei, *Proc. of the Boston Area Computer Architecture Workshop*, Jan. 2016.
104. "Exploring the Efficiency of the OpenCL Pipe Semantic on an FPGA," with A. Momeni, H. Tabkhi, Y. Ukidave and G. Schirner, *Proc. of the International Symposium on High-Efficient Accelerators and Reconfigurable Technologies - also appearing in SIGARCH Computer Architecture News*, June 2015, pp. 52-57.
105. "A Framework for Visualization of OpenCL Application Execution: A Tutorial," with A.K. Ziabari, R. Ubal Tena and D. Schaa, *Proceedings of the 3rd International Worksotp on OpenCL*, ACM, April 2015, pp. 1-22.
106. "The Use of Benchmarks for High-Reliability Systems," H.Quinn, W. Robinson, P. Rech, A. Barnard, M. Aquirre, M. Desogus, L. Entrena, M. Garcia-Valderas, S.M. Guertin, F. Lima Kastensmidt, B. Kiddie, A. Sanchez-Clement, M. Sonza Reorda, L. Sterpone and M. Wirthlin, *Los Alamos National Laboratory Technical Report*, LA-UR-15-22303, March, 2015.
107. "Performance of the NVIDIA Jetson TK1 in HPC," with Y. Ukidave, U. Gupta and K. Keville, *Proc. of IEEE International Conference on Cluster Computing*, Sept., 2015, pp. 533-534.

108. "Side-channel Power Analysis on GPU AES Implementation," *Proc. of the IEEE International Conference on Computer Design*, October 2015, pp. 281-288.
109. "Securing Virtualized Execution Environments through Machine Learning-based Intrusion Detection," with F. Azmandian, J.G. Dy and J.A. Aslam, *Proc. of the IEEE International Workshop on Machine Learning for Signal Processing*, Sept. 2015, pp. 1-6.
110. "Asymmetric NoC Architectures for GPU Systems," with A.K. Ziabari, J.L. Abellan, Y. Ma and A. Joshi, *Proceedings of the 9th IEEE/ACM Symposium on Networks on Chip*, Sept. 2015, pp. 1-8.
111. "Leveraging Silicon-Photonic NOC for Designing Scalable GPUs," with A.K. Ziabari, J.L. Abellan, R. Ubal, C. Chen. with A. Joshi, *Proceesings of the 29th ACM International Conference on Supercomputing*, June, 2015, pp. 273-282.
112. "Hardware Support for Local Memory Transactions on GPU Architectures," with A. Villegas, A. Navarro, R. Asenjo, and O. Plata, *Proc. of 10th SIGPLAN Workshop on Transactional Computing*, June 2015, pp. 1-9.
113. "Exploring the Features of OpenCL 2.0," with S. Mukherjee, X. Gong, L. Yu, C. McCardwell, Y. Ukidave, T. Dao, and F. Nina Paravecino, *Proceedings of the International Workshop on OpenCL (IWOCCL)*, May 2015.
114. "Field, Experimental, and Analytical Data on Large-scale HPC Systems and Evaluaton of the Implications for Exascale System Design," with N. DeBardeleben, S. Blanchard and P. Rech, *IEEE 33rd VLSI Test Symposium*, April 2015, pp. 1-2.
115. "Big Data Analysis on Puerto Rico Testsite for Exploring Contamination Threats," with X. Li, L. Yu, Y. Yao, P. Wang, and R. Giese, ALLDATA, April 2015, pp. 29-34.
116. "Spatiotemporal Change of CVOC Concentrations in Karst Aquifers: Analysis of Three Decades of Data from Puerto Rico," with X. Yu, R. Ghasemizadeh, I. Padilla, C. Irizarry and A. Alshawabkeh, *Science of the Total Environment*, No. 511, 2015, pp. 1-10.
117. "Side-Channel Analysis of MAC-Keccak Hardware Implemmentations," with P. Luo, Y. Fei, A.A. Ding and M. Leeser, *Proc. of the Fourth Workshop on Hardware and Architectural Support for Security and Privacy*, June 2015, pp. 1-8.
118. "Mahout on Heterogeneous Clusters using HadoopCL," with X. Li and M. Grossman, *Proc. of the 2nd Workshop on Parallel Programming for Analytics*, February, 2015, pp. 9-16.
119. "High Performance Computing of Fiber Scattering Simulation," with L. Yu, Y. Zhang, X. Gong, N. Roy and L. Makowski, *Proc. of GPGPU-8, Proc. of the 8th Workshop on General Purpose Processing with Graphics Processing Units*, February, 2015, pp. 90-98.
120. "Bridging Architecture and Programming for Throughput-Oriented Vision Processing," with A. Momeni, H. Tabkhi and G. Schirner, *FPGA 2015*, pp. 275.

121. "NUPAR: A Benchmark Suite for Modern GPU Architecture," with Y. Ukidave, F. Nina Paravecino, L. Yu, C. Kalra, A. Momemi, Z. Chen, N. Materise and B. Daley, *Proc. of the the 6th ACM International Conference of Performance Engineering*, Feb. 2015, pp. 253-264.
122. "Speech Recognition on Modern Graphics Processing Units," with L. Yu, J. Magrath, A. Pandey and M. Sears, *Proceedings of the 6th Boston Area Computer Architecture Workshop*, January, 2015.
123. "Image Segmentation Using Graph Analysis on GPUs," with E. Hovaniak and F. Nina-Paravecino, *Proceedings of the 6th Boston Area Computer Architecture Workshop*, January, 2015.
124. "Side Channel Attack on GPUs," with S. Mukherjee, C. Luo, C. Finnegan, and Y. Fei, *Proceedings of the 6th Boston Area Computer Architecture Workshop*, January, 2015.
125. "FIR Filtering and AES Encryption with OpenCL 2.0," with C. McCardwell, T. Dao and S. Mukherjee, *Proceedings of the 6th Boston Area Computer Architecture Workshop*, January, 2015.
126. "GPU-accelerated HMM for Speech Recognition," with L. Yu and Y. Ukidave, *Proc. of the 43rd International Conference on Parallel Processing Workshops*, 2014, pp. 395-402.
127. "Power Analysis Attack on Hardware Implementation of MAC-Keccak on FPGAs," with P. Luo, Y. Fei, X. Fang, A.A. Ding, and M. Leeser, *Proc. of the Conference on Reconfigurable Computing and FPGAs (ReConfig'14)*, Dec. 2014, pp. 854.
128. "Fast Simulation of X-ray Diffraction Patterns from Cellulose Fibrils using GPUs," with Y. Zhang, L. Yu and L. Makowski, *IEEE Northeast Bioengineering Conference*, 2014, pp. 1-2.
129. "Calculating Architectural Vulnerability Factors for Spatial Multi-Bit Transient Faults," with M. Wilkening, V. Sridharan, S. Gurusurthi, F. Previlon and S. Li, *Proc. of the 47th IEEE/ACM International Symposium on Microarchitecture*, Cambridge, England, Dec., 2014, pp. 293-305.
130. "Scalable Open-source Side-channel Evaluation Platform for Cryptographic Devices," with N. Shah, T. Swamy, H. Dimmig and Y. Fei, *Advanced Cyber Security Center Conference*, Nov. 2014, Best poster award.
131. "Runtime Support for Adaptive Spatial Partitioning and Inter-Kernel Communication on GPUs," with Y. Ukidave, C. Kalra, P. Mistry and D. Schaa, *Proc. of the 26th IEEE International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, Paris, France, 2014, pp. 168-175.
132. "System Call Anomaly Detection Using Multi-HMMs," with E. Yolacan and J.G. Dy, *Proc. of the 8th IEEE International Conference on Software Security and Reliability - Companion*, 2014, pp. 25-60.
133. "Accelerated Connected Component Labeling using CUDA Framework," with Fanny Paravecino Nina, *International Conference on Computer Vision and Graphics*, Springer International, Sept. 2014, pp. 502-509.

134. "Exploring the Heterogeneous Design Space for both Performance and Reliability," with R. Ubal, D. Schaa, X. Gong, Y. Ukidave, Z. Chen and G. Schirner, *Proceedings of the 51st Design Automation Conference*, June 2014, pp. 1-6.
135. "Scalable and Efficient Implementation of Correlation Power Analysis using Graphics Processing Units (GPUs)," with T. Swamy, N. Shah, P. Luo, and Y. Fei, *Hardware and Architectural Support for Security and Privacy*, June 2014, No. 10, pp. 1-8.
136. "A Parallel Clustering Algorithm for Placement," with A. Momeni and P. Mistry *International Symposium on Quality Electronic Design*, March 2014, pp. 349-356.
137. "Scalar Waving: Improving the Efficiency of SIMD Execution on GPUs," with A. Yilmazer and Z. Chen, *28th IEEE International Parallel and Distributed Processing Symposium*, April 2014, pp. 103-112.
138. "Performance Evaluation and Optimization Mechanisms for with Y. Ukidave and X. Gong, Inter-operable Graphics and Computation on GPUs," *Proceedings of GPGPU-7*, pg. 37-45, March 2014.
139. "Case Study - Puerto Rico Test Site for Exploring Contamination Threats," with J.F. Cordero, J.D. Meeker, T. Sheahan, I. Padilla, R. Giese, M.B. Silevitch, R. Loch-Caruso and A.N. Alshawabkeh, *Bridges*, Vol. 10, 2014, pp. 3553-3562.
140. "Datacenters as Controllable Load Resources in the Electricity Market," with R. Wang, N. Kandasamy and C. Nwankpa, *33rd International Conference on Distributed Computing Systems*, July 2013, pp. 176-185.
141. "Puerto Rico Testsite for Exploring Contamination Threats (PROTECT): An innovative approach to assessing and addressing preterm birth in Puerto Rico, " with L. Anzalota, J.D. Meeker, A. Alshawabkeh, P. Brown, C. Villez Vega, D. Cantonwine, L.O. River-Gonzalez, B. Jimenez and J. Cordero, *6th International Conference on Health Promoting Universities*, San Juan, PR, March 2013.
142. "Analyzing Optimization Techniques for Power Efficiency on Heterogeneous Platforms," with Y. Ukidave, *Proceeding of the 3rd Workshop on Accelerators and Hybrid Exascale Systems*, May 2013, pp. 1040-1049.
143. "Unstructured Control Flow in GPGPU," with R. Dominguez, *Multicore and GPU Programming Models, Languages and Compilers Workshop*, May 2013, pp. 1194-1202.
144. "Characterizing Scalar Opportunities in GPGPU Applications," with Z. Chen and N. Rubin, *IEEE International Symposium on Performance Analysis of Systems and Software*, April 2013, pp. 225-234.
145. "Quantifying the Energy Efficiency of FFTs on Heterogeneous Platforms," with Y. Ukidave, A Ziabari, and P. Mistry, *IEEE International Symposium on Performance Analysis of Systems and Software*, April 2013, pp. 235-244.

146. "HQL: A Scalable Synchronization Mechanism for GPUs," with A. Yilmazer, *28th IEEE International Parallel and Distributed Processing Symposium*, April 2013, pp. 475-486.
147. "Architecture-Independent Dynamic Information Flow Tracking," with R. Whelan and T. Leek, *ACM Compiler Construction*, March 2013, pp. 144-163.
148. "A Framework for Profiling and Performance Monitoring of Heterogeneous Applications," with P. Mistry, Y. Ukidave and D. Schaa, *6th Workshop on Programmability Issues for Heterogeneous Multicores (MULTIPROG'13)*, January 2013.
149. "Valar: A Benchmark Suite to Study the Dynamic Behavior of Heterogeneous Systems," with P. Mistry, Y. Ukidave, and D. Schaa, *GPGPU6*, March 2013, pp. 54-65.
150. "Dione: A Flexible Disk Monitoring and Analysis Framework," with J. Mankin, *The Symposium on Research in Attacks, Intrusions and Defenses (RAID-12)*, 2012, pp. 127-146.
151. "Algorithm Acceleration for Geospatial Analysis," with J. Goodman and M. Sellitto, *NVIDIA GTC*, May, 2012.
152. "Enabling Task-level Scheduling on Heterogeneous Platforms," with E. Sun, D. Schaa, R. Bagley and N. Rubin, *Proceedings of the 5th Annual Workshop on General Purpose Processing with Graphics Processing Units*, March, 2012, pp. 84-93.
153. "Selecting Feature to Intrinsically Enhance Outlier Detection," *NEML*, with F. Azmandian, J. Dy and J. Aslam, May 2012.
154. "Local Kernel Density Ratio-Based Feature Selection for Outlier Detection," with F. Azmandian, J. Dy and J. Aslam, *Proceedings of the Asian Conference on Machine Learning (ACML)*, Oct., 2012.
155. "Feature Weighting and Selection Using Hypothesis Margin of Boosting," with M. Alshwabkeh, J. Aslam, and J. Dy, *IEEE International Conference on Data Mining*, Dec., 2012, pp. 41-50.
156. "GPU-Accelerated Feature Selection for Outlier Detection Using the Local Kernel Density Ratio," with F. Azmandian, A. Yilmazer, J. Dy and J. Aslam, *IEEE International Conference on Data Mining*, Dec., 2012, pp. 51-60.
157. "Enhancing Boosting-based Algorithm for Intrusion Detection in Virtual Machine Environments," with M. Alshwabkeh, J. Dy, J. Aslam and D. Schaa, *Proceedings of the First International Workshop on Secure and Resilient Architectures and Systems*, Sept. 2012, pp. 13-18.
158. "Securing Cloud Storage Systems through a Virtual Machine Monitor," with F. Azmandian, J. Dy, J. Aslam and D. Schaa, *Proceedings of the First International Workshop on Secure and Resilient Architectures and Systems*, Sept. 2012, pp. 19-24.
159. "Statistical Fault Injection-based AVF Analysis of a GPU Architecture," with N. Farazmand, *IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE)*, 2012.

160. "Multi2Sim: A Simulation Framework for CPU-GPU Computing," with R. Ubal, B. Jang, P. Mistry and D. Schaa, *Proceedings of PACT*, 2012, pp. 335-344.
161. "Enabling task-level scheduling on heterogeneous platforms," with E. Sun, D. Schaa, R. Bagley and N. Rubin, *Proceedings of the 5th Annual Workshop on General Purpose Processing with Graphics Processing Units*, also appearing in *ACM Online Conference Proceedings Series*, 2012, pp. 84-93.
162. "The Convergence of HPC and Embedded Systems in Our Heterogeneous Computing Future," with D. Akodes, *Proc. of ICCD*, 2011, pp. 9-11.
163. "A Novel Feature Selection for Intrusion Detection in Virtual Machine Environments," with M. Alshawabkeh, J. Dy and J. Aslam, *Proc. of the 23rd International Conference on Tools with Artificial Intelligence*, 2011, pp. 879-881.
164. "Aggressive Value Prediction on GPUs," with E. Sun, *Proc. of the 23rd Int. Symposium on Computer Architecture and High Performance Computing*, Oct. 2011.
165. "Computational Model of Optical Scattering by Elastin in Lung," with T. Swedish, J. Robinson, M. Silva, A. Gouldstone and C. Dimarzio, *Proceedings of SPIE*, volume 7904, Feb. 2011.
166. "Workload Characterization at the Virtualization Layer," with F. Azmandian, *Proc. of 19th IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems*, July 2011.
167. "Developing Portable Profiling and Performance Analysis Tools for Heterogeneous Applications," with P. Mistry, D. Schaa, N. Rubin and R. Ubal, *AMD Fusion Summit*, 2011.
168. "Increasing Power/Performance Resource Efficiency on Virtualized Enterprise Servers," with E. Arzuaga, *Proceeding of the 2011 IEEE Computing Frontiers*, Ischia, Italy, May 2011.
169. "Analyzing Program Flow with a Many-kernel OpenCL Application," with P. Mistry, C. Gregg, N. Rubin and K. Hazelwood, *GPGPU-4 Proceedings of the 4th Workshop on General Purpose Processing on Graphics Processing Units*, ACM Conference Proceedings Series, April 2011.
170. "Caracal: Dynamic Translation of Runtime Environments for GPUs," with Rodrigo Dominguez and Dana Schaa, *GPGPU-4 Proceedings of the 4th Workshop on General Purpose Processing on Graphics Processing Units*, ACM Conference Proceedings Series, April 2011.
171. "Macroarchitecture: A Unifying Framework for Manycore Architecture Research," with B. Cordes and G. Schirner, *Proc. of the Workshop on MicroArchitectural Support for Virtualization, Data Center Computing and Clouds*, Dec. 2010.
172. "Interdisciplinary Three-Level Approach to Study Impact of Contamination on Public Health in Puerto Rico," with M.B. Silevitch, R. Giese, T. Sheahan, M. Nobrega, A. Alshawabkeh, J. F. Cordero, I. Padilla R.Loeh-Caruso, J. Meeker, *Proc. of Sixth International Congress on Environmental Geotechnics*, New Delhi, India, November, 2010.

173. "Case Study - Puerto Rico Test Site for Exploring Contamination Threats," *GeoCongress 2012 State of the Art and Practice of Geotechnical Engineering*, with J.F. Cordero, J.D. Meeker, T. Sheahan, I. Padilla, R. Giese, M.B. Silevitch, R. Loch-Caruso and A. Alshawabkeh, 2012, pp. 3553-3562.
174. "Out-of-Order Retirement of Instructions in Sequentially Consistent Multiprocessors," with R. Ubal, J. Sahuquillo, S. Petit, and P. Lopez, *IEEE International Conference on Computer Design*, 2010, pp. 1-8.
175. "Leveraging Graphical Processor Units for the Acceleration of an Imaging Spectrometry Algorithm in the Littoral Zone," with James Goodman, Dana Schaa and Ayse Yilmazer, *International Symposium on Spectral Sensing Research*, pp. 8, 2010
176. "Accelerating a Hyperspectral Inversion Model for Submerged Marine Ecosystems using High-performance Computing on Graphical Processor Units," with J. Goodman, D. Schaa and A. Yilmazer, *SPIE Defense, Security and Sensing: Algorithms and Technologies for Multispectral, Hyperspectral, and Ultraspectral Imagery XVI*, Vol. 7695, 2010.
177. "Toward Whole-System Dynamic Analysis for ARM-based Mobile Devices," with R. Whelan, *Recent Advances in Intrusion Detection, 13th International Symposium*, Sept. 2010, pp. 512-513
178. "Using Hardware Vulnerability Factors to Improve AVF Analysis," with V. Sridharan, *IEEE/ACM International Symposium on Computer Architecture (ISCA-37)*, June, 2010, pp. 461-472.
179. "Data Structures and Transformations for Physically Based Simulations on a GPU," with P. Mistry, D. Schaa, B. Jang, A. Dvornik and D. Meglan, *9th International High performance Computing for Computational Science (VECPAR)*, online proceedings, 2010.
180. "Accelerating the Local Outlier Factor Algorithm on a GPU for Intrusion Detection Systems," with M. Alshawabkeh, and B. Jang, *Proc. of GPGPU-3*, 2010, pp. 104-110.
181. "Data Transformations Enabling Loop Vectorization on Multithreaded Data Parallel Architectures," with B. Jang, P. Mistry, and D. Schaa, *ACM SIGPLAN Symposium on the Principles and Practice of Parallel Programming*, Jan. 2010, pp. 353-354.
182. "Quantifying Load Imbalance on Virtualized Enterprise Servers," with E. Arzuaga, *ACM Conference on Performance Engineering WOSP/SIPEW*, Jan 2010, pp. 235-242.
183. "A Binary Instrumentation Tool for the Blackfin Processor," with E. Sun, *Proceedings of the Workshop on Binary Instrumentation and Applications*, Dec. 2009.
184. "Improving the Open64 Backend for GPUs," with R. Dominguez, J. Cavazos and M. Murphy, *NVIDIA NVISIONS Workshop*, October 2009.
185. "Profile-Guided Optimization of Critical Medical Imaging Algorithms," with B. Jang, P. Mistry and D. Schaa, *IEEE International Symposium on Biomedical Imaging*, Invited Session, June 2009, pp. 1293-1294.

186. "Multi GPU Implementation of Iterative Tomographic Reconstruction Algorithms," with B. Jang, S. Do and H. Pien, *IEEE International Symposium on Biomedical Imaging*, June 2009, pp. 185-188.
187. "Architecture-aware Optimization Targeting Multi-Threaded Stream Computing," with B. Jang, S. Do, H. Pien, *Proceedings of GPGPU 2009*, pp. 62-70.
188. "Accelerating Phase Unwrapping and Affine Transformations for Optical Quadrature Microscopy Using CUDA," with P. Mistry, S. Braganza, and M. Leeser, *Proceedings of GPGPU 2009*, pp. 28-37.
189. "Software Transactional Memory for Multicore Embedded Systems," with J. Mankin and J. Ardini, *Proceedings of the ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems*, June 2009, pp. 90-98.
190. "Exploring the Multiple-GPU Design Space," with D. Schaa, *IEEE International Parallel and Distributed Processing Symposium*, **Best Paper Award**, May 2009, pp. 1-12.
191. "Eliminating Microarchitectural Dependency From Architectural Vulnerability," with V. Sridharan, *Proceedings of the 15th International Conference on High Performance Computer Architecture*, IEEE Computer Society, Feb. 2009, pp. 117-128.
192. "Performance Prediction in Multi-GPU Execution," with D. Schaa, *NVISION'08* August, 2008.
193. "A Taxonomy to Enable Error Recovery and Correction in Software," with V. Sridharan and D. Liberty, *Workshop on Quality-Aware Design (W-QUAD)*, June, 2008.
194. "Quantifying Software Vulnerability," with Vilas Sridharan, *WREFT '08: Proceedings of the 2008 workshop on Radiation effects and fault tolerance in nanometer technologies*, May 2008, pp. 323-328.
195. "A Field Analysis of System-Level Effects of Soft Errors Occurring in Microprocessors used in Information Systems," with S. Shazli, M. Abdul-Aziz and M.B. Tahoori, *International Test Conference*,, November 2008.
196. "A Field Analysis of Soft Errors Occurring in Microprocessors used in Information Systems," with S. Shazli and M. Tahoori, *North Atlantic Test Conference*, May 2008.
197. "Field Failure Analysis of Microprocessors used in Information Systems," with S. Shazli, M. Abdul-Aziz and M. Tahoori, *DSN 2008 Workshop on Resilience Assessment and Dependability Benchmarking*, June 2008.
198. "Performance Evaluation of Virtual Appliances," with Z. Chen and K. Murphy, *First International Workshop on Virtualization Performance: Analysis, Characterization, and Tools (VPACT'08)*, April, 2008.
199. "Resource-Conscious Optimization of Cryptographic Algorithms on an Embedded Architecture," with W. Bassalee, *Proceedings of the ACM Workshop on Optimizations for DSP and Embedded Systems*, April 2008, pp. 82-92.

200. "Interactive Deformable Registration Visualization and Analysis of 4D Computed Tomography," with B. Erem, G. Sharp, and Z. Wu, Proceedings of the *1st International Conference on Medical Biometrics*, ICMB Hong Kong, China, January 4-5, 2008, pp. 232-239.
201. "An M/G/1 Queue Model for Multiple Application on Storage Area Networks," with E. Arzuaga, Proceedings of the *11th Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW-11)*, February 2008.
202. "Characterizing the Relationship Between ILU-based Preconditioners and the Storage Hierarchy," with D. Rivera and M. Kilmer, Proceedings of the *International Conference on Preconditioning Techniques for Large Sparse Matrix Problems in Scientific and Industrial Applications*, 2007, pp. 74-77.
203. "Exploring Novel Parallelization Technologies for 3-D Imaging Applications," with D. Rivera, D. Schaa, and M. Moffie, *The 19th Symposium on Computer Architecture and High Performance Computing*, October 2007, pp. 26-35.
204. "Stream Image Processing on a Dual-Core Embedded System," with M. Benjamin, Proceedings of the *Embedded Computer Systems: Architectures, Modeling, and Simulation, 7th International Workshop, SAMOS 2007*, Samos, Greece, July 2007, also appearing in *Lecture Notes in Computer Science*, Springer 2007, pp. 185-194.
205. "Reliability in the Shadow of Long-Stall Instructions," with V. Sridharan and A. Biswas, Proceedings of the *3rd Workshop on Silicon Errors in Logic - System Effects (SELSE-3)*, April 2007.
206. "External Memory Page Remapping for Embedded Multimedia Systems," with K. Ning, Proceedings of the *ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems*, June 2007, pp. 185-194.
207. "Heterogeneous Clustered VLIW Microarchitectures," with A. Aleta, J.M. Codina, and A. Gonzalez, Proceedings of the *5th IEEE International Symposium on Code Generation and Optimization*, March 2007, pp. 354-366.
208. "Case Study: Soft Error Rate Analysis in Storage Systems," with B. Mullins, H. Asadi, M. Tahoori, K. Granlund, R. Bauer, and S. Romano, Proceedings of the *25th IEEE VLSI Test Symposium*, May 2007, pp. 256-264.
209. "Use of an Embedded Configurable Memory for Stream Image Processing," with M. Benjamin, Proceedings of the *5th Workshop on Optimizations for DSP and Embedded Systems*, March 2007, pp. 14-20.
210. "A Code Layout Framework for Embedded Processors with Configurable Memory Hierarchy," with K. Sanghai, A. Raikman and K. Butler," Proceedings of the *5th Workshop on Optimizations for DSP and Embedded Systems*, March 2007, pp. 29-38.
211. "Stream Programming on the Blackfin Architecture," with M. Benjamin, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 29-30.

212. "Characterizing the Relationship Between Sparse Matrix Preconditioners and the Storage Hierarchy," with D. Rivera and M. Kilmer, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 37-38.
213. "Performance Characterization of SPEC CPU2006 Integer Benchmarks," with D. Ye and J. Ray, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 67-72.
214. "Instruction-Level Energy Estimation," with S. Molloy, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 95-100.
215. "Case Study: Soft Error Rate Analysis in Storage Systems," with B. Mullins, H. Asadi, M. Tahoori, K. Granlund, R. Bauer, and S. Romano, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 39-40.
216. "Acceleration of Maximum Likelihood Estimation for Tomosynthesis Mammography," with J. Zhang, W. Meleis, T. Wu, Proceedings of the *International Conference on Parallel and Distributed Systems*, July 2006, 291-299.
217. "Hunting Trojan Horses," with M. Moffie, W. Cheng, and Q. Zhao, Proceedings of the *Workshop on Architecture and System Support for Improving Software Dependability*, October 2006, pp. 12-17.
218. "Performance Characterization of SPEC CPU2006 Integer Benchmarks on the x86-64 Architecture," with D. Ye, C. Harle, and J. Ray, Proceedings of the *IEEE Symposium on Workload Characterization*, invited paper, October 2006, pp. 120-129.
219. "Experiences with the Blackfin Architecture for an Embedded Systems Lab," with M. Benjamin and R. Platcow, Proceedings of the *Workshop on Computer Architecture Education*, July 2006. pp. 3-9.
220. "Vulnerability Analysis of L2 Cache Elements to Single Event Upsets," with H. Asadi, V. Sridharan and M. Tahoori, Proceedings of *Design Automation and Test in Europe (DATE) Conference*, March 2006, pp. 1276-1281.
221. "Visualization of 4-D Computed Tomography Images," with N. Dedual and G. Chen, Proceedings of the *IEEE Southwest Symposium on Image Analysis and Interpretation*, March 2006, pp. 120-123.
222. "Model-based Probabilistic Prediction of Tumor Respiratory Motion," with H. Wu, G. Sharp, B. Salzberg, H. Shirato and S. Jiang, Proceedings of the *47th Annual Meeting of the American Association of Physicists in Medicine (AAPM)*, 2005.
223. "A Benchmark Suite for Behavior-Based Security Mechanisms," with D. Ye and M. Moffie, Proceedings of the *Workshop on Software Security Assurance Tools, Techniques, and Metrics (SSATM '05)*, November 2005.
224. "ASM: An Application Security Monitor," with M. Moffie and W. Cheng, Proceedings of the *Workshop on Binary Instrumentation and Applications (WBIA '05)*, September 2005, pp. 31-36.

225. "Reliability Tradeoffs in the Design of Cache Memories," with H. Asadi, V. Sridharan and M. Tahoori, Proceedings of the *First Workshop on Architectural Reliability (WAR-I)*, Barcelona, Spain, November 2005, pp. 50-57.
226. "Load Balancing using Grid-based Peer-to-Peer Parallel I/O," with Y. Wang, Proceedings of the *2005 IEEE Cluster Computing Conference*, Boston, MA, 2005.
227. "Power Aware External Bus Arbitration for System-on-a-Chip Embedded Systems," with K. Ning, Proceedings of *HIPEAC*, November, 2005, pp. 95-106.
228. "Exploiting Temporal Locality in Drowsy Cache Policies," with S. Petit, J. Sahuquillo and J.M. Such, *Computing Frontiers*, 2005, pp. 371-377.
229. "A Multinomial Clustering Model for Fast Simulation of Computer Architecture Designs," with K. Sanghai, T. Su, and J. Dy, *Proceedings of the 11th ACM SIGKDD International Conference on Knowledge Discovery and Data Mining*, Aug. 2005, pp. 808-813.
230. "Subsequence Matching on Structured Time Series Data," with H. Wu, B. Salzberg, G.C. Sharp, S.B. Jiang, and H. Shirato, *Proc. of ACM Conference on the Management of Data (SIGMOD)*, 2005, pp. 682-693.
231. "Demystifying On-the-Fly Spill Code," with A. Aleta, J.M. Codina, and A. Gonzalez, *Proc. of the ACM Conference on Programming Languages, Design and Implementation (PLDI)*, 2005, pp. 180-189.
232. "Code and Data Partitioning on the Blackfin 561 Dual-core Platform," with K. Sanghai and R. Gentile, *Proc. of the Workshop on Optimization of DSP and Embedded Systems*, March 2004, pp. 92-100.
233. "A MATLAB Toolbox for Hyperspectral Image Analysis," with E. Arzuaga-Cruz, L.O. Jimenez-Rodriguez, M. Velez-Reyes, M., E. Rodriguez-Diaz, H.T. Velazquez-Santana, A. Castrodad-Carrau, L.E. Santos-Campis, C. Santiago, *Geoscience and Remote Sensing Symposium*, Vol. 7, Sept. 2004, pp. 4839-4842.
234. "Program Comprehension Using Aspects," with D. Ng and D. Lorenz, *Proceedings of the Workshop in Directions in Software Engineering Environments*, May 2004.
235. "Balancing Performance and Reliability in the Memory Hierarchy," with G. Asadi, V. Sridharan and M. Tahoori, *Proceedings IEEE of International Symposium on Performance Analysis, Systems and Software*, March 2005, pp. 269-279.
236. "Bus Power Estimation and Power-Efficient Bus Arbitration for System-on-a-Chip Embedded Systems," with Ke Ning, *Workshop on Power Aware Computing Systems*, December 2004.
237. "Execution-Driven Simulation of Network Storage Systems," with Y. Wang, *Proceedings of the 12th ACM/IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS)*, October 2004, pp. 604-611.

238. "Value Prediction with Perceptrons," with A. Thomas, *Proceedings of the 2nd Annual Value Prediction Workshop*, October, 2004, pp. 3-9.
239. "A Reliable Return Address Stack: Microarchitectural Features to Defeat Stack Smashing," with D. Ye, *Proceedings of the Workshop on Architectural Support for Security and Anti-Virus*, October 2004, pp. 69-76, also appearing in *ACM SIGARCH News*, March 2005.
240. "Characterizing Antivirus Workload Execution," with D. Uluski and M. Moffie, *Proceedings of the Workshop on Architectural Support for Security and Anti-Virus*, October 2004, pp. 86-94, also appearing in *ACM SIGARCH News*, March 2005.
241. "Developing Energy-Aware Strategies for the Blackfin Processor," with S. VanderSanden, G. Olivadoti and R. Gentile, *Proceedings of the 8th Workshop on High Performance Embedded Computing (HPEC)*, MIT Lincoln Labs, September 2004, pp. 198-200.
242. "A Study of Errant Pipeline Flushes caused by Value Misspeculation," with D. Balkan and J. Kalamatianos, *The 15th Symposium on Computer Architecture and High Performance Computing*, October 2004, pp. 32-39.
243. "Characterizing the Dynamic Behavior of Workload Execution in SVM Systems," with Salvador Petit, Julio Sahuquillo and Ana Pont, *The 15th Symposium on Computer Architecture and High Performance Computing*, October 2004, pp. 230-237.
244. "Exploring Hybrid Instruction Prefetching Schemes to Boost Performance," with M. de Alba, *The 5th International Conference on Control, Virtual Instrumentation and Digital Systems*, Sept, 2004, pp. 155-164.
245. "A Hidden Markov Model for Tumor Motion Analysis," with W. Wu, G.C. Sharp, B. Salzberg, and H. Shirato, *46th Annual Meeting of the American Association of Physicists*, 2004, 31(6),1760.
246. "Bi-Criteria Models for All-Uses Test Suite Reduction," with J. Black and E. Melanchrinoudos, *International Conference on Software Engineering (ICSE)*, May 2004, pp. 106-115.
247. "A Polylogarithmic Time Parallel Maximum Weight Bipartite Matching Algorithm for Scheduling in Input-Queued Switches," with M. Fayyazi and W. Meleis, *Proceedings of International Parallel and Distributed Processing Symposium (IPDPS)*, April 2004, pp. 4-5.
248. "Digital Tomosynthesis Mammography using a Parallel Maximum Likelihood Reconstruction Method," with T. Wu, R. Moore, E. Rafferty, D. Koppans, J. Zhang and W. Meleis, *Medical Imaging: Physics of Medical Imaging*, 5368, February 2004, pp. 1-11.
249. "A Reliable Call/Return Address Stack-Pair to Defeat Stack Smashing," with D. Ye and M. Moffie, *Proceedings of the 2004 Boston Area Computer Architecture Research Workshop*, January 2004.
250. "Profile-Guided I/O Partitioning," with Y. Wang, *Proceedings of the 17th ACM International Symposium on Supercomputing*, June 2003, pp. 252-260.

251. "Instruction Replication for Clustered Microarchitectures," with A. Aleta, J.M. Codina and A. Gonzalez, *Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture*, Dec. 2003, pp. 326-335.
252. "Dynamic Input Buffer Allocation (DIBA) for Fault Tolerant Ethernet Packet Switching," with M. Fayyazi and Z. Navabi, *Proceedings of PDPTA*, June 2003, pp. 819-823.
253. "The Impact of Value Misspeculation on Branch Resolution in Out-of-Order Superscalar Microprocessor," with D. Balkan and J. Kalamatianos, *Proceedings of the Value Prediction Workshop*, June 2003.
254. "Source Level Transformations to Apply I/O Data Partitioning," with Y. Wang, *Proceedings of the IEEE Workshop on Storage Network Architecture And Parallel IO*, Oct. 2003, pp.12-21.
255. "The CenSSIS Image Database," with H. Wu, B. Norum, J. Newmark, B. Salzberg, C.M. Warner and C. DiMarzio, *Proceedings of the 15th ACM International Conference on Scientific and Statistical Database Management*, June 2003, pp. 117-126.
256. "A MATLAB Toolbox for Hyperspectral Imaging," with E. Arzuaga-Cruz, L. Jimenez-Rodriguez, M. Velez-Reyes, E. Rodriquez-Diaz, L. Santos-Campis and C. Santiago, *Proceedings of the IEEE Workshop on Advances in Techniques for Analysis of Remotely Sensed Data*, Oct. 2003.
257. "Developing an Object-oriented Parallel Iterative-Methods Library," with C. Ouarroui, *Proceedings of Workshop on Hardware/Software Support for High Performance Scientific and Engineering Computing*, September 2003, pp. 8-15.
258. "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," with D. Morano, A. Khalafi and A. Uht, *ACM SIGARCH Computer Architecture News*, Vol. 31, No. 1, March 2003, pp. 16-25.
259. "Profile-Guided Data Partitioning to Achieve High Performance I/O," with Y. Wang *Proceedings of the Boston Area Computer Architecture Research Workshop*, January 2003.
260. "Characterization and Evaluation of Loop Unrolling Hardware," with M. de Alba, *Proceedings of the Boston Area Computer Architecture Research Workshop*, January 2003.
261. "Realizing High IPC Using Time-Tagged Resource-Flow Computing," with A. Khalafi, D. Morano and A. Uht, *Proceedings of Europar 2002*, Springer-Verlag, August, 2002, pp. 490-499.
262. "Path-based Hardware Loop Prediction," with M. de Alba, *4th International Conference on Control, Virtual Instrumentation and Digital Systems*, Mexico City, Mexico, August, 2002, pp. 29-38.
263. "Exploiting Pseudo-schedules to Guide Data Dependence Graph Partitioning", with A. Aleta, J. Sanchez and A. Gonzalez, *Proceedings of IEEE Parallel Architectures and Compilation Techniques*, Sept. 2002, pp. 281-290.

264. "Register Pressure-Based Modulo Scheduling for Clustered VLIW Architectures," with A. Aleta, J. Sanchez and A. Gonzalez, *Proceedings of Jornadas de Concurrencia*, June 2002, pp. 1-10.
265. "Localized Message Passing Structures for High Speed Ethernet Packet Switching", with M. Fayyazi, *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications*, June 2002, pp. 1551-1557.
266. "WBT'01 Workshop Summary," with E. Altman, *Computer Architecture News*, eds. S. Bartolini, R. Giorgi, J. Protic, C. Prete and M. Valero, Vol. 29, No. 5, December 2001, pp. 84-85.
267. "Profile-guided Tuning of Heap-based Memory Access," with E. Yardimci, *Proceedings of the Workshop on Memory Performance Issues*, June 2001.
268. "Runtime Predictability of Loops," with M. de Alba, *IEEE 4th Annual Workshop on Workload Characterization*, held with the 34th Annual International Symposium on Microarchitecture, Austin Texas, December 2001, pp. 91-98.
269. "Profile-Guided Compilation Targeting High Performance Embedded Applications," with J. Smith, M. Bicer and E. Yardimci, *Proceedings of the 5th Workshop on High Performance Embedded Computing (HPEC)*, MIT Lincoln Labs, November 2001, pp. 147-148
270. "Levo: IPC in the 10's via Resource Flow Computing," with Uht A.K., Morano D., Khalafi A., de Alba M., Wenisch T. and Ashouei M., *PACT 2001 Work-In-Progress (WIP) Session*, September 2001, also appearing in *IEEE TCCA News*, October 2001, pp. 25-29.
271. "Analysis of Dynamic Loops," with M. de Alba, *3rd International Conference on Control, Virtual Instrumentation and Digital Systems*, August 2001. Mexico City, Mexico, pp. 93-106.
272. "Binary Translation," with E. Altman, *IEEE TCCA News*, October 2001, pp. 4-5
273. "Accurate Simulation and Evaluation of Code Reordering," with J. Kalamatianos, *Proceedings of the IEEE International Symposium on the Performance Analysis of Systems and Software*, Austin, TX, April 2000.
274. "Model Based Parallel Programming with Profile-Guided Application Optimization," with J. Smith, *Proceedings of the 4th Annual High Performance Embedded Computing Workshop*, MIT Lincoln Labs, Lexington, MA, September 2000, pp.85-86.
275. "Scalable Cached Disk Arrays," with M. Singh and W. Zahavi, *Proceedings of the 3rd Workshop on Computer Architecture Evaluation using Commercial Workloads*, Toulouse, France, January 2000.
276. "Using Cache Line Coloring to Perform Aggressive Procedure Inlining," with H. Aydin, *Proceedings of Interact-4*, Toulouse, France, January 2000, *ACM SIGARCH News*, March 2000.

277. "DSPTune: A Performance Evaluation Toolset for the SHARC Signal Processor," with S. Sair, G. Olivadoti, W. Meleis, *Proc. of the 33rd Simulation Symposium*, April 2000, pp. 51-57.
278. "Studying the Performance of the FX!32 Binary Translation System," with P. Drongowski, M. Fayyazi, D. Hunter and J. Casmira, *Proceedings of the 1st Workshop on Binary Translation*, Newport Beach, CA, Oct. 1999, also appearing in the IEEE TCCA News, December 1999, pp. 56-68.
279. "A Study of Dynamic Branch Predication for SHARC DSP's", with S. Sair and J. Fridman, *Proceedings of the 2nd International Workshop on Compiler and Architecture Support for Embedded Systems (CASES'99)*, Washington, D.C., Oct. 1999.
280. "Improving the Accuracy of Indirect Branch Prediction via Branch Classification," with J. Kalamatianos, *Proceedings of the 3rd Workshop on the Interaction Between Compilers and Computer Architecture*, October 1998, San Jose, CA, also appearing in ACM Computer Architecture News, Vol. 27, No. 1, March 1999, pp. 23-26.
281. "Predicting Indirect Branches via Data Compression," with J. Kalamatianos, *Proceedings of 31st ACM/IEEE Symposium on Microarchitecture*, Dec. 1998, Dallas, TX, pp. 272-281.
282. "Parameter Value Characterization of Windows NT-based Applications," with J. Kalamatianos and R. Chaiken, *Proceedings of the 1st Workshop on Workload Characterization*, IEEE Press, Dallas, TX, December 1998.
283. "A Study of Loop Unrolling for VLIW-based DSP Processors," with S. Sair and W. Meleis, *Proceedings of the IEEE Workshop on Signal Processing Systems: Design and Implementation*, October 1998, pp. 519-527.
284. "Performance Analysis Using NT-based Workloads," with J. Casmira and D. Hunter, *Proceedings of the 3rd Workshop on Pre-Hardware Performance Analysis Techniques*, Barcelona, Spain, June 1998.
285. "Memory Performance Tuning using Graph-based Analysis," with J. Kalamatianos, A. Khalafi, and W. Meleis, *Proceedings of the 3rd Workshop on Pre-Hardware Performance Analysis Techniques*, Barcelona, Spain, June 1998.
286. "Temporal-based Procedure Reordering for Improved Instruction Cache Performance," with J. Kalamatianos, *Proceedings of the 4th International Conference on High Performance Computer Architecture*, February 1998, pp. 244-253.
287. "Operating System Impact on Trace-Driven Simulation," with J. Casmira, J. Fraser, and W. Meleis, *Proceedings of the 31st Annual Simulation Symposium*, IEEE Computer Society, April 1998, pp. 76-82.
288. "Efficient Procedure Mapping using Cache Line Coloring," with A.H. Hashemi and B. Calder, *Proceedings of ACM SIGPLAN Conference on Programming Languages Design and Implementation*, June 1997, Las Vegas, Nevada, pp. 171-182.

289. "Analytical Models of Workload Behavior and Pipeline Performance," with M. Squillante and H. Sinha, *Proceedings of IEEE MASCOTS*, January 1997, Israel, pp. 91-96.
290. "Efficient Static Procedure Mapping using Cache Line Coloring," with A.H. Hashemi and B. Calder, *Proceedings of the 2nd Workshop on Interaction between Compilers and Computer Architectures*, February 1997, San Antonio, TX.
291. "Improving Multiprocessor Scalability Using Lockup Free Caches," *Proceedings of Parallel and Distributed Processing, with H. Sinha, Technology and Applications 1996*, Sunnyvale, CA, Aug. 1996, pp. 619-622.
292. "Using a BTB to Guide Data Cache Prefetching," with Y. Liu, *Proceedings of the 1996 IEEE International Conference on Computer Design*, Austin, Tx., Oct. 1996, pp. 225-230.
293. "Performance Modeling Using Object-Oriented Execution-Driven Simulation," with A.V. Sampogna, D. Green, M. Silva and C.J. Sniezek, *Proceedings of the 29th Annual Simulation Symposium*, New Orleans, LA, April 1996, pp. 183-192.
294. "Improving Multiprocessor Scalability Using Lockup Free Caches," with S. Belayneh and H. Sinha, *Proceedings of the 6th Workshop on Shared Memory Multiprocessors*, Cambridge, MA, Oct. 1996.
295. "A Discussion on Non-Blocking/Lockup-Free Caches," with S. Belayneh, *Computer Architecture News*, Vol. 24, No. 4, September 1996.
296. "A Discussion on Non-Blocking/Lockup-Free Caches," with S. Belayneh, *Computer Architecture News*, Vol. 24, No. 3, June 1996.
297. "Efficient Procedure Mapping for Improved Instruction Cache Performance," with A.H. Hashemi, *Proceedings of the Workshop on Interaction Between Compilers and Computer Architectures*, San Jose, CA, Feb. 1996.
298. "Combining Object-Oriented Design and Computer Architecture into a Single Senior-Level Class," *Proceedings of the Workshop on Undergraduate Computer Architecture Education*, Santa Margherita, Italy, June 1995.
299. "Scalable Performance on a Distributed Shared-Memory Machine," with L. Fong, D. Renfrew, R. Booth, and K. Imming, *Proceedings of Parallel and Distributed Processing, Technology and Applications 1995*, Athens, Georgia, Nov. 1995, pp. 728-737.
300. "Memory Hierarchy Exploration Using Execution-Driven Simulation," with A. Sampogna, *Proceedings of the ACM Workshop on Pre-Hardware Performance Analysis Techniques*, Santa Margherita, Italy, June 1995.
301. "Reducing Cache Pollution," with J. Casmira, *Proceedings of IASTED International Conference on Modeling and Simulation*, Pittsburgh, PA, April 1995, pp. 123-126.
302. "Branch-Directed Data-Cache Prefetching," with P.Y. Chang and Y. Liu, *Proceedings of the 4th Workshop on Scalable Shared Memory Multiprocessors*, Chicago, IL, 1994.

303. "Predicting the Number of Branches in a Finite-Length Pipeline," with M. Squillante and P. Emma, *Proceedings of the 23rd Annual Pittsburgh Modeling and Simulation Conference*, Vol. 23, Part 2, April 1992, pp. 765-772.
304. "A Study of 80X86/80X87 Floating-Point Execution," with Z. Miljanic, *Proc. of the 1991 ACM SIGSMALL/PC Symposium on Small Systems*, June 1991, pp. 34-42.
305. "Branch History Table Prediction of Moving Target Branches Due to Subroutine Returns," with P. Emma, *Proceedings of the ACM 18th Annual International Symposium on Computer Architecture*, Vol. 19, No. 3, May 1991, pp. 34-42.
306. "Issues in Trace-Driven Simulation," *Proceedings of the 22rd Annual Pittsburgh Modeling and Simulation Conference*, Vol. 22, Part 5, May 1991, pp. 2533-2540.
307. "PC Workload Characterization," with S. Ong and S. Kirkpatrick, *Proceedings of ACM Sigmetrics and Performance 89*, Vol. 17, No. 1, May 1989, pp. 220.

U.S. Patents and Industrial Disclosures:

1. *Evaluating and Predicting Computer System Performance Using Kneepoint Analysis*, with G. Smirnov, L. Fairbanks and K. Hu, U.S. Serial No. 9,977,721, May 22, 2018, U.S. Patent Office.
2. *Evaluating and Predicting Computer System Performance Using Kneepoint Analysis*, with G. Smirnov, L. Fairbanks and K. Hu, U.S. Serial No. 8,805,647, August 12, 2014, U.S. Patent Office.
3. *VMM-Based Intrusion Detection System*, with M. Moffie, A. Cohen, J. Aslam, M. Alshawabkeh, J. Dy and F. Azmandian, U.S. Serial No. 8,719,936, May 6, 2014, U.S. Patent Office.
4. *Not-taken Path Instruction for Selectively Generating a Forwarded Result from a Previous Instruction Based on Branch Outcome*, with G. Uht and D. Morano, U.S. Serial No. 8,601,245, December 3, 2013, U.S. Patent Office.
5. *Systems and Methods for Determining Placement of Virtual Machines*, with G. Smirnov and K. Hu, U.S. Serial No. 8,099,487, January 17, 2012, U.S. Patent Office.
6. *Concurrent Execution of Instruction in a Processing System*, with A. Uht and D. Morano, U.S. Serial No. 7,991,980, August 21, 2011, U.S. Patent Office.
7. *Managing Application System Load*, with R. Corley, W. Stronge, K. Faulkner, B. Schofer and P. Beale, U.S. Patent Application 20110060827, March 10, 2011.
8. *A VMM-Based Intrusion Detection System*, with M. Moffie, A. Cohen, J. Aslam, and M. Alshawabkeh, PCT International Application No. PTC/US2009/32858, February 2009.
9. *Resource Flow Computer*, with A. Uht and D. Morano, U.S. Patent Application 20090043994, February 12, 2009, U.S. Patent Office.
10. *Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates*, with G. Uht and D. Morano, U.S. Serial No. 7,409,524, August 5, 2008, U.S. Patent Office.
11. *Methods and Systems for Identifying Application System Storage Recourses*, with W. Stronge, R. Strechay, K. Faulkner and R. Corley, U.S. Patent Application No. 20080163234, July 3, 2008.
12. *Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates*, with G. Uht and D. Morano, U.S. Serial No. 7,380,108, May 27, 2008, U.S. Patent Office.
13. *Managing Application System Load*, with R. Corley, W. Stronge, K. Faulkner, B. Schofer and P. Beale, U.S. Patent Application 20080027948, January 31, 2008, U.S. Patent Office.
14. *Method and Apparatus for Managing Application Storage Load Based on Storage Network Resources*, with R. Corley, W. Stronge, K. Faulkner, B. Schofer, P. Beale, U.S. Serial No. 60/806,699, U.S. and International patent pending, July 2007.

15. *Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates*, with A. Uht and D. Morano, U.S. Serial No. 7,210,025, April 2007, U.S. Patent Office.
16. *Resource Flow Computing Device*, with A. Uht and D. Morano, U.S. Patent No. 6,976,150, December 13, 2005, U.S. Patent Office.
17. *Memory Architecture Dependent Program Mapping*, with B. Calder and A. Hashemi, U.S. Serial No. 5963972, filed jointly with Digital Equipment Corporation, October 5, 1999 U.S. Patent Office.
18. *Case Block Table for Predicting the Outcome of Blocks of Conditional Branches Having A Common Operand*, with P. Emma, U.S. Serial No. 5,333,283, July 26, 1994, U.S. Patent Office.
19. *Selective Prefetching Based on Miss Latency*, with N. Perugini, IBM Technical Disclosure No. Y08921147.
20. *Tying Data Prefetching to Branch Prediction*, with N. Perugini, IBM Technical Disclosure No. Y08901085.
21. *Aliasing Reduction in the DHT*, with P. Emma, J. Knight, and T. Puzak, IBM Technical Disclosure No. Y08920597.
22. *Folding Resolution of a Case Block into a Case-Block Table*, with P. Emma, IBM Technical Disclosure No. Y08920590.
23. *Efficient Case-Block-Table Miss Handling*, with P. Emma, IBM Technical Disclosure No. Y08920598.
24. *A Tool to Validate Trace Tape Representativeness*, with J. Morris and S. Ong, IBM Technical Disclosure No. Y08900481, IBM Tech. Disc. Bulletin Vol. 34, No. 4B, Sept. 1991, pp. 345-346.
25. *Branch History Table for an Intel 80386*, with S. Ong, IBM Technical Disclosure No. Y08880663, IBM Tech. Disc. Bulletin Vol. 33, No. 4, Sept. 1990, pp. 67.

Publication Editing:

- **Editor-in-Chief** - ACM Transaction on Architecture and Code Optimization, 2020-present.
- **Associate Editor** - Elsevier Future Generation Computer Systems, 2021-present.
- **Associate Editor** - ACM Transaction on Architecture and Code Optimization, 2014-2020.
- **Associate Editor** - Journal of Parallel and Distributed Computing, 2011 - 2021.
- **Associate Editor** - IEEE Transactions on Parallel and Distributed Systems, 2011 - 2020.
- **Associate Editor** - Journal of Instruction Level Parallelism, 2003 - 2010.
- **Associate Editor** - IEEE Computer Architecture Letters, 2001 - 2011.
- **Guest Editor** - Journal of Parallel and Distributed Computing, *General-Purpose Parallel Processing Using GPUs*, 2008, with M. Leeser.
- **Associate Editor** - IEEE Transactions on Computers, 2000 - 2004.
- **Guest Editor** - IEEE Transactions on Computers, Special Issue on High Performance Memory Systems, with F. Lombardi and H. Hadimioglu, November 2001.
- **Co-Editor** - IEEE Computer Magazine, special issue on Binary Translation, March 2000.
- **Co-Editor** - UNESCO Encyclopedia on Life Sciences, Volume on Computer Sciences, June 2000.
- **Editor** - IEEE Technical Committee on Computer Architecture Newsletter, 1998 - 2000.
- **Guest Editor** - IEEE Technical Committee on Computer Architecture Newsletter, Proceedings of WCAE-2, June 1996.
- **Guest Editor** - IEEE Technical Committee on Computer Architecture Newsletter, Proceedings of WCAE-1, Spring 1995.

Invited and Tutorial Talks:

1. "Accelerating Large-Scale Data Studies Through Efficient Data Pipelines and High-Performance Computing," *Gulf of Maine Research Institute Seminar Series*, Nov. 2023.
2. "25 Years of IISWC Innovation," *IEEE IISWC 25th Anniversary Panel*, Oct. 2022.
3. "AMD HIP and ROCm," *AMD HIP Training Course*, 10 sessions, Fall 2021.
4. "Side-channel Analysis and Resiliency Targeting Accelerators," Lehigh University, November 17, 2020.
5. "Exploiting the Benefits of Graphics Processing Units - Programming, Architecture and Simulation," HIPEAC ACACES Summer School, July 16-17, 2020.

6. "The Path to Multi-GPU Computing," *Workshop on General Purpose Processing Using GPUs*, February 23, 2020, Keynote.
7. "CARD Mini-Panel on Security," *Computer Architecture Research Directions*, Panel Organizer, June 23, 2019.
8. "Side-Channel Analysis and Resiliency Targeting Accelerators," *NSF SaTC PI Meeting*, October 28, 2019.
9. "Office Hour - EQUIS and PROTECT - Environmental Containment Threats and Preterm Birth," *Earthsoft Office Hours Webinar*, January 24, 2019.
10. "Side-Channel Attacks: Cyber Offense and Defense," *NSF IUCRC Planning Meeting*, August 23, 2018.
11. "Side-Channel Attacks and Defenses on Today's GPU Accelerators," *SRC T3S e-Workshop*, November 5, 2018.
12. "Side-Channel Analysis and Resiliency Targeting Accelerators," *SRC Annual Meeting*, July 25, 2018.
13. "Research in High Performance Computer Architecture," *Technical University of Munich Lecture Series*, Fraueninsel on Chiemesee, January 19, 2017, invited speaker.
14. "Expanding the Scope of GPU Computing Through Supporting Diversity," *Technical University of Munich Lecture Series*, February 14, 2017, Distinguished Lecture.
15. "Northeastern University Computer Architecture Research Laboratory", *Ghent University Research Seminar Series*, April 19, 2017, Distinguished Lecture.
16. "A Cross-Layer Approach to Accelerating Heterogeneous Applications," *University of Edinburgh Distinguished Lecture Series*, June 12, 2017, Distinguished Lecture.
17. "A Cross-Layer Approach to Accelerating Heterogeneous Computing," *SUNY Binghamton University Distinguished Lecture Series*, September 27, 2017, Distinguished Lecture.
18. "Combining Architectural Fault-Injection and Neutron Beam Testing Approaches Toward Better Understanding of GPU Soft-Error Resilience," *MWSCAS, Hardware-software Co-design Techniques*, August 7, 2017, Invited Paper.
19. "EQUIS and PROTECT at Northeastern University," *Earthsoft Office Hours*, webinar format, December 2016.
20. "How can GPUs become First-class Computing Devices?," *The College of William and Mary Distinguished Lecture Series*, October 2016.
21. "Multi2sim 5.0," *Tutorial at IISWC*, September 2016.
22. "Managing Big Data in SRP Research," *NIEH 50 years of NIEHS*, July 2016.
23. "Accelerators as First-class Computing Devices," *MULTIPROG Workshop*, January 2016.

24. "Integrating Data from Multidisciplinary Research," *NIEHS Superfund Research Program e-Learning Web Seminar Series*, November 2015.
25. "How Cyber Hacks are Changing Higher Ed," *NPR On Campus Series*, January 2015.
26. "The Road to New Heterogeneous Systems," *Drexel University*, May 2014.
27. "Preventing Cyber Threats," *Fox-25 News*, November 2014.
28. "Utilizing EQUIS to Study Exposure and its Impact on Reproductive Health in Northern Puerto Rico," *Earthsoft Corporation*, October 2014.
29. "Protecting Reproductive Health through Environmental Big Data Analysis," *Making Sense from Big Data*, Northeastern University, October 2014.
30. "Exploring the Heterogeneous Design Space for both Performance and Reliability," *Invited Speaker at the 51st Design Automation Conference*, June 2014.
31. "The Road to New Programming Models and Architectures for Future Heterogeneous Systems," *HIPEAC Keynote*, January 2014.
32. "Secure Embedded Systems," Special Session Organizer, *IEEE HPEC*, Sept. 2013.
33. "SHPEC - Secure High Performance Extreme Computing," *IEEE HPEC Panelist*, Sept. 2013.
34. "Heterogeneous Computing: Evolving Programming Models and Emerging Platforms," *IEEE HPEC Invited Talk*, Sept. 2012.
35. "The Convergence of HPC and Embedded Systems in our Heterogeneous Computing Future." *IEEE ICCD Keynote*, Oct. 2011.
36. "Biomedical Computing with GPUs," *Analogic Corporation*, May 2011.
37. "Adventures in Desktop Supercomputing," *Keynote at the 24th Annual CCSC:Southeastern Conference at Spelman College*, November 2010.
38. "Macroarchitecture: A Unifying Framework for Manycore Architecture Research," *Workshop on Micro Architectural Support for Virtualization, Data Center Computing, and Clouds*, December 2010.
39. "GPU Computing - Low-cost High-performance Embedded Computing," *Analogic Distinguished Lecture Series*, October 2010.
40. "Biomedical Research on GPUs" - panel sponsored by Dell Computer and NVIDIA, *Harvard Medical School and Dell*, October 2010.
41. "Commodity Desktop Supercomputing," *Analogic Corporation*, August 2010.
42. "GPUs in Biomedical Imaging," *BK Medical*, Copenhagen, Denmark, August 2010.

43. "GPU Computing," *University Polytechnica of Catalonia - PUMPS Summer School*, June 2010.
44. "Many-core Computing: A Disruptive Technology Enabling Low-cost, Low-power Desktop Computing Organization/Sponsor," Keynote Talk, *IEEE Systor Conference*, May 2010.
45. "Adventures in Desktop Supercomputing," *Hewlett Packard Invited Lecture Series*, March 2010.
46. "The Road to Many-Core Computing," *IBM T.J. Watson Research Center - Invited Lecture Series*, March 2010.
47. "Challenges in Binary Translation for Desktop Supercomputing," *3rd Workshop on Architectural and Microarchitectural Support for Binary Translation*, February 2011.
48. "GPUs and Biomedical Computing," *Boston University*, November 2009.
49. "Trends in GPU Computing," *Harvard Medical School*, October 2009.
50. "GPU Computing," *Tufts University*, October 2009.
51. "GPU Computing," *Spelman College*, September 2009.
52. "GPU Computing," *University of Illinois*, July 2009.
53. "Biomedical Computing with Graphics Processing Units," *IEEE ISBI*, July 2009.
54. "Architectural Approaches to Support Software Security," *IBM T.J. Watson Research Center*, June 2006.
55. "Architectural Approaches to Support Software Security," *Boston University*, May 2006.
56. "Power-Aware Profiling and Benchmarking," *Universitat Politecnica de Catalunya*, Spain, May 2004.
57. "Profiling and Instrumentation," *Universitat Politecnica de Catalunya*, Spain, May 2004.
58. "Power-aware Embedded Benchmarking," *The EEMBC Quarterly Meeting*, Boston MA, April 2004.
59. "A High IPC Multipath Microarchitecture," *Universitat Politecnica de Valencia*, Valencia, Spain, February 2003.
60. "Realizing High IPC Through a Scalable, Multipath Microarchitecture," *Universitat Politecnica de Catalunya*, Barcelona, Spain, July 2002.
61. "Profile Guided Compilation," *Tufts University, Department of Electrical and Computer Engineering*, June 2001.
62. "Profile-Guided Compilation," *University of Massachusetts at Amherst, Department of Electrical and Computer Engineering*, March 2001.

63. "Compilation Techniques for Data Parallel Applications," *Mercury Computer Systems*, April 2001.
64. "Profile-Guided Compilation," InCert Corporation Lecture Series, May 2000.
65. "High-Level Language Control and Hardware-based Branch Prediction," presented at the *University of Rhode Island Electrical Engineering Invited Lecture Series*, October 1998.
66. "Tying High-level Language Control Structure to Dynamic Branch Prediction," presented at the *IBM Mid-Hudson Valley Server Group Technical Vitality Council Seminar*, September 1998.
67. "Operating System Rich Workload Analysis," presented at *IBM T.J. Watson Research Center*, Yorktown Heights, N.Y., July 1998.
68. "Memory Performance Tuning using Graph-based Analysis," presented at the *University Polytechnic of Catalunya*, Barcelona, Spain, June 1998.
69. "Instruction and Data Cache Prefetching," presented at *Brooklyn Polytechnic's Technical Seminar Series*, Brooklyn, N.Y., September 1997.
70. "3-D VLSI Design Automation," presented at *Digital Equipment Corporation's ETE Technical Seminar Series*, Hudson, MA, June 1997.
71. "Procedure Mapping Using Static Call Graph Estimation," invited talk at Microsoft Research, Redmond, WA, May 19, 1997 and at Boston University's *Computer Science Colloquium*, Boston, MA, February 26, 1997.
72. "Issues in Trace-Driven Simulation," invited talk at *Intel Corporation*, Santa Clara, CA, February 1997.
73. "Issues in Trace-Driven Simulation," half-day tutorial presented at *IEEE MASCOTS*, Israel, January 1997.
74. "Issues in Trace-Driven Simulation," half-day tutorial presented at *Performance '97*, Lausanne, Switzerland, Oct. 1996.
75. "Performance Modeling Using Object-Oriented, Execution-Driven Simulation," presented at *Performance Analysis and its Impact on Design*, IBM Austin Research Laboratory, March 27, 1996.
76. "Real-Time Trace Generation," invited keynote talk at *Performance Analysis and its Impact on Design*, IBM Austin Research Laboratory, March 27, 1996.
77. "Prefetching Strategies for the Instruction and Data Stream," presented at *Digital Equipment Corporation's ETE Technical Seminar Series*, Hudson, MA, Sept. 1995.
78. "Issues in Trace-Driven Simulation," half-day tutorial presented at the *20th International Symposium on Computer Architecture*, San Diego, CA, May 1993.
79. "Trace-Driven Simulation," half-day tutorial presented at the *1993 Sigmetrics and Performance '93*, Santa Clara, CA, May 1993.

Research Funding - PI, unless stated otherwise

1. \$600,000 “Collaborative Research: CSR: Medium: Architecting GPUs for Practical Homomorphic Encryption-based Computing, NSF Medium CSR program, 2023.
2. \$3,000,000 “NRT-FW-HTF-HDR: Platforms for Exchange and Allocation of Resources (PEAR),” 2023, co-PI.
3. \$25,000 “AMD D-Gift”, AMD, 2023.
4. \$100,000 “AMD D-Gift”, AMD, 2023.
5. \$98,000 “P17_2023: Integrating GPUs and FPGAs with Processing-in-Memory to Accelerate Fully Homomorphic Encryption,” 2023.
6. \$3,000,000 “NRT-FW-HTF-HDR: Platforms for Exchange and Allocation of Resources (PEAR),” NSF, 2023, co-PI.
7. \$404,391 “f-Site: REU-PATHWAYS: Pathways for Community College Student to Enrich Their Education and Careers,”. NSF, 2023, senior personnel.
8. \$35,094,394 “ECHO-PROTECT Cohort Study Site in Puerto Rico,” NIH, 2023, co-PI.
9. \$750,000 “SAI-R: Designing an Improved Information Infrastructure for Better Decision Making in Pharmaceutical Supply Chains, NSF, 2022, co-PI.
10. \$100,000 “AMD C-Gift”, 2022, PI.
11. \$58,000 “P18-22: Evaluating the Potential for Fully Homomorphic Encryption on Accelerator Platforms (NSF CHEST),” NSF CHEST, 2022, PI.
12. \$86,192 “Developing Courseware For Leveraging AI and Analytics Centered on FAIR Principles,” NIH, 2021, co-PI.
13. \$309,313 “PROTECT Administrative Supplement,” NIEHS, 2021, co-PI.
14. \$85,000 “Secure RISC-V Processor Design, Implementation and Simulation,” NSF IUCRC, 2021, co-PI.
15. \$10,000,000 “Engineering PLUS - Partnerships Launching Underrepresented Systems,” NSF INCLUDES, 2021, senior investigator.
16. \$30,000 “AMD HIP Training,” AMD, 2021, PI.
17. \$99,901 “RAPID: Rapid Monitoring and Assessment of Critical Pharmaceutical Supply Chains,” NSF, 2020, co-PI.
18. \$1,555,750 “Next-Generation Monte Carlo eXtreme Light Transport Simulation Platform,” NIH-R01, 2020.
19. \$70,000 “Secure Processor Design by RISC-V Framework,” NSF IUCRC, 2020, co-PI.

20. \$28,902 “Astrophysics - Amendment 11,” Astrophysics, 2020, co-PI.
21. \$2,200,000 “AI Jumpstart,” Mass-Tech, 2020, co-PI.
22. \$13,527,000 “PROTECT Renewal,” NIEHS, 2020, co-PI.
23. \$140,000 “AMD Gift Agreement A and B,” AMD, 2020.
24. \$557,914 “NSF Major Research Instrumentation,” NSR-MRI, 2020, PI.
25. \$78,501 “PROTECT Internal Use Case,” NIEHS, 2019, co-PI.
26. \$175,482 “Astrophysics - Amendment 9,” Astrophysics, 2019, co-PI.
27. \$28,902 “Astrophysics - Amendment 10,” Astrophysics, 2019, co-PI.
28. \$28,902 “3-D Reconstruction of CT Images,” AstroPhysics, 2019, co-PI.
29. \$201,897 “Mapping PROTECT to Publicly Available Datasets,” NIEHS, 2019, co-PI.
30. \$90,000 “AMD RoCM Research,” AMD Corporation, 2019, PI.
31. \$753,466 “TA2: Dynamic Hardware/Software Compilers for High-Level Languages,” DARPA Software-Defined Hardware, 2018.
32. \$13,217,535 “Environmental Influences on Child Health Outcomes in Puerto Rico (ECHO-PRO),” National Institute of Health, 2018, co-PI.
33. \$50,000 “Heterogeneous Systems Architecture Unrestricted Gift,” HSA Foundation, 2018.
34. \$50,000 “Heterogeneous Systems Architecture Unrestricted Gift,” HSA Foundation, 2017.
35. \$348,037 “Aitf: Collaborative Resesearch: A Framework of Simultaneous Acceleration and Storage Reduction on Deep Neural Networks Using Structured Matrics,” NSF Algorithms in the Field Program, 2017.
36. \$5,749,090 “Renewal: SFS at Northeastern - A Multi-disciplinary Approach,” NSF DGE Scholarship For Service Program, 2017.
37. \$50,000 “Analog Devices Unrestricted Gift for 2016,” Analog Devices, 2015.
38. \$15,000 “Student Travel for PACT 2016,” NSF CCF Program, 2016.
39. \$15,000 “Northeastern University Planning Grant: I/UCRC Energy-Smart Electronic Systems,” NSF I/UCRC Program, 2016.
40. \$1,240,428 “Environmental Influences on Child Health Outcomes in Puerto Rico (ECHO-PRO),” NIH ECHO Program, 2016-2020, co-PI.
41. \$50,000 “Heterogeneous Systems Architecture Unrestricted Gift,” HSA Foundation, 2016.
42. \$50,000, “Evaluation a Parallel Programming Model for Heterogeneous SoCs,” Analog Devices, 2016.

43. \$450,000 “STARSS: Small: Side-Channel Analysis and Resiliency Targeting Accelerators,” NSF STARSS joint program with SRC, 2016-2019.
44. \$500,000, “CRISP Type 1: Multi-Agent Modeling Framework for Mitigating Distributed Disruptions in Critical Supply Chains,” NSF CRISP, 2016-2018, co-PI
45. \$359,587 “REU Site: REU Research Experiences and Mentoring in Data-Driven Discovery,” NSF REU Site Program, 2016-2019.
46. \$100,000 “GPU-Accelerated Monte Carlo Photon Transport Simulation Platform,” NIH/NIGMS R01-GM114365, 2015-2019, co-PI.
47. \$30,000 “Analog Devices Unrestricted Gift for 2015,” Analog Devices, 2015.
48. \$860,648, “BIGDATA: IA: Exploring Analysis of Environment and Health Through Multiple Alternative Clustering,” NSF-IIS, 2016-2019, co-PI.
49. \$250,000 “CSR: Small: Collaborative Research: Leveraging Intra-chip/Inter-chip Silicon-Photonic Networks for Designing Next-Generation Accelerators,” NSF-CNS, 2015-2018.
50. \$30,000 “Advanced Micro Device Unrestricted Gift,” AMD, 2015.
51. \$1,257,461 “DMREF: Engineering Strong, Highly Conductive Nanotube Fibers Via Fusion,” NSF-DMREF, 2014-2017, co-PI.
52. \$50,000 “Heterogeneous Systems Architecture Unrestricted Gift,” HSA Foundation, 2014-2015.
53. \$70,000 “Advanced Micro Device Unrestricted Gift,” AMD, 2014.
54. \$50,000 “Analog Devices Unrestricted Gift for 2014,” Analog Devices, 2014.
55. \$450,000 “CSR:Small:Power Efficient Emerging Heterogeneous Platforms,” NSF-CNS, 2013-2016, co-PI.
56. \$500,00 “MRI: Development of a Testbed for Side Channel Analysis and Security Evaluation (TeSCASE),” NSF-MRI, 2013-2016, co-PI.
57. \$16,607 “Full System Taint,” MIT Lincoln Labs, 2013.
58. \$30,000 “Analog Devices Unrestricted Gift for 2013,” Analog Devices, 2013.
59. \$25,000 “Samsung Southern Islands Simulator,” 2013.
60. \$55,000 “AMD GPU Research Gift,” 2013.
61. \$18,000 “Reducing Uncertainties in SBRT for Pancreatic Cancer,” Massachusetts General Hospital, 2013, subcontract.
62. \$20,016 “Reducing Uncertainties in SBRT for Pancreatic Cancer,” Massachusetts General Hospital, 2012, subcontract.

63. \$40,000 “A System Model for Effective Anomaly Analysis and Detection,” NU-Technion Collaboration, 2012.
64. \$4,500,000 “NSF Scholarship for Service Program,” 2012-2017, co-PI.
65. \$4,540,000 “C3DDB Phase II Application,” MA Life Science, 2012, co-PI.
66. \$95,000 “Multiscale Computation of Nanomaterials,” MGHPC, 2012, co-PI.
67. \$31,126 “Portable Dynamic Taint Analysis with QEMU”, MIT Lincoln Labs, 2012-2013.
68. \$45,495 “A Disk-subsystem Interposer Using a Lightweight Virtual Machine Monitor”, MIT Lincoln Labs, 2012-2013.
69. \$25,000 “Qualcomm Unrestricted Gift,” 2012.
70. \$25,000 “Analog Devices Unrestricted Gift for 2012 Student Support,” Analogic Devices, 2012.
71. \$90,000 “Analogic Research Gift,” 2012.
72. \$30,517 “Analogic GPU Research Project,” 2012.
73. \$65,000 “AMD GPU Research Gift,” 2012.
74. \$8,000 “AMD Reliability Research,” 2012.
75. \$48,121 “Portable Dynamic Taint Analysis with QEMU,” MIT Lincoln Labs, 2011.
76. \$48,121 “A Disk-subsystem Interposer Using a Lightweight Virtual Machine Monitor,” MIT Lincoln Labs, 2011.
77. \$90,000 “Analogic Research Gift,” 2011.
78. \$30,517 “Analogic GPU Research Project,” 2011.
79. \$30,000 “Ultrasound Image Reconstruction Acceleration,” Analogic Corp., 2011.
80. \$56,000 “AMD GPU Research Gift,” 2011.
81. \$25,000 “Analog Devices Unrestricted Gift for 2011 Student Support,” Analogic Devices, 2011.
82. \$349,999 “ SHF:Small:The Cross-layer Reliability Stack,” NSF CCF, 2009-2013.
83. \$824,248 “Puerto Rico Testsite For Exploring Contamination Threats,” NIEHS, 2010-2013, co-PI.
84. \$90,000 “Analogic CenSSIS Corporate Membership to fund GPU Research,” Analogic Corp., 2010.
85. \$30,000 “Analog Devices Unrestricted Gift for 2010 Student Support,” Analogic Devices, 2010.

86. \$199,947 “In-situ Calibration of Stereo Camera and Acoustic Bathymetric Sensors,” NSF ERC SECO, 2010, co-PI.
87. \$80,000 “PRoTECT Partial Equipment Supplement,” NIH, 2010.
88. \$38,371 “Analogic-BK Phase I Grant,” Analogic Corp., 2010.
89. \$30,744 “Analogic-BK Phase II Grant,” Analogic Corp., 2010.
90. \$48,121 “A Disk-subsystem Interposer Using a Lightweight Virtual Machine Monitor,” MIT Lincoln Labs, 2011.
91. \$26,000 “AMD GPU Research Gift - Part 1,” 2010.
92. \$26,617 “AMD GPU Research Gift - Part 2,” 2010.
93. \$12,500 “AMD GPU Research Gift - Part 3,” 2010.
94. \$44,567 “Open Computational Infrastructure for Surgical Skill Development and Assessment,” NIST, 2010, subcontract.
95. \$44,502 “A Disk-subsystem Interposer Using a Lightweight Virtual Machine Monitor,” MIT Lincoln Labs, 2010.
96. \$36,000 “Analogic-BK Ultrasound Acceleration”, Analogic Corp., May 2010.
97. \$56,000, “AMD Biomedical Computing,” AMD Corp, Feb. 2010.
98. \$248,400, “REU Site: BIOSENSE,” NSF EEC-HRD, Apr. 2010-2013, co-PI.
99. \$20,000, “Careers in High Performance Systems Mentoring Workshop,” NSF CCF, 7, 2009, co-PI.
100. \$28,100 “Analog Devices Unrestricted Gift for 2009 Student Support,” Analogic Devices, 2009.
101. \$1,300,000, “Biomedical Imaging Acceleration Toolbox,” NSF-ERC Innovation Program, Dec. 2009-2013.
102. \$1,935,701, “Multi-disciplinary Preparation of Next Generation Information Assurance Practitioners,” NSF DUE, Nov. 2008-2013.
103. \$50,000, “Binary Translation and Optimization on Larrabee,” Intel Corporation, November 2008.
104. \$67,631, “CRI:CRD Collaborative Research: Archer - Seeding a Community-based Computing Infrastructure for Computer Architecture Research and Education,” NSF-CRI Program, April 15, 2008, co-PI.
105. \$61,146, “Benchmarking Virtual Machine Performance,” Network Engines, May 2008.
106. \$25,000, “A Binary Translation Layer for ATI Stream Computing,” AMD, May 2008.

107. \$46,007, "Draper Research Fellowship," Draper Labs, Cambridge MA., July 2007.
108. \$6,656, "Akorri Funding," Akorri Funding, May 2007.
109. \$57,899, "Modeling and Performance Analysis of Multiple Virtual Machines working in Context," Network Engines, March 2007.
110. \$150,000, "Commercial Grade Automatic and Manual Parallelization and Performance Tools," NSF STTR, January 2007, subcontract.
111. \$199,999, "MRI/Acq: Enabling Research on Terabyte-Scale Datasets," National Science Foundation, May 2006, co-PI.
112. \$113,352, "Soft-Error Modeling," EMC, Hopkington, MA., April 2006, co-PI.
113. \$40,973, "Draper Research Fellowship," Draper Labs, Cambridge MA., July 2006.
114. \$55,000, "BlackFin Research," Analog Devices, Norwood, MA., April 2006.
115. \$23,000, "BlackFin Research," Analog Devices, Norwood, MA., September 2005.
116. \$10,000, "Parallelization of Segmentation Codes," Massachusetts General Hospital, September 2005, co-PI.
117. \$50,000, "BlackFin Research," (PI) Analog Devices, Norwood, MA., October 2004.
118. \$500, "Undergraduate Research," (PI) NU Provosts Office, Northeastern University, October 2004.
119. \$12,107, "Developing Power-Aware Compilation Strategies For the Blackfin Platform," Analog Devices, Norwood, MA., July 2004.
120. \$300,000 "Collaborative Research: Tuning Libraries to Effectively Exploit the Memory Hierarchy," National Science Foundation, Advanced Computational Research Program, January 2004, PI.
121. \$1,000 "Boston Area Computer Architecture Research Workshop," (PI), Intel Corporation, Santa Clara, CA, January 2004.
122. \$22,400 "NSF REU Grant," December 2003.
123. \$30,673, "Partitioning of Multimedia Applications on a Multi-core Blackfin Platform," Analog Devices, Norwood, MA., October 2003.
124. \$23,546 "Developing Power-Aware Compilation Strategies For the Blackfin Platform," Analog Devices, Norwood, MA., October 2003.
125. \$241,043 "Architectural Features for Virus Detection and Recovery," National Science Foundation, Computer Systems Architecture Program, Aug. 2003.
126. \$681,674 "Institute of Complex Software Science, ICSS, 5 years, 2002, co-PI.

127. \$19,463 "Software-Defined Radio," Mercury Computer Systems, January 2002.
128. \$25,000 "Foreign Visitors Program," Spanish Ministry of Education and Sports, September 2001.
129. \$9,734 "Research at UPC Barcelona, Spain," NSF Supplemental Award - NSF International Program, July 2001.
130. \$74,961 "Profile-Guided Optimization and Parallelization Targeting Mercury Dataflow Architectures," Mercury Computer, December 2000.
131. \$500,000 "Mercury RACE-system Grant," Mercury Computer, December 2000.
132. \$45,243 "FRIO Processor Performance," Analog Devices, May 2000.
133. \$10,000 "NSF REU Grant," September 2000, co-PI.
134. \$43,000 "Compaq Corporation Funding," October 2000.
135. \$16,500,000(estimated) "An Engineering Research Center for Subsurface Sensing and Imaging System," NSF NSF ERC Program, September 2000, senior investigator, though thrust lead. .
136. \$143,000 "A Memory Intensive Compilation Environment Targeting VLIW and DSP Architectures, NSF MRI Program, September 2000, co-PI.
137. \$21,000 "IBM Partnership Award," IBM Corporation, August 1999.
138. \$255,427 "Interprocedural Value-Based Program Optimization," National Science Foundation, July 1999, co-PI.
139. \$5,000 "Undergraduate Research Fellowship," Sun Microsystems, June 2000.
140. \$32,000 "Compaq Research Grant," Compaq Corporation, May 1999.
141. \$25,778 "Shared University Research Grant," IBM Corporation, September 1998.
142. \$329,794 "A High-Performance, Low-Cost Testbed for Network-based Research," NSF Major Research Instrumentation Program, August 1998, co-PI.
143. \$30,000 "Data/Knowledge Bases for Image Generation," Northeastern Pre-ERC Funding, Northeastern University, June 1998.
144. \$35,000 "Prototype Low-cost Parallel/Distributed Testbed," Northeastern Pre-ERC Funding, Northeastern University, June 1998.
145. \$30,000 " IBM Partnership Award," IBM Corporation, August 1998.
146. \$22,000 "EMC/NUCAR Joint Research Program," EMC Corporation, December 1997.
147. \$84,198 "Development of a DSP Compilation Testbed," NCRI: 97-29856, National Science Foundation, 1997-1998.

148. \$35,000 "Compiler Research," Microsoft Research, August 1997.
149. \$12,000 "Design in the 3rd Dimension," Design Automation Conference, June 1997.
150. \$59,000 "Research on Plasma Etching of Vias for 3-D Microelectronics," Office of Naval Research, April 1996, co-PI.
151. \$79,946 "Three-Dimensional Electronics Using Transferred SOI Films," Kopin Corporation, 1994, co-PI.
152. \$200,000 "Three-Dimensional Electronics Using Transferred SOI Films," Kopin Corporation, 1994-1997, co-PI.
153. \$131,995 "CAREER Program: Research and Education Plan," NSF CAREER Program, Grant Number 95-01172, 1995-1998.
154. \$25,000 "Open Systems I/O Characterization," EMC Corporation, June 1996.
155. \$21,708 "Autobahn Research," Data General Corporation, July 1996.
156. \$21,000 "Tools and Techniques for Open System I/O Tracing," , EMC Corporation, Oct. 1996.
157. \$5,000 "Studying the Characteristics of I/O Database Mining," , Northeastern University College of Engineering, 1996.

Equipment/Software Donations

1. \$58,000 “2 AMD MI-210 GPUs,” AMD, 2023.
2. \$14,000 “2 AMD MI-100 GPUs,” AMD, 2021.
3. \$20,958 “SuperMicro AS-4024GS-TNR Server,” SuperMicro, 2021.
4. \$2,200 “4 NVIDIA GPUs,” NVIDIA, 2020.
5. \$20,000 “6 NVIDIA GPUs,” NVIDIA, 2019.
6. \$3,000 “28 Raspberry Pis and Networking Hardware,” Draper Labs, 2018.
7. \$64,000 “8 NVIDIA V100 GPU cards,” NVIDIA, 2018.
8. \$32,000 “4 NVIDIA V100 GPU cards,” NVIDIA, 2017.
9. \$31,552 “4 Supermicro 2U AMD servers,” Supermicro, 2017.
10. \$44,000 “8 AMD MI25 GPU cards,” AMD, 2017.
11. \$10,000 “144 hours of beam time at Los Alamos National Laboratories for HPC reliability testing,” Los Alamos National Labs, 2017..
12. \$8,000 “ Supermicro Hardware,” Supermicro, 2016.
13. \$5,000 “ AMD APU Hardware,” AMD, 2014.
14. \$5,000 “ Altera FPGA Boards,” Altera, 2013.
15. \$80,000 “ EQiUS Software License,” Earthsoft, 2012-2014.
16. \$20,000 “ APU Cluster,” AMD, 2012.
17. \$2,000, “Snapdragon Tablets,” Qualcomm, 2012.
18. \$10,000, “Developing a GPU Teaching and Research Testbed,” NVIDIA, January 2008.
19. \$14,000, “VI3 ESX Server Licenses,” VMWare, November 2007.
20. \$38,585, “BlackFin BF561s with FPGAs,” Analog Devices, January 2006.
21. \$1,500 “EEMBC Benchmark Consortium Membership,” EEMBC, June 2004.
22. \$3,400 “Power Measurement Equipment,” Analog Devices, May 2004.
23. \$8,000 “BlackFin BF533 Easykits,” Analog Devices, August 2003.
24. \$5,200 “RTExpress Licenses,” Integrated Sensors Incorporated, May 2001.
25. \$5,319,050 “Synopsys Software Licenses Renewal,” Synopsys Corp., January 2000.

26. \$15,683 "Alpha Miata Machines," Compaq Corporation, May 1999.
27. \$20,000 "EDG Compilation Toolset," Edison Design Group, April 1997-2000.
28. \$15,610 "Microsoft Software Licenses," Microsoft Corporation, August 1997.
29. \$10,740 "Alpha PC-164 Gift," Digital Equipment Corporation, April 1997.
30. \$300,000 "EMC Centriplex Donation," EMC Corporation, December 1996.
31. \$6,000 "SCSI-bus Analyzer," EMC Corporation, June 1996.
32. \$6,144,013 "Synopsys University Program," April 1996.
33. \$77,688 "Hewlett Packard Equipment Grant," January 1995.

Panels, Program Chairs and Committees

- **Committee Member** - IEEE Computer Society Fellows Selection Committee, 2010, 2011, 2012, 2014, 2016, 2018, 2020, 2021.
- **Committee Member** - ACM Young Researcher Selection Committee, 2022, 2023.
- **Committee Member** - IEEE Senior Member Selection Committee, 2019.
- **Panel Member** - NSF SHF Small, 2020.
- **Panel Member** - NIH ECHO Data Harmonization Panel, 2020.
- **Panel Member** - DOE SBIR/STTR Program, 2015, 2016, 2017, 2018.
- **Panel Member** - Natural Sciences and Engineering Research Council Strategic Project Grants Program, 2010, 2011, 2012, 2013, 2019.
- **Panel Member** - NSF CAREER Awards, 1998, 2003, 2005, 2006, 2007, 2017.
- **Panel Member** - Canada Foundation for Innovation, Ottawa, Ontario, 2002.
- **Panel Member** - Austrian Science Fund Program, 2009.
- **Panel Member** - SRC PI Meeting, 2017, 2018.
- **Panel Member** - NSF XPS Panel, 2018.
- **Panel Member** - NSF CyberTrust PI Meeting, 2004.
- **Panel Member** - NSF SaTC Panel, 2017.
- **Panel Member** - NSF ITR Panel, May 2004.
- **Panel Member** - NSF Next Generation Software Program, 2001.
- **Panel Moderator** - IEEE ICCD, 2011.
- **General Co-chair** - IEEE International Symposium on Performance Analysis and Systems Software, Boston, MA, April 2020.
- **General Chair** - International Workshop on OpenCL, Northeastern University, May 2019.
- **General Co-Chair** - ACM Computing Frontiers, 2018 Ischia, Italy.
- **General Co-Chair** - Boston Area Computer Architecture Workshop, Northeastern University, January 2020.
- **General Chair** - IEEE CGO 2014, Orlando, FL.
- **General Co-Chair** - ACM ICPE, 2012, Boston, MA.
- **General Chair** - ACM/IEEE ISCA, 2006, Boston, MA.

- **General Co-Chair** - ACM/IEEE PACT, 2003, New Orleans, LA.
- **General Co-chair** - IEEE HPCA-8, 2002, Cambridge, MA.
- **General Co-chair** - HIPEAC, 2017.
- **Program Chair** - HPCA 2023.
- **Program Co-Chair** - IEEE IISWC, 2020.
- **Program Co-Chair** - IWOCL, 2018, 2019.
- **Program Chair** - HIPEAC, 2015.
- **Program Chair** - IEEE CGO 2010.
- **Program Chair** - IISWC, 2005.
- **Program Chair** - SPEC 2009 Workshop.
- **Program Vice-Chair** - IEEE Frontiers, 2007.
- **Program Vice-Chair** - IPDPS, 2008, 2013.
- **Program Vice-Chair** - ICPADS, 2006.
- **Program Track Chair** - SBAC-PAD 2015.
- **Student Travel Chair** - PACT, 2016.
- **Benchmark Chair** - IISWC, 2006.
- **Registration Chair** - ACM ASPLOS, 2004.
- **Tutorial Chair** - IEEE HPCA, 2003.
- **Tutorial and Workshop Chair** - ACM ASPLOS, 1998.
- **Tutorial and Workshop Chair** - IEEE HPCA, 1997.
- **Workshop Chair** - IEEE/ACM PACT, 2004.
- **Local Arrangements Chair** - SELSE, 2017.
- **Local Arrangements Chair** - ACM Sigmetrics, Cambridge, MA, June 2001.
- **Local Arrangements Chair** - ACM ASPLOS, Cambridge, MA November 2001.
- **Local Arrangements Chair** - ACM ASPLOS, 2000.
- **Student Travel Chair** - ACM/IEEE PACT, 2016.
- **ACM Student Research Competition** - ACM/IEEE PACT, 2014.

- **Steering Committee** - ISCA, 2009-2016.
- **Steering Committee** - HPCA, 2009-2016.
- **Steering Committee** - ISPASS, 2022-present.
- **Steering Committee** - IISWC, 2005-present.
- **Steering Committee** - IWOCL, 2019-present.
- **Program Committee** - HPCA, 1999, 2002, 2004, 2007, 2008, 2011, 2016, 2017, 2018, 2019, 2020, 2024.
- **Program Committee** - MICRO, 2001, 2003, 2004, 2005, 2008, 2011.
- **Program Committee** - ISCA, 2008, 2011, 2012, 2015, 2019, 2020, 2021, 2023.
- **Program Committee** - ISPASS, 2001, 2002, 2003, 2004, 2005, 2006, 2019, 2023.
- **Program Committee** - IISWC, 2008, 2009, 2016, 2018, 2019.
- **Program Committee** - IPDPS, 2004.
- **Program Committee** - ICCD, 2010, 2011, 2012, 2017, 2018, 2019, 2021.
- **Program Committee** - ICS, 2018, 2019.
- **Program Committee** - IEEE Big Data 2017, 2018.
- **Program Committee** - Min-Move 2018.
- **Program Committee** - CGO 2008.
- **Program Committee** - PACT, 2000, 2015, 2018.
- **Program Committee** - IWOCL, 2015, 2016, 2017, 2018, 2019, 2020, 2022.
- **Program Committee** - PISCES, 2017.
- **Program Committee** - HASP, 2016, 2017, 2018, 2019.
- **Program Committee** - SELSE, 2012-2022.
- **Program Committee** - REUNS, 2019, 2021, 2022.
- **Program Committee** - Interational Symposium on Foundations and Applications of Big Data Applications, 2017, 2018, 2019.
- **Program Committee** - INFOCOMP, 2014.
- **Program Committee** - SELSE, 2014, 2018.
- **Program Committee** - ICPE, 2014, 2021.

- **Program Committee** - GPGPU, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2022.
- **Program Committee** - ACM Computing Frontiers, 2004, 2007, 2008, 2012, 2021.
- **Program Committee** - Digital Systems Design, 2014.
- **Program Committee** - HotPAR, 2013.
- **Program Committee** - EduPar, 2013, 2014, 2017, 2018, 2019.
- **Program Committee** - CLOSER, 2013, 2014, 2015, 2016, 2018, 2019.
- **Program Committee** - NPC, 2013, 2014.
- **Program Committee** - FutureTech 2012.
- **Program Committee** - CC-Grid, 2012.
- **Program Committee** - Euromicro-DSD Conference 2012.
- **Program Committee** - Workshop on Frontiers of GPU Computing, 2012.
- **Program Committee** - IEEE International Conference on Supercomputing 2012, 2018.
- **Program Committee** - Workshop on On-chip Memory Hierarchy and Interconnects, 2012.
- **Program Committee** - FGC, 2010, 2011.
- **Program Committee** - AINA, 2011.
- **Program Committee** - AMAS-BT, 2010, 2011, 2012, 2013, 2014, 2015.
- **Program Committee** - NaBIC, 2011.
- **Program Committee** - NPC, 2011.
- **Program Committee** - SAAHPC, 2009, 2010, 2011, 2012.
- **Program Committee** - VALID, 2011, 2012.
- **Program Committee** - WACY, 2011.
- **Program Committee** - ACM ICSSDM, 2004.
- **Program Committee** - MEDEA Workshop, 2000, 2003, 2004, 2006.
- **Program Committee** - MTEAC Workshop, 2000-2002, 2007.
- **Program Committee** - WMPI Workshop, 2004, 2005.
- **Program Committee** - ICPP-HPSEC04, 2004.
- **Program Committee** - SBAC-PAD, 2004, 2005, 2006, 2007, 2015, 2015, 2016, 2017, 2018.

- **Program Committee** - ICPP, 2002.
- **Program Committee** - SNAPI, 2003, 2004.
- **Program Committee** - CCN-DMS, SCS, 2002.
- **Program Committee** - IEEE WWC, 2000-2004.
- **Program Committee** - Annual Simulation Symposium, 2000-2006.
- **Program Committee** - W-ICCA, 2000-2001.
- **Program Committee** - SHARC, 2000.
- **Program Committee** - W-EFTS, 1996.
- **Program Committee** - ASONAM, 2021.
- **Program Committee** - WCAE, 2021.
- **Organizer** - Workshop on Architecture and System Support for Improving Software Dependability, 2006.
- **Organizer** - Workshop on Architectural Support for Security and Anti-virus, 2004.
- **Co-Organizer** - Workshop on Memory Performance Issues, 2001, 2002.
- **Co-Organizer** - Workshop on Binary Instrumentation and Applications, 2005, 2006.
- **Co-Organizer** - Workshop on Binary Translation, 1999-2003.
- **Co-Organizer** - 1st Workshop on Solving the Memory Wall, 2000.
- **Co-Organizer** - 1st Workshop on PC-based System Performance Analysis, 1998.
- **Co-organizer** - Workshop on Fault-Tolerant Parallel and Distributed Systems, 1996, 1997, 1998.

Professional Activities:

- **Chair** - IEEE Technical Committee on Computer Architecture, 2009-2015
- **Chair** - IEEE Technical Committee on Microarchitecture and Microprogramming, 2007-2010
- **Vice-Chair** - IEEE Technical Committee on Computer Architecture, 2006-2009
- **Member** - IEEE Computer Society Adhoc Committee on Ethics, Diversity and Inclusion, 2019-present.
- **Member** - NSF TeraGrid Scientific Advisory Board, 2007-2010
- **Member** - CRA Computing Community Consortium, 2007-2010

- **Member** - IEEE/ACM Eckert Mauchley Award Committee, 2022-2023
- **Member** - IEEE/ACM Dissertation Award Committee, 2022-2023
- **Member-at-Large** - ACM SIGMICRO - 2006-2013
- **Executive Committee** - IEEE Technical Committee on Computer Architecture, 2000-2006, 2015-2022
- **Treasurer** - ACM SIGMICRO - 2006-2008
- **Director** - ACM SIGMICRO Awards Program, November 2001-2005
- **Chair** - Sigmetrics Corporate Sponsor Program - 1994-95

Other Honors:

- **IEEE IISWC Hall of Fame** - 2022.
- **IEEE IISWC Attendee Award** - 2022.
- **COE Service Award** - 2018.
- **Best paper nominee** - IEEE ICPE, 2018.
- **Best paper award** - IEEE ICCD, 2017.
- **Best paper nominee** - IEEE IISWC, 2016.
- **ECE Professor of the Year** - ECE HKN Chapter, 2016.
- **IEEE Fellow** - 2010
- **ACM Fellow** - 2022
- **ACM Distinguished Scientist** - 2014
- **COE Distinguished Professor** - 2014
- **HSA Distinguished Professor** - 2014-present
- **HSA Center of Excellence** - 2016-present
- **NVIDIA Research Center** co-director - 2011-2016
- **AMD Academic Research Partner** - 2010-present
- **Award of Recognition** - Northeastern University presented by SWE, SHPE, BESS and SASE, 2014
- **Research Award** - Northeastern RISE, 2012
- **Outstanding Service Award** - SPEC, 2009

- **Outstanding Researcher Award** - Northeastern University College of Engineering, 2009
- **Mentorship Award** - Northeastern University College of Engineering, 2007
- **Distinguished Researcher Award Program** - Northeastern University Provost's Office, 2004, 2005, 2006
- **Eta Kappa Nu Engineering Honor Society**
- **Sigma Xi Honor Society**
- **Who's Who in Teaching in America, 1996**

Consulting and Textbook Reviews:

- **Expert Witness, Hogan, Lovells LLP, 2022-2023.**
- **Expert Witness, Munger, Tolles and Olsen LLP, 2021.**
- **Expert Witness, Latham and Watkins LLP, 2020-2023.**
- **Expert Witness, Devlin Law Firm LLC, 2020-2022.**
- **Expert Witness, Desmarais LLP, 2019-present.**
- **Expert Witness, Grunecker LLP, 2018.**
- **Expert Witness, Freshfields Bruckhaus Deringer LLP, 2018.**
- **Expert Witness, Freitas, Angell and Weinberg, LLP, 2017-2018.**
- **Expert Witness, Barr Group, 2015.**
- **Expert Witness, Oblon, Spivak, McClelland, Maier and Neustadt, LLP, 2014**
- **Chief Science Advisor of Apposable Software, Medway, MA, 2011-2014**
- **CTO of NUIC Technologies, Medway, MA, 2007-2011**
- **Consultant, GLG, 2018.**
- **Consultant for Akorri Networks, Littleton, MA, 2005-2011**
- **Consultant for InCert Corporation, Cambridge, MA, 2000**
- **Motorola Paging Systems, Boynton Beach, FL, 1997-98**
Course developer for the Motorola Architecture Leadership Program
- **Intel Corporation, Santa Clara, CA, 1997**
Expert witness in the Intel-DEC patent lawsuit case
- **Dynamics Research Corporation, West Newton, MA 1994**
Education on Object-oriented Design and C++ Programming

- **Modular Computing Technology, Concord, MA 1993**
Performance modeling and simulation of client-server platforms
- **Various publishers including: Morgan Kaufmann, CRC, Elsevier, Weste, McGraw Hill**
Reviewing textbooks and proposals for texts

Graduate Students:

Defended Ph.D. Theses

1. Dr. Amir Hooshang Hashemi, *Efficient Procedure Mapping for Improved Cache Performance*, PhD, May 1996.
2. Dr. John Kalamatianos, *Microarchitectural and Compile Time Optimizations for Performance Improvement of Procedural and Object Oriented Languages*, PhD, January 2000.
3. Dr. Alireza Khalafi, *Exploring Multipath Execution on a Distributed Microarchitecture*, PhD, June 2003.
4. Dr. Jennifer Black, *Multi-criteria Data Flow Testing*, PhD, August 2003.
5. Dr. Marcos de Alba, *Exposing Instruction Level Parallelism in the Presence of Loops*, PhD, December 2003.
6. Dr. Morteza Fayyazi, *Fault-Tolerant and Efficient Cluster Switch Architecture*, PhD, April 2005.
7. Dr. Huanmei Wu, *Time-based Indexing of Multidimensional Databases*, PhD, May 2005.
8. Dr. David Morano, *Exploring Instruction Level Parallelism Using Resource Flow Execution*, PhD, April 2006.
9. Dr. Yijian Wang, *Modeling and Acceleration of File-IO Dominated Parallel Workloads*, PhD, December 2006.
10. Dr. Ke Ning, *System-Level Memory Power and Performance Optimization for System-on-a-Chip Embedded Systems*, PhD, May 2007.
11. Dr. Micha Moffie, *Investigating the Utility of Software Semantics for Host-based Intrusion Detection Systems*, PhD, August 2008.
12. Dr. Vilas Sridharan, *The System Vulnerability Stack: Abstraction for Vulnerability Assessment*, PhD, May 2010.
13. Dr. Byunghyun Jang, *Evaluation and Enhancement of Memory Efficiency Targeting General-Purpose Computations on Scalable Data-Parallel GPU Architectures*, PhD, December 2010.
14. Dr. Demetris Galatopolullous, *p2pSOA: A Middleware Architecture to Enable Group Collaboration*, PhD, December 2011.

15. Dr. Emmanuel Arzuaga, *Using Live Virtual Machine Migration to Improve Resource Efficiency in Virtualized Data Centers*, PhD, December 2011.
16. Dr. Fatemeh Azmandian, *Virtual Machine Monitor Characterization using Machine Learning*, PhD, August 2012.
17. Dr. Malak Alshawabkeh, *Hypothesis Margin Based Weighting for Feature Selection Using Boosting: Theory, Algorithms and Applications*, PhD, April 2013.
18. Dr. Rodrigo Dominguez, *Dynamic Translation of Runtime Environments for Heterogeneous Computing*, PhD, April 2013.
19. Dr. Jennifer Mankin, *Classification of Malware Persistence Mechanisms using Low-Artifact Disk Instrumentation*, PhD, September 2013.
20. Dr. Ayse Yilmazer, *Micro-architectural Support for Improving Synchronization and Efficiency of SIMD Execution on GPUs*, PhD, December 2013.
21. Dr. Dana Schaa, *Improving the Cooperative Capability of Heterogeneous Processors*, PhD, April 2014.
22. Dr. Perhaad Mistry, *Architectural Support for Irregular Programs and Performance Monitoring for Heterogeneous Systems*, PhD, April 2014.
23. Dr. Esra Yolacan, *Learning from Sequential Data for Anomaly Detection*, PhD, October 2014.
24. Dr. Yash Ukidave, *Architectural and Runtime Enhancements for Dynamically Controlled Multi-Level Concurrency on GPUs*, PhD, December 2015.
25. Dr. Thomas McCormick, *Ultra-Reliable Flash Memory Systems for Embedded Applications*, PhD, April 2016.
26. Dr. Enqiang Sun, *Cross-Platform Heterogeneous Runtime Environment*, PhD, April 2016.
27. Dr. Amir Kavyan Ziabari, *Improving the Global Memory Efficiency in GPU-Based Systems*, PhD, November 2016.
28. Dr. Fanny Nina-Paravecino, *GPU Computing for Image-based Analysis*, PhD, December 2016.
29. Dr. Zhongliang Chen *Architectural Exploration in a Scalar/Vector-based Many-core System*, PhD, December 2016.
30. Dr. Amir Momeni *Exploiting Thread-level Parallelism on Reconfigurable Architectures: A Cross-Layer Approach*, PhD, May, 2017.
31. Dr. Navid Farazmand, *Dynamic Power Management for Graphics and Compute Applications on State-of-the-art Mobile GPUs*, PhD, March 2018.

32. Dr. Mohammad Khavari Tavana, *Architectural Support for Designing Dependable Non-volatile Main Memories*, PhD, March 2018.
33. Dr. Xiang Gong, *Improving GPU Performance Through Instruction Redistribution and Diversification*, PhD, August 2018.
34. Dr. Xiangyu Li, *Exploiting Large-Scale Data Analytics Platforms*, PhD, August 2018.
35. Dr. Akshay Lahiry, *Exploring Compression in the GPU Memory Hierarchy for Graphics and Compute*, PhD, August 2018.
36. Dr. Leiming Yu, *Multi-level Interference-aware Scheduling on Modern GPUs*, PhD, April 2019.
37. Dr. Fritz Previlon, *Characterization and Remediation for Soft Error Reliability for GPUs*, PhD, August 2019.
38. Dr. Charu Kalra, *Compiler-based Resilience Predication and Enhancements for GPU Applications*, PhD, August 2019.
39. Dr. Xun Gong, *Hing Assisted Scheduling on Modern GPUs*, PhD, April 2020.
40. Dr. Saoni Mukherjee, *A Power Modeling Approach to Protect GPUs from Side Channel Attacks*, PD, April 2020.
41. Dr. Yifan Sun, *Enabling Collaborative Heterogeneous Computing*, August 2020.
42. Dr. Shi Dong, *Exploring High Performance Deep Neural Networks on GPUs*, August 2020.
43. Dr. Trinayan Baruah, *Improving the Virtual Memory Efficiency of GPUs*, May 2021.
44. Dr. Maher Kachmar, *Active Resource Partitioning and Planning for Storage Systems Using Time Series Forecasting and Machine Learning Techniques*, June 2021.
45. Dr. Elmira Karimi, *Exploring High Performance Sparse Operations on GPUs*, April 2022.

Defended MS Theses

1. Angela Sampogna, *Architectural Implications of C and C++ Programming Models*, MSEE 1995
2. Yue Liu, *Analysis of Branch Directed Data Cache Prefetching*, MSEE 1995
3. Samson Belayneh, *The Effect of Balanced Instruction Scheduling on the Performance of Non-Blocking Caches*, MSEE 1996
4. Himanshu Sinha, *Non-blocking Caches in Shared Memory Multiprocessors*, MSEE 1996
5. John Fraser, *Cache Analysis in a Multiprocess Environment Using Execution Driven Simulation*, MSEE 1996

6. Mona Dimitri, *Cache Pointer-Based Prefetching for Complex Data Structures*, MSCSE 1997
7. Svetlana Sokolova, *Static Branch Prediction Using High-Level Control Structure*, MSEE 1997
8. Tracy Tao, *Branch Prediction With Branch History Chain Table for Wide-Issue Superscalar Processors*, MSEE 1998
9. Jason Casmira, *Operating System Rich Workload Characterization*, MSEE 1998
10. Mekalu Teshome, *I/O Cache Structures and System Performance*, MSEE 1998
11. Kyle Bowers, *Characterization of the Java Virtual Machine*, MSEE 1999.
12. Hua Huang, *A Buffering Scheme for Improved BSD Fast File System Performance*, MSEE 1999.
13. Ying Liu, *A Channel Routing Algorithm for 3-D VLSI*, MSEE 1999.
14. Manpreet Singh, *Scalable Interconnects and Topologies for High Performance ICDSs*, MSEE 1999.
15. Philip Sailer, *YIFAN is a Pure RISC in a Three-Dimensional Integrated Circuit*, MSEE 2000.
16. Hakan Aydin, *Exploring the Effects of Cache Line Coloring and Procedure Inlining*, MSEE 2000.
17. Efe Yardimci, *Profile-guided Heap Layout*, MSEE, 2001.
18. Songqing Zhang, *BDSPTune: Binary-level Instrumentation of the SHARC DSP*, MSEE, 2001.
19. Murat Bicer, *A Software Communications Architecture Compliant Software Defined Radio Implementation*, MSEE 2002.
20. Deniz Balkan, *Side-Effects of Value Speculation on Branch Resolution and Performance in Out-of-Order Superscalar Microprocessors*, MSEE 2003.
21. Stephen VanderSanden, *Developing Power-Aware Strategies for Embedded DSPs*, MSEE 2004.
22. Anita Thomas, *Value Prediction with Perceptrons*, MSEE 2004.
23. Darren Ng, *Aspect Oriented Garbage Collection*, MSEE 2005.
24. Kaushal Sanghai, *A Code Layout Framework for Embedded Processors with a Configurable Memory Hierarchy*, MSEE 2005.
25. Vilas Sridharan, *Soft Errors in Cache Memories*, MSEE 2006.
26. Diego Rivera, *Accelerating Sparse Matrix Computations*, MSCSE 2007.

27. Brian Mullins, *Soft Errors in Storage Systems*, MSECE 2007.
28. Michael Benjamin, *A Study of Video Processing using Stream Computing on Blackfin Processors*, MSECE 2007.
29. Fatemeh Azmandian, *The Chart Checker: Applying Data Mining Techniques to Detect Major Errors in Radiotherapy Treatment Charts*, MSECE 2008.
30. Seth Molloy, *Energy Conservation Techniques for the Blackfin Processor*, MSEE, 2008.
31. Burak Erem, *Interactive Deformable Registration Visualization and Analysis of 4D Computed Tomography*, MSEE 2008.
32. Derek Uluski, *Real Time Anti-virus for a Virtualized Environment*, MSECE 2008.
33. Wassim Bassalle, *Optimization of Cryptographic Algorithms on an Embedded Architecture*, MSECE 2008.
34. Zhaoqian Chen, *Performance Evaluation and Characterization of Virtual Appliances*, MSECE 2008.
35. Dana Schaa, *Multi-GPU Performance Modeling*, MSECE 2009.
36. Jenny Mankin *Embedded System Transactional Memory*, MSECE 2009.
37. Yungho Yang *Memory Forensics on Embedded Linux*, MS Project 2009.
38. Sarmad George *Multi-core Reliability*, MS Project 2009.
39. Tong Pan *Mapping Decision Tree Algorithms to GPUs*, MSECE 2010.
40. Roberto Cabral *Upgrading a Fieldable Air Traffic Control Interrogator*, MSECE 2010.
41. Joshua Hodosh *Memory System Introspection*. MSECE 2010.
42. Kin Kone Kito *Power profiling on Embedded Processors*, MSECE 2010.
43. Kevin McKinley *GPU Acceleration in a Gordon Challenge Project*, MS Project 2010.
44. Kulin Seth *Heterogeneous System Modeling*, MSECE 2011.
45. Stephen Maresh *Using HAsim to Model a Re-Order Buffer*, MS Project 2011.
46. Matthew Sellitto *Exploring GPU Computing for Hyperspectral Image Analysis*, MSECE 2011.
47. Cristy Casella *Wireless Management of Unattended Ground Sensors*, MS Gordon Leadership, 2011.
48. Jie Tang *An X86 Application on Android*, MS Project, 2011.
49. Allen Lee *Transparent and Dynamic Software Updates for Security*, MS Project, 2012.

50. Raghu Varier *MADNESS - Multi-Resolution Adaptive Numerical Environment for Scientific Simulation*, MS Project, 2012.
51. Yash Ukidave *Investigating Power-Efficiency of Optimization Techniques Applied to Heterogeneous Applications*, MS Thesis 2012.
52. Ryan Whelan *Architecture-Independent Dynamic Information Flow Tracking*, MS Thesis, 2012.
53. Sam Coe, *Full System Taint Analysis*, MS Project, 2014.
54. Yuqing Shi, *A Software Model for Control-Flow Instructions on an NVIDIA Kepler GPU*, MS Project, 2014.
55. Xiangyu Li, *Accelerating Mahout on Heterogeneous Clusters Using HadoopCL*, MS Thesis, 2014.
56. Adrienne Horne, *Power Congestion Analysis Constraint Impact Tool*, MS Gordon Leadership, 2015.
57. Charu Kalra, *Code Optimizatin for Heterogeneous Devices*, MS Thesis, 2015.
58. Fritz Previlon, *GPU Reliability Factor*, MS Thesis, 2016.
59. Obeahon Okaiwele, *Network Failover*, MS Gordon Leadership, 2016.
60. Seth Lipkind, *Automated Nightly Regression Testing of Metro Ethernet Forum and Point-to-point Protocol over Ethernet Protocols*, MS Gordon Leadership, 2016.
61. Patrick Hingston, *Improvements to the Handheld X-ray Fluorescent Analyzer*, MS Gordon Leadership, 2016.
62. Julian Gutierrez, *Exploring the Benefits of Heterogeneous Computing to Accelerate Face Detection Deep Learning Inference*, MS Thesis, 2017.
63. Trinayan Baruah, *Energy Efficient Heterogeneous Applications*, MS Thesis 2017.
64. Bradley Courville, *Exploring the Memory Hierarchy of the NVIDIA Kepler GPU*, MS Thesis, 2017.
65. Benjamin Reynolds, *Kessel Run Release Engineering and Continuous Delivery Pipelines*, MS Gordon Leadership, 2019.
66. Timothy Liming, *AMETEK Aerospace and Defense - S and FMS*, MS Gordon Leadership, 2019.
67. Matin Raayai Arkakani, *A Framework for Denoising Two and Three-Dimensional Monte Carlo Photon Transport Simulations Using Convolutional Neural Networks*, MS Thesis, 2021.

68. Rubens Felix LaCouture, *GPUBLQMR: GPU-Accelerated Sparse Block Quasi-Minimum Residual Linear Solver*, MS Thesis, 2021.
69. Griffin Knipe, *Unifying Performance and Security Evaluation for Microarchitecture Design Exploration*, MS Thesis, 2021.
70. Nicholas Bohm Agostini, *SODA-OPT: Enabling System-Level Design in MLIR for HLS and Beyond*, MS Thesis, 2022.

Courses Taught

- Honors Seminar (Sharing Economy) - (undergraduate)
- High Performance Computing (both undergraduate and graduate)
- Embedded Design - Enabling Robotics (undergraduate)
- Computer Architecture (both undergraduate and graduate)
- Advanced Computer Architecture (graduate)
- Parallel Computing (undergraduate)
- Computer Security (graduate)
- Software Engineering (both undergraduate and graduate)
- Profiling and Instrumentation (graduate)
- VLSI Design (undergraduate)
- Digital Design (undergraduate)
- Introduction to Programming (undergraduate)
- Engineering Programming Models (undergraduate)

Teaching Awards

- **University Teaching Award** - nominated, 1996, 1997, 2012, 2013
- **COE Teaching Award** - Student Speaks Award, 2011
- **Most Outstanding ECE Professor Award** - Northeastern University Eta Kappa Nu Award, 1996, 2016

Present Ph.D. Students

- Nicolas Bohm Agostini,
- Yuhui Bao,

- Aymane El Jerari,
- Zlatan Feric,
- Julian Gutierrez,
- Malith Jayaweera,
- Elmira Karimi,
- Matin Raayai Ardakani,
- Kaustubh Shivdikar,
- Amir Taherin

Present MS Students

- Sana Taghipour Anvari
- Mark Tiburu