Implementation of a 2x2 MIMO-OFDM Real-time System on DSP/FPGA Platform

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***Abstract*—In this paper we present a 2x2 MIMO-OFDM real-time system based on Sundance's Software Radio development kits, which includes TI DSP, Xilinx FPGA, ADC/DAC and RF modules, etc. As a demonstration, we implement an MIMO-OFDM system, which is a simplification version of two antennas IEEE802.11n standard, on this platform to verify its availability. At transmitter it contains OFDM packet generation, encoding of Alamouti STBC and DUC, and DDC. At receiver, the system contains some necessary receiver algorithms, such as OFDM synchronization, channel estimation, decoding of Alamouti STBC, soft demapper and other components. In addition, the designed platform has greater feasibility and can be used for performance evaluation of newly developed signal processing algorithms.**

Keywords- MIMO-OFDM; IEEE802.11n; synchronization; soft demapper

I. INTRODUCTION

The growing demand for high system capacity, high transmission rate and broadband access motivates researchers to search a new technology which is suitable to the above scenarios. Ref. [1] shows that these system requirements of future communication systems can be met by the combination of two powerful technologies in the physical layer design: multiple-input multiple-output (MIMO) antennas and orthogonal frequency division multiplexing (OFDM) modulation, resulting in MIMO-OFDM technique. Multiple antennas at the transmitter and receiver provide diversity in a fading environment without increasing the transmitting power. OFDM is a promising approach for high delay spread channels or high data rate with lower complexity of equalizers. Therefore MIMO-OFDM has become one of the most promising physical layer schemes in the fourth generation wireless communication systems.

Most of former research results have been provided through theoretical analysis or computer simulation. Recently, a great deal of experimental MIMO-OFDM platforms has sprung up. However, most of them work in non-real time mode[2-4]. It is necessary to develop a MIMO-OFDM real-time platform. Rice University's WARP[5-6] is a scalable and extensible programmable wireless platform, built from the ground up, to prototype advanced wireless networks. By referring to WARP project, we develop a 2x2 MIMO-OFDM real-time platform on Sundance's DSP and FPGA development kits. The difference between our system with WARP exists: DUC and DDC module to fit into Sundance's platform, Frame Detection, Fine timing synchronization, Symbol equalization and demodulation, etc.

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The rest of the paper is organized as follows. In Section II, hardware architecture of the platform and the main parameters of building blocks are described. In Section III, physical layer design is shown, also synchronization, space-time block coding and soft demapper algorithms are proposed for multiple transmit and receive antennas. In Section IV, some test results of our platform are analyzed. Finally, conclusions are drawn in Section V.

II. HARDWARE ARCHITECTURE OF THE PLATFORM

The whole hardware consists of four key parts: the Digital Signal Processor (DSP), the Field Programmable Gate Arrays (FPGA), the uniform linear antenna array and the four-channel RF front-end. First two parts are integrated and provided by Sundance SDR platform. The detailed configuration is shown in Fig. 1. The transmitter board consists of three TIMs(Texas Instruments Module) embedded in the PCI SMT310Q carrier board: one SMT365-4-1 and two SMT350+SMT368, interconnected with two Sundance High Speed Buses. As one SMT350 module support one channel DAC and two channel ADC, only one SMT350 module is used at the receiver part. Baseband signal processing, such as frame detection, CFO (Carrier Frequency Offset) estimation, time synchronization, channel estimation, modulation and demodulation, and Intermediate Frequency (IF) processing (DUC at the transmitter and DDC at the receiver) are implemented in the FPGA board, namely SMT368 modules in our system. The DSPs on boards are assigned to do some configurations, such as, delivering the parameters from PC to the FPGA board. Additionally, PCs are used to capture the video source in the transmitter and display the recovery video data, SNR and BER in the receiver, etc.

III. 2X2 REAL-TIME MIMO-OFDM SYSTEM

The architecture of the transmitter and the receiver is

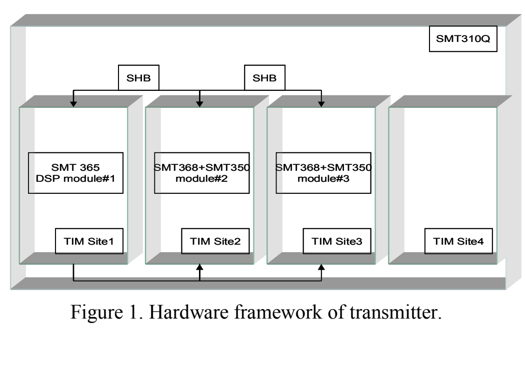

Figure 1. Hardware framework of transmitter.

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illustrated in Fig. 3 and Fig. 4 respectively. The adopted signal format is in accordance with 802.11n standard. In this section, a general description of the algorithms which are implemented on the FPGA board of the platform will be provided, including physical layer description, digital up/down converter, synchronization, space-time block coding/decoding and soft decoding for scenarios with two transmit and receive antennas.

A. Physical Layer Description

The physical layer is a simplification version of the IEEE 802.11n PHY standard [7] with two transmitting antennas and two receiving antennas. 802.11n PHY technique supports 20MHz and 40MHz bandwidth mode.

In the paper, we use the HT-mixed physical layer convergence procedure protocol data unit (PPDU) format and 16.384 MHz bandwidth mode. Fig. 6 shows the HT-mixed PPDU format adopted. In the platform, the L-SIG, HT-SIG and HT-STF are not used, because the L-STF, L-LTF, HT-LTF can replace them to make the target of carrying the information known to the receiver.

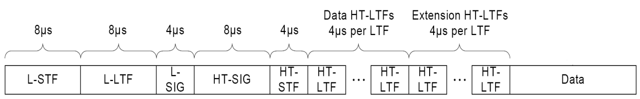

Figure 2. the HT-mixed PPDU format

1) Preamble definition: The first three parts (L-STF, L-LTF, HT-LTF) are used for synchronization and channel estimation at the receiver. L-STF composed of ten short repeated sequences, is basically used for the start of frame (SOF) detection and the coarse carrier frequency offset (CFO) estimation. L-LTF is made up of two long repeated sequences and a long GI whose time is twice as the common GI and it mainly used for fine synchronization and channel estimation. In addition, the channel state is estimated by using HT-LTF which has two sequences.

2) Data field: First of all, bit stream which has been scrambled and interleaved is separated into spatial streams by stream parser. Secondly, spatial streams are mapped into constellation. Thirdly, the points on the constellation are through the STBC encoder to transform the spatial streams to space-time streams. Fourthly, spatial mapper maps space-time streams into transmit chains. And lastly, the transmit chains are inserted pilot, IFFT modulated, added CP (Cyclic Prefix), then transmitted through the DUC, DAC and RF modules.

B. Digital Up/Down Converter

The digital up converter (DUC) and the digital down converter (DDC) are important components of this platform. The carrier modulation/demodulation is realized by mixer and multiplier with the frequency of 69MHz. The sample rate up/down is implemented through cascading the Cascaded Integrator Comb (CIC) filters, compensation filter and matched filter. CIC filter performs sample rate conversion by using only additions and subtractions not multipliers. But it has a passband droop shortcoming, so we need a corresponding compensation filter to make the passband flat. The matched filter is used to make the transmitter and the receiver paired up and it can improve the SNR by reducing the noise.

C. Synchronization

In this section, we will describe the synchronization algorithms which are implemented on the FPGA board. According to the 802.11n, L-STF and L-LTF are used for synchronization [8]. In our MIMO-OFDM platform, we revise the traditional synchronization algorithms and propose a novel synchronization method adapt to multiple antennas. The coarse

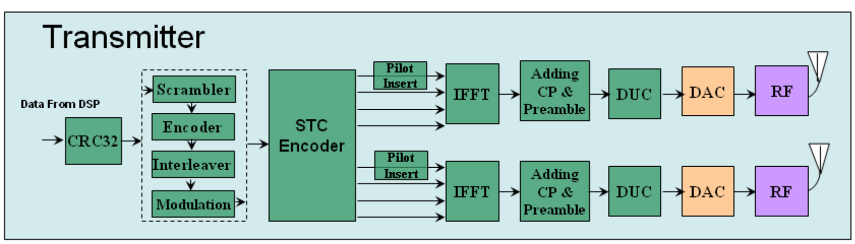

Figure 3 System architecture of the transmitter

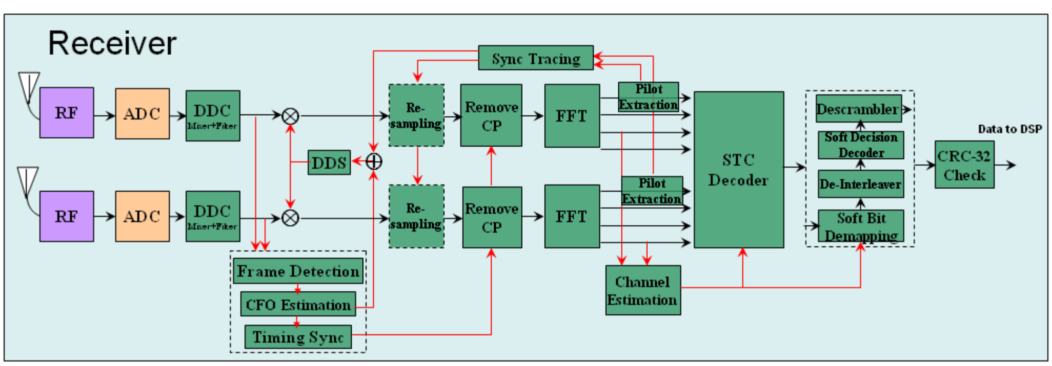

Figure 4. System architecture of the receiver

synchronization can be calculated as:

$$\Phi_{n,coarse} = \left|\sum_{i=1}^{Nr} R_{i,n,coarse}\right|^2 \Big/ \left|\sum_{i=1}^{Nr} P_{i,n}\right|^2 \tag{1}$$

$$R_{i,n,coarse} = \sum_{k=0}^{N_1-1}(r^*_{i,n+k} r_{i,n+k+N_1})$$

$$P_{i,n} = \sum_{k=0}^{N_1-1} r^*_{i,n+k} r_{i,n+k}$$

Where i is the index of antenna, N_r is the total number of antenna, $r_{i,n}$ is the received sequences, N_1 is the length of the correlation window, $R_{i,n,coarse}$ is the auto-correlation of the received data and $P_{i,n}$ is the enenergy of received data.

We use two receive antennas data (Algorithm 2) to do coarse synchronization in real-time platform, whereas in WARP only one antenna(Algorithm 1) is used as a traditonal SISO system. Fig. 7 compares the probability of frame error detection between two different algorithms when the False Alarm Rate is setting to 0.01.

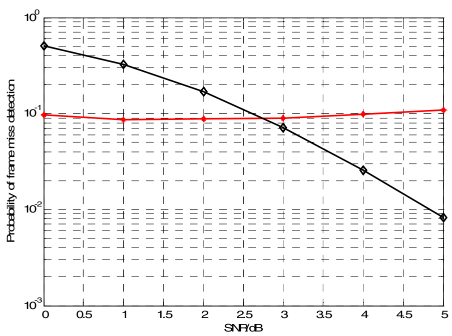

Figure 5. Probability of frame miss detection of Algorithm 1 and Agorithm 2 for coarse synchronizaition.

As shown in Fig. 5, the traditional Algorithm 1 gets a almost flat performance curve, but Algorithm 2 shows better performance at SNR above 2.7dB, which is usually the regular communication condition. In nature, Algorithm 2 reduces the fluctuation of correlation value, and which is essentially get from spatial diversity of multiple antennas system.

The fine synchronization can be calculated as:

$$N_{fine} = \arg\max_{n\in n_{coarse}} \sum_{k=0}^{N_1-1}(s^*_k r_{n+k}) \Big/ R_n^{\,2} \tag{3}$$

Where s_k^* is the training sequence, $\sum_{k=0}^{N_1-1} s^*_k r_{n+k}$ is the co-correlation of received data and L-LTF stored in the receiver ahead, N_{fine} is the beginning sample of the frame.

The estimation of Frequency offset Δf_F is calculated as followed:

$$\Delta f_F = \frac{1}{2\pi \cdot N_1}\arctan\left(\frac{real(J)}{imag(J)}\right), \tag{4}$$

Where

$$J = \sum_{k=0}^{N_1-1} r_{n+k} r^*_{n+N_1+k} = e^{-j\theta}\sum_{k=0}^{N_1-1}\left|r_{n+k}\right|^2 .$$

Cordic computational module is used to compensate the carrier offset before the received data entering FFT module to avoid Inter-Carrier Interference (ICI).

D. Space-time Block Coding/Decoding

Alamouti's transmit diversity scheme [9] with two transmit antennas and two receive antennas are used in this paper. Alamouti's scheme is a space-time block code and suitable when two transmit antennas and an arbitrary number of receive antennas are used [10]. As the main and most important characteristic of Alamouti's scheme is simple in the coding and decoding, we select it as an ideal candidate for real-world implementation. In this platform, we just consider when the number of space-time streams equals to the number of spatial streams, and the number is two. The coding matrix is

$$\mathrm{A}_{22} = \begin{bmatrix} s_{k,2n} & s_{k,2n+1} \\ -s^*_{k,2n+1} & s^*_{k,2n} \end{bmatrix} \tag{5}$$

Where $s_{k,m}$ is the data of space-time streams, k is the index of subcarriers, m is the index of OFDM data symbols. The decoding process is done in case of two antennas as our system as,

$$\begin{bmatrix} \hat{s}_{k,2n} \\ \hat{s}_{k,2n+1} \end{bmatrix} = \left(\sum_{i=1}^{2} \tilde{H}^H_{i,k}\tilde{H}_{i,k}\right)^{-1} \sum_{i=1}^{2}\tilde{H}^H_{i,k}\begin{bmatrix} y_{k,i}(2n) \\ y^*_{k,i}(2n+1)\end{bmatrix}, \tag{6}$$

$$\tilde{H}_{i,k} = \begin{bmatrix} h^*_{i1,k} & h_{i2,k} \\ h^*_{i2,k} & -h_{i1,k}\end{bmatrix}$$

Where $y_{k,i}(m)$ denotes the post-FFT data at k-th subcarrier and m-th OFDM symbol of the i-th receiving antenna. $h_{ij,k}$ denotes the channel response between j-th transmitting antenna and i-th receiving antenna at k-th subcarrier, function which is estimated by the HT-LTF. Unlike complex division computation to recover the symbol in WARP, only multiplication operation is used in our system as described in next part.

E. Soft demapper

Significantly, a new M-QAM soft-demapper method is used to reduce the complexity of implementation and resources occupancy of hardware boards. First, We define $A_k = \sum_{i=1}^{2}\tilde{H}^H_{i,k}\tilde{H}_{i,k}$ and $z_k(m) = \sum_{i=1}^{2}\tilde{H}^H_{i,k} y_{k,i}(m)$, thus the estimation of symbol $s_k(m)$ is expressed by $A_k^{-1} z_k(m)$. The method can be modeled as：

$$LLR_{I,l} = \begin{cases} \mathrm{Re}(A_k z_k(m)) & l = 1 \\ -\left|LLR_{I,l-1}\right| + d_{I,l}\left|A\right|^2 & l = 2,3,\ldots,\frac{1}{2}\log_2 M \end{cases} \tag{7}$$

Where $LLR_{I,l}$ is the I path Log-Likelihood Ratio, and $d_{I,l}$ is the half of the decision field of M-QAM. Equation (7) gives the method of I part LLR calculation and the Q part is as same as I part. Without using the cordic equalization which consumes a lot of hardware resources. Resources which are important to hardware design engineers will be saved in our new method.

IV. Test Results

During the test period, the transmitter and the receiver cabinets are located in two adjacent indoor rooms. Fig. 6 shows the receiver cabinet of 2x2 MIMO-OFDM real-time system, the transmitter is located in the neighboring room, both with 4 antennas on the top of the cabinet. The tests are finished on the case that: the distance between transmit and receive cabinets are fixed and the linear array of antenna is used. Fig. 7 illustrates the test indoor environment.

The main parameters of 2x2 MIMO-OFDM real-time platform are outlined in Table I. In the testing, the data frame length is set to3840.

TABLE I. Platform Parametres

Parameters	Value
Number of subcarriers	48
Number of pilot	4
Total number of subcarriers	52
IDFT length	64
Length of data symbol	80
Constellation maping mode	QPSK
Sample Rate	81.92MHz
Intermediate Frequency	69MHz
Length of L-STF and L-LTF	160
Length of HT-LTF	80

Figure 6 Receiver cabinet

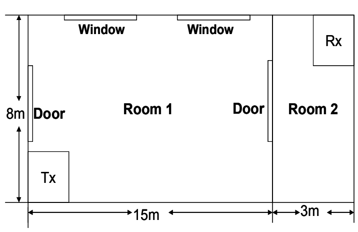

Figure 7. Indoor test environment

Fig. 8 shows the constellation recovered at the receiver in real time. Fig. 9 presents the real-time video transmission picture on our real-time platform. The testing shows our 2x2 MIMO-OFDM system work well, and it will become a convenient tool to evaluate and testify the performance and availability of MIMO system.

Figure 8 Constellation recovered at the reciever

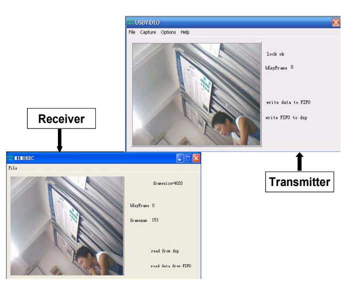

Figure 9. Demonstration of video transmission

V. Conclusions

A flexible 2x2 MIMO-OFDM platform is presented in the paper. In the FPGA section, Sundance board is provided for the implementation of baseband and IF signal processing algorithms. Some necessary receiver algorithms, such as OFDM synchronization, channel estimation, decoding of Alamouti STBC, soft demapper and other components, are implemented in FPGA. Test results obtained in indoor environment show that our platform can work as a base to demonstrate other advanced algorithms and upper layer techniques.

VI. References

[1] Sampath, H.,Talwar, S.,Tellado, J., "A fourth-generation MIMO-OFDM broadband wirelesssystem: design, performance, and field tria l results," *Communications Magazine*, IEEE , Volume: 40 , Issue: 9, 2002.

[2] Ventura, L.M., Nieto, X., Gregoire, J.P., " A Broadband Wireless MIMO-OFDM Demonstrator. Design and Measurement Results," *Personal, Indoor and Mobile Radio Communications*, 2006 IEEE 17th International Symposium on 11-14 Sept. 2006.

[3] Guillen, A.F., Guillaud, M., Caire, G., "A MIMO-OFDM Platform for Wireless Local Area Networks," *Signals, Systems and Computers*, 2005. Conference Record of the Thirty-Ninth Asilomar Conference on Oct. 28 2005-Nov. 1 2005 pp. 82 - 86.

[4] Nieto, X., Ventura, L.M., Mollfulleda, A., "GEDOMIS: a broadband wireless MIMO-OFDM testbed, design and implementation," *Testbeds and Research Infrastructures for the development of Networks and Communities*, 2006. pp. 121.

[5] "Rice University WARP Project, http://warp.rice.edu"

[6] Kiarash Amiri, Yang Sun, Patrick Murphy, "WARP, a Modular Testbed for Configurable Wireless NetworkResearch at Rice", *Proceedings of IEEE SWRIF*, 2007

[7] IEEE Std 802.11n™-2009, "IEEE STANDARD for Information Technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements. Oct. 2009.

[8] En Zhou, Xiaolin Hou, Jianping Chen, "FPGA Implementation and Experimental Performaces of a Novel Timing Synchronization Method in MIMO-OFDM Tesbed," *Proc. of 14th Asia-Pacific Conference on Communications*, APCC 2008. Oct. 2008

[9] S. M. Alamouti, "A simple transmit diversity technique for wireless communications," *IEEE Journal on Selected Areas in Communication*, vol. 16, pp. 1451-1458, Oct. 1998.

[10] Junior, L.H.M., Junior, R.R.S., Silveira, M, " An FPGA implementation of Alamouti's transmit diversity technique applied to an OFDM system," *Antennas and Propagation Society International Symposium* 2006, pp. 149 – 152.